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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	MIPS32® M-Class
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, PMP, SPI, SQI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	97
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	2.1V ~ 3.6V
Data Converters	A/D 48x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C
Mounting Type	Surface Mount
Package / Case	124-VFTLA Dual Rows, Exposed Pad
Supplier Device Package	124-VTLA (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mz1024efk124-e-tl

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

TABLE 1-4: OC1 THROUGH OC9 PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number				Pin Type	Buffer Type	Description
	64-pin QFN/ TQFP	100-pin TQFP	124-pin VTLA	144-pin TQFP/ LQFP			
Output Compare							
OC1	PPS	PPS	PPS	PPS	O	—	Output Compare Outputs 1-9
OC2	PPS	PPS	PPS	PPS	O	—	
OC3	PPS	PPS	PPS	PPS	O	—	
OC4	PPS	PPS	PPS	PPS	O	—	
OC5	PPS	PPS	PPS	PPS	O	—	
OC6	PPS	PPS	PPS	PPS	O	—	
OC7	PPS	PPS	PPS	PPS	O	—	
OC8	PPS	PPS	PPS	PPS	O	—	
OC9	PPS	PPS	PPS	PPS	O	—	
OCFA	PPS	PPS	PPS	PPS	I	ST	Output Compare Fault A Input
OCFB	30	44	B24	62	I	ST	Output Compare Fault B Input

Legend: CMOS = CMOS-compatible input or output
 ST = Schmitt Trigger input with CMOS levels
 TTL = Transistor-transistor Logic input buffer
 Analog = Analog input
 O = Output
 PPS = Peripheral Pin Select
 P = Power
 I = Input

TABLE 1-5: EXTERNAL INTERRUPTS PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number				Pin Type	Buffer Type	Description
	64-pin QFN/ TQFP	100-pin TQFP	124-pin VTLA	144-pin TQFP/ LQFP			
External Interrupts							
INT0	46	71	A48	104	I	ST	External Interrupt 0
INT1	PPS	PPS	PPS	PPS	I	ST	External Interrupt 1
INT2	PPS	PPS	PPS	PPS	I	ST	External Interrupt 2
INT3	PPS	PPS	PPS	PPS	I	ST	External Interrupt 3
INT4	PPS	PPS	PPS	PPS	I	ST	External Interrupt 4

Legend: CMOS = CMOS-compatible input or output
 ST = Schmitt Trigger input with CMOS levels
 TTL = Transistor-transistor Logic input buffer
 Analog = Analog input
 O = Output
 PPS = Peripheral Pin Select
 P = Power
 I = Input

TABLE 4-2: BOOT FLASH 1 SEQUENCE AND CONFIGURATION WORDS SUMMARY

Virtual Address (BFC4_#)	Register Name	Bit Range	Bits																All Reset
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
FF40	ABF1DEVCFG3	31:0	Note: See Table 34-2 for the bit descriptions.																XXXX
FF44	ABF1DEVCFG2	31:0																	XXXX
FF48	ABF1DEVCFG1	31:0																	XXXX
FF4C	ABF1DEVCFG0	31:0																	XXXX
FF50	ABF1DEVCP3	31:0																	XXXX
FF54	ABF1DEVCP2	31:0																	XXXX
FF58	ABF1DEVCP1	31:0																	XXXX
FF5C	ABF1DEVCP0	31:0																	XXXX
FF60	ABF1DEVSIGN3	31:0																	XXXX
FF64	ABF1DEVSIGN2	31:0																	XXXX
FF68	ABF1DEVSIGN1	31:0	XXXX																
FF6C	ABF1DEVSIGN0	31:0	XXXX																
FFC0	BF1DEVCFG3	31:0	Note: See Table 34-1 for the bit descriptions.																XXXX
FFC4	BF1DEVCFG2	31:0																	XXXX
FFC8	BF1DEVCFG1	31:0																	XXXX
FFCC	BF1DEVCFG0	31:0																	XXXX
FFD0	BF1DEVCP3	31:0																	XXXX
FFD4	BF1DEVCP2	31:0																	XXXX
FFD8	BF1DEVCP1	31:0																	XXXX
FFDC	BF1DEVCP0	31:0																	XXXX
FFE0	BF1DEVSIGN3	31:0																	XXXX
FFE4	BF1DEVSIGN2	31:0																	XXXX
FFE8	BF1DEVSIGN1	31:0	XXXX																
FFEC	BF1DEVSIGN0	31:0	XXXX																
FFF0	BF1SEQ3	31:16	CSEQ<15:0>																XXXX
		15:0	TSEQ<15:0>																XXXX
FFF4	BF1SEQ2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	XXXX	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	XXXX	
FFF8	BF1SEQ1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	XXXX	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	XXXX	
FFFC	BF1SEQ0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	XXXX	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	XXXX	

Legend: x = unknown value on Reset; — = Reserved, read as '1'. Reset values are shown in hexadecimal.

TABLE 4-11: SYSTEM BUS TARGET 3 REGISTER MAP

Virtual Address (BF8F_#)	Register Name	Bit Range	Bits															All Resets	
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1		16/0
8C20	SBT3ELOG1	31:16	MULTI	—	—	—	CODE<3:0>				—	—	—	—	—	—	—	—	0000
		15:0	INITID<7:0>							REGION<3:0>				—	CMD<2:0>			0000	
8C24	SBT3ELOG2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	GROUP<1:0>		0000	
8C28	SBT3ECON	31:16	—	—	—	—	—	—	—	ERRP	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
8C30	SBT3ECLRS	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000	
8C38	SBT3ECLRM	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000	
8C40	SBT3REG0	31:16	BASE<21:6>															xxxx	
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>				—	—	—	xxxx	
8C50	SBT3RD0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8C58	SBT3WR0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8C60	SBT3REG1	31:16	BASE<21:6>															xxxx	
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>				—	—	—	xxxx	
8C70	SBT3RD1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8C78	SBT3WR1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8C80	SBT3REG2	31:16	BASE<21:6>															xxxx	
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>				—	—	—	xxxx	
8C90	SBT3RD2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8C98	SBT3WR2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note: For reset values listed as 'xxxx', please refer to Table 4-6 for the actual reset values.

TABLE 4-14: SYSTEM BUS TARGET 6 REGISTER MAP

Virtual Address (BF8E_#)	Register Name	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	
9820	SBT6ELOG1	31:16	MULTI	—	—	—	CODE<3:0>			—	—	—	—	—	—	—	—	0000
		15:0	INITID<7:0>							REGION<3:0>				—	CMD<2:0>			0000
9824	SBT6ELOG2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	GROUP<1:0>		0000
9828	SBT6ECON	31:16	—	—	—	—	—	—	—	ERRP	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
9830	SBT6ECLRS	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
9838	SBT6ECLRM	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
9840	SBT6REG0	31:16	BASE<21:6>															xxxx
		15:0	BASE<5:0>					PRI	—	SIZE<4:0>					—	—	—	xxxx
9850	SBT6RD0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0
9858	SBT6WR0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0
9860	SBT6REG1	31:16	BASE<21:6>															xxxx
		15:0	BASE<5:0>					PRI	—	SIZE<4:0>					—	—	—	xxxx
9870	SBT6RD1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0
9878	SBT6WR1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note: For reset values listed as 'xxxx', please refer to Table 4-6 for the actual reset values.

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

REGISTER 4-8: SBTxREGy: SYSTEM BUS TARGET 'x' REGION 'y' REGISTER (‘x’ = 0-13; ‘y’ = 0-8)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BASE<21:14>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BASE<13:6>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0	U-0
	BASE<5:0>						PRI	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0
	SIZE<4:0>					—	—	—

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as ‘0’

-n = Value at POR

‘1’ = Bit is set

‘0’ = Bit is cleared

bit 31-10 **BASE<21:0>**: Region Base Address bits

bit 9 **PRI**: Region Priority Level bit

1 = Level 2

0 = Level 1

bit 8 **Unimplemented**: Read as ‘0’

bit 7-3 **SIZE<4:0>**: Region Size bits

Permissions for a region are only active if the SIZE is non-zero.

11111 = Region size = $2^{(SIZE-1)} \times 1024$ (bytes)

•

•

•

00001 = Region size = $2^{(SIZE-1)} \times 1024$ (bytes)

00000 = Region is not present

bit 2-0 **Unimplemented**: Read as ‘0’

Note 1: Refer to Table 4-6 for the list of available targets and their descriptions.

2: For some target regions, certain bits in this register are read-only with preset values. See Table 4-6 for more information.

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

REGISTER 4-10: SBTxWRy: SYSTEM BUS TARGET 'x' REGION 'y' WRITE PERMISSIONS
REGISTER ('x' = 0-13; 'y' = 0-8)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	R/W-0	R/W-1	R/W-1	R/W-1
	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

bit 31-4 **Unimplemented:** Read as '0'

bit 3 **Group3:** Group 3 Write Permissions bits

1 = Privilege Group 3 has write permission

0 = Privilege Group 3 does not have write permission

bit 2 **Group2:** Group 2 Write Permissions bits

1 = Privilege Group 2 has write permission

0 = Privilege Group 2 does not have write permission

bit 1 **Group1:** Group 1 Write Permissions bits

1 = Privilege Group 1 has write permission

0 = Privilege Group 1 does not have write permission

bit 0 **Group0:** Group 0 Write Permissions bits

1 = Privilege Group 0 has write permission

0 = Privilege Group 0 does not have write permission

Note 1: Refer to Table 4-6 for the list of available targets and their descriptions.

2: For some target regions, certain bits in this register are read-only with preset values. See Table 4-6 for more information.

TABLE 12-12: PORTE REGISTER MAP FOR 64-PIN DEVICES ONLY

Virtual Address (BF86_#)	Register Name(s)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0400	ANSELE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	ANSE7	ANSE6	ANSE5	ANSE4	—	—	—	—	00F0
0410	TRISE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	TRISE7	TRISE6	TRISE5	TRISE4	TRISE3	TRISE2	TRISE1	TRISE0	00FF
0420	PORTE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	RE7	RE6	RE5	RE4	RE3	RE2	RE1	RE0	xxxx
0430	LATE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	LATE7	LATE6	LATE5	LATE4	LATE3	LATE2	LATE1	LATE0	xxxx
0440	ODCE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	ODCE7	ODCE6	ODCE5	ODCE4	ODCE3	ODCE2	ODCE1	ODCE0	0000
0450	CNPUE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CNPUE7	CNPUE6	CNPUE5	CNPUE4	CNPUE3	CNPUE2	CNPUE1	CNPUE0	0000
0460	CNPDE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CNPDE7	CNPDE6	CNPDE5	CNPDE4	CNPDE3	CNPDE2	CNPDE1	CNPDE0	0000
0470	CNCONE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	EDGE DETECT	—	—	—	—	—	—	—	—	—	—	—	0000
0480	CNENE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CNENE7	CNENE6	CNENE5	CNENE4	CNENE3	CNENE2	CNENE1	CNENE0	0000
0490	CNSTATE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CN STATE7	CN STATE6	CN STATE5	CN STATE4	CN STATE3	CN STATE2	CN STATE1	CN STATE0	0000
04A0	CNNEE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CNNEE7	CNNEE6	CNNEE5	CNNEE4	CNNEE3	CNNEE2	CNNEE1	CNNEE0	0000
04B0	CNFE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CNFE7	CNFE6	CNFE5	CNFE4	CNFE3	CNFE2	CNFE1	CNFE0	0000
04C0	SRCON0E	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	SR0E3	SR0E2	SR0E1	SR0E0	0000
04D0	SRCON1E	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	SR1E3	SR1E2	SR1E1	SR1E0	0000

Legend: x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 “CLR, SET, and INV Registers”** for more information.

TABLE 12-22: PERIPHERAL PIN SELECT INPUT REGISTER MAP (CONTINUED)

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
1488	U5RXR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	U5RXR<3:0>				0000
148C	U5CTSR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	U5CTSR<3:0>				0000
1490	U6RXR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	U6RXR<3:0>				0000
1494	U6CTSR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	U6CTSR<3:0>				0000
149C	SDI1R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	SDI1R<3:0>				0000
14A0	SS1R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	SS1R<3:0>				0000
14A8	SDI2R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	SDI2R<3:0>				0000
14AC	SS2R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	SS2R<3:0>				0000
14B4	SDI3R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	SDI3R<3:0>				0000
14B8	SS3R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	SS3R<3:0>				0000
14C0	SDI4R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	SDI4R<3:0>				0000
14C4	SS4R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	SS4R<3:0>				0000
14CC	SDI5R ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	SDI5R<3:0>				0000
14D0	SS5R ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	SS5R<3:0>				0000
14D8	SDI6R ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	SDI6R<3:0>				0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

- Note** 1: This register is not available on 64-pin devices.
2: This register is not available on devices without a CAN module.

REGISTER 23-2: PMMODE: PARALLEL PORT MODE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —
23:16	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —
15:8	R-0 BUSY	R/W-0 IRQM<1:0>	R/W-0 IRQM<1:0>	R/W-0 INCM<1:0>	R/W-0 INCM<1:0>	R/W-0 MODE16	R/W-0 MODE<1:0>	R/W-0 MODE<1:0>
7:0	R/W-0 WAITB<1:0> ⁽¹⁾	R/W-0 WAITB<1:0> ⁽¹⁾	R/W-0 WAITB<1:0> ⁽¹⁾	R/W-0 WAITM<3:0> ⁽¹⁾	R/W-0 WAITM<3:0> ⁽¹⁾	R/W-0 WAITM<3:0> ⁽¹⁾	R/W-0 WAITE<1:0> ⁽¹⁾	R/W-0 WAITE<1:0> ⁽¹⁾

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **BUSY:** Busy bit (Master mode only)

1 = Port is busy

0 = Port is not busy

bit 14-13 **IRQM<1:0>:** Interrupt Request Mode bits

11 = Reserved, do not use

10 = Interrupt is generated when Read Buffer 3 is read or Write Buffer 3 is written (Buffered PSP mode) or on a read or write operation when PMA<1:0> = 11 (Addressable Slave mode only)

01 = Interrupt is generated at the end of the read/write cycle

00 = No Interrupt is generated

bit 12-11 **INCM<1:0>:** Increment Mode bits

11 = Slave mode read and write buffers auto-increment (MODE<1:0> = 00 only)

10 = Decrement ADDR<15:0> and ADDR<14> by 1 every read/write cycle⁽²⁾

01 = Increment ADDR<15:0> and ADDR<14> by 1 every read/write cycle⁽²⁾

00 = No increment or decrement of address

bit 10 **MODE16:** 8/16-bit Mode bit

1 = 16-bit mode: a read or write to the data register invokes a single 16-bit transfer

0 = 8-bit mode: a read or write to the data register invokes a single 8-bit transfer

bit 9-8 **MODE<1:0>:** Parallel Port Mode Select bits

11 = Master mode 1 (PMCSx, PMRD/PMWR, PMENB, PMA<x:0>, and PMD<15:0>)⁽³⁾

10 = Master mode 2 (PMCSx, PMRD, PMWR, PMA<x:0>, and PMD<15:0>)⁽³⁾

01 = Enhanced Slave mode, control signals (PMRD, PMWR, PMCSx, PMD<7:0>, and PMA<1:0>)

00 = Legacy Parallel Slave Port, control signals (PMRD, PMWR, PMCSx, and PMD<7:0>)

bit 7-6 **WAITB<1:0>:** Data Setup to Read/Write Strobe Wait States bits⁽¹⁾

11 = Data wait of 4 TPBCLK2; multiplexed address phase of 4 TPBCLK2

10 = Data wait of 3 TPBCLK2; multiplexed address phase of 3 TPBCLK2

01 = Data wait of 2 TPBCLK2; multiplexed address phase of 2 TPBCLK2

00 = Data wait of 1 TPBCLK2; multiplexed address phase of 1 TPBCLK2 (default)

Note 1: Whenever WAITM<3:0> = 0000, WAITB and WAITE bits are ignored and forced to 1 TPBCLK2 cycle for a write operation; WAITB = 1 TPBCLK2 cycle, WAITE = 0 TPBCLK2 cycles for a read operation.

2: Address bits 14 and 15 are not subject to auto-increment/decrement if configured as Chip Select.

3: The PMD<15:8> bits are not active if the MODE16 bit = 1.

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

REGISTER 29-1: CiCON: CAN MODULE CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	S/HC-0	R/W-1	R/W-0	R/W-0
	—	—	—	—	ABAT	REQOP<2:0>		
23:16	R-1	R-0	R-0	R/W-0	U-0	U-0	U-0	U-0
	OPMOD<2:0>			CANCAP	—	—	—	—
15:8	R/W-0	U-0	R/W-0	U-0	R-0	U-0	U-0	U-0
	ON ⁽¹⁾	—	SIDLE	—	CANBUSY	—	—	—
7:0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	DNCNT<4:0>				

Legend: HC = Hardware Clear S = Settable bit
R = Readable bit W = Writable bit P = Programmable bit r = Reserved bit
U = Unimplemented bit -n = Bit Value at POR: ('0', '1', x = Unknown)

bit 31-28 **Unimplemented:** Read as '0'

bit 27 **ABAT:** Abort All Pending Transmissions bit
1 = Signal all transmit buffers to abort transmission
0 = Module will clear this bit when all transmissions aborted

bit 26-24 **REQOP<2:0>:** Request Operation Mode bits
111 = Set Listen All Messages mode
110 = Reserved - Do not use
101 = Reserved - Do not use
100 = Set Configuration mode
011 = Set Listen Only mode
010 = Set Loopback mode
001 = Set Disable mode
000 = Set Normal Operation mode

bit 23-21 **OPMOD<2:0>:** Operation Mode Status bits
111 = Module is in Listen All Messages mode
110 = Reserved
101 = Reserved
100 = Module is in Configuration mode
011 = Module is in Listen Only mode
010 = Module is in Loopback mode
001 = Module is in Disable mode
000 = Module is in Normal Operation mode

bit 20 **CANCAP:** CAN Message Receive Time Stamp Timer Capture Enable bit
1 = CANTMR value is stored on valid message reception and is stored with the message
0 = Disable CAN message receive time stamp timer capture and stop CANTMR to conserve power

bit 19-16 **Unimplemented:** Read as '0'

bit 15 **ON:** CAN On bit⁽¹⁾
1 = CAN module is enabled
0 = CAN module is disabled

bit 14 **Unimplemented:** Read as '0'

Note 1: If the user application clears this bit, it may take a number of cycles before the CAN module completes the current transaction and responds to this request. The user application should poll the CANBUSY bit to verify that the request has been honored.

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

REGISTER 29-3: CiINT: CAN INTERRUPT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0
	IVRIE	WAKIE	CERRIE	SERRIE	RBOVIE	—	—	—
23:16	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	MODIE	CTMRIE	RBIE	TBIE
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0
	IVRIF	WAKIF	CERRIF	SERRIF ⁽¹⁾	RBOVIF	—	—	—
7:0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	MODIF	CTMRIF	RBIF	TBIF

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 31 **IVRIE:** Invalid Message Received Interrupt Enable bit
 1 = Interrupt request is enabled
 0 = Interrupt request is not enabled
- bit 30 **WAKIE:** CAN Bus Activity Wake-up Interrupt Enable bit
 1 = Interrupt request is enabled
 0 = Interrupt request is not enabled
- bit 29 **CERRIE:** CAN Bus Error Interrupt Enable bit
 1 = Interrupt request is enabled
 0 = Interrupt request is not enabled
- bit 28 **SERRIE:** System Error Interrupt Enable bit
 1 = Interrupt request is enabled
 0 = Interrupt request is not enabled
- bit 27 **RBOVIE:** Receive Buffer Overflow Interrupt Enable bit
 1 = Interrupt request is enabled
 0 = Interrupt request is not enabled
- bit 26-20 **Unimplemented:** Read as '0'
- bit 19 **MODIE:** Mode Change Interrupt Enable bit
 1 = Interrupt request is enabled
 0 = Interrupt request is not enabled
- bit 18 **CTMRIE:** CAN Timestamp Timer Interrupt Enable bit
 1 = Interrupt request is enabled
 0 = Interrupt request is not enabled
- bit 17 **RBIE:** Receive Buffer Interrupt Enable bit
 1 = Interrupt request is enabled
 0 = Interrupt request is not enabled
- bit 16 **TBIE:** Transmit Buffer Interrupt Enable bit
 1 = Interrupt request is enabled
 0 = Interrupt request is not enabled
- bit 15 **IVRIF:** Invalid Message Received Interrupt Flag bit
 1 = An invalid messages interrupt has occurred
 0 = An invalid message interrupt has not occurred

Note 1: This bit can only be cleared by turning the CAN module off and on by clearing or setting the ON bit (CiCON<15>).

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

REGISTER 29-5: CiTREC: CAN TRANSMIT/RECEIVE ERROR COUNT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	R-0	R-0	R-0	R-0	R-0	R-0
	—	—	TXBO	TXBP	RXBP	TXWARN	RXWARN	EWARN
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	TERRCNT<7:0>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	RERRCNT<7:0>							

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 31-22 **Unimplemented:** Read as '0'
- bit 21 **TXBO:** Transmitter in Error State Bus OFF (TERRCNT ≥ 256)
- bit 20 **TXBP:** Transmitter in Error State Bus Passive (TERRCNT ≥ 128)
- bit 19 **RXBP:** Receiver in Error State Bus Passive (RERRCNT ≥ 128)
- bit 18 **TXWARN:** Transmitter in Error State Warning (128 > TERRCNT ≥ 96)
- bit 17 **RXWARN:** Receiver in Error State Warning (128 > RERRCNT ≥ 96)
- bit 16 **EWARN:** Transmitter or Receiver is in Error State Warning
- bit 15-8 **TERRCNT<7:0>:** Transmit Error Counter
- bit 7-0 **RERRCNT<7:0>:** Receive Error Counter

REGISTER 29-6: CiFSTAT: CAN FIFO STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	FIFOIP31	FIFOIP30	FIFOIP29	FIFOIP28	FIFOIP27	FIFOIP26	FIFOIP25	FIFOIP24
23:16	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	FIFOIP23	FIFOIP22	FIFOIP21	FIFOIP20	FIFOIP19	FIFOIP18	FIFOIP17	FIFOIP16
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	FIFOIP15	FIFOIP14	FIFOIP13	FIFOIP12	FIFOIP11	FIFOIP10	FIFOIP9	FIFOIP8
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	FIFOIP7	FIFOIP6	FIFOIP5	FIFOIP4	FIFOIP3	FIFOIP2	FIFOIP1	FIFOIP0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 31-0 **FIFOIP<31:0>:** FIFOx Interrupt Pending bits
- 1 = One or more enabled FIFO interrupts are pending
- 0 = No FIFO interrupts are pending

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REGISTER 29-17: CiFLTCON7: CAN FILTER CONTROL REGISTER 7

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN31	MSEL31<1:0>		FSEL31<4:0>				
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN30	MSEL30<1:0>		FSEL30<4:0>				
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN29	MSEL29<1:0>		FSEL29<4:0>				
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN28	MSEL28<1:0>		FSEL28<4:0>				

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 31 **FLTEN31:** Filter 31 Enable bit
1 = Filter is enabled
0 = Filter is disabled
- bit 30-29 **MSEL31<1:0>:** Filter 31 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected
- bit 28-24 **FSEL31<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0
- bit 23 **FLTEN30:** Filter 30 Enable bit
1 = Filter is enabled
0 = Filter is disabled
- bit 22-21 **MSEL30<1:0>:** Filter 30 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected
- bit 20-16 **FSEL30<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

Note: The bits in this register can only be modified if the corresponding filter enable (FLTENN) bit is '0'.

30.0 ETHERNET CONTROLLER

Note: This data sheet summarizes the features of the PIC32MZ EF family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 35. “Ethernet Controller”** (DS60001155) in the “PIC32 Family Reference Manual”, which is available from the Microchip web site (www.microchip.com/PIC32).

The Ethernet controller is a bus master module that interfaces with an off-chip Physical Layer (PHY) to implement a complete Ethernet node in a system.

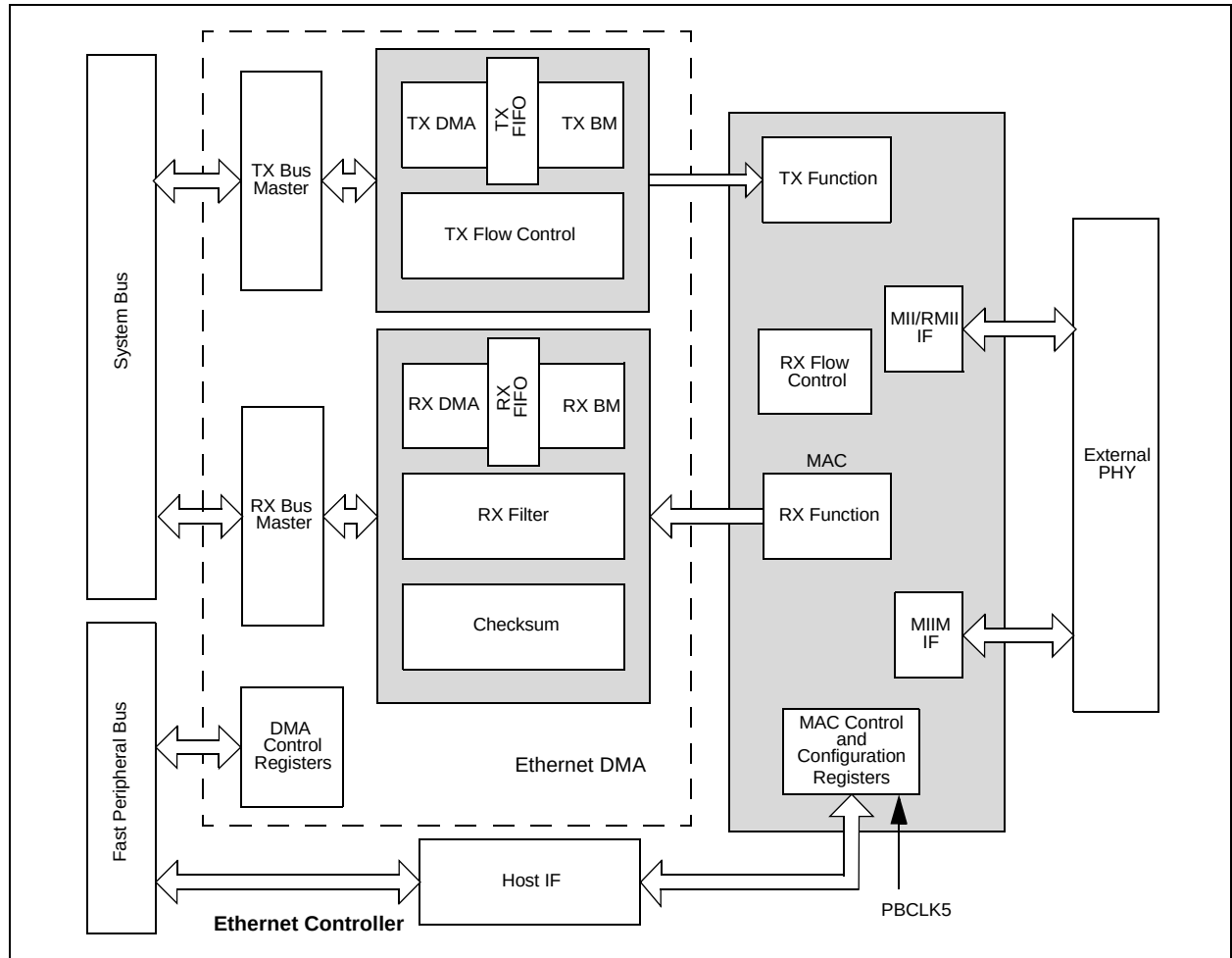
Key features of the Ethernet Controller include:

- Supports 10/100 Mbps data transfer rates
- Supports full-duplex and half-duplex operation

- Supports RMI and MII PHY interface
- Supports MIIM PHY management interface
- Supports both manual and automatic Flow Control
- RAM descriptor-based DMA operation for both receive and transmit path
- Fully configurable interrupts
- Configurable receive packet filtering
 - CRC check
 - 64-byte pattern match
 - Broadcast, multicast and unicast packets
 - Magic Packet™
 - 64-bit hash table
 - Runt packet
- Supports packet payload checksum calculation
- Supports various hardware statistics counters

Figure 30-1 illustrates a block diagram of the Ethernet controller.

FIGURE 30-1: ETHERNET CONTROLLER BLOCK DIAGRAM



PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

REGISTER 30-2: ETHCON2: ETHERNET CONTROLLER CONTROL REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	RXBUFSZ<6:4>		
7:0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0
	RXBUFSZ<3:0>				—	—	—	—

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-11 **Unimplemented:** Read as '0'

bit 10-4 **RXBUFSZ<6:0>:** RX Data Buffer Size for All RX Descriptors (in 16-byte increments) bits

1111111 = RX data Buffer size for descriptors is 2032 bytes

•

•

•

1100000 = RX data Buffer size for descriptors is 1536 bytes

•

•

•

0000011 = RX data Buffer size for descriptors is 48 bytes

0000010 = RX data Buffer size for descriptors is 32 bytes

0000001 = RX data Buffer size for descriptors is 16 bytes

0000000 = Reserved

bit 3-0 **Unimplemented:** Read as '0'

Note 1: This register is only used for RX operations.

2: The bits in this register may only be changed while the RXEN bit (ETHCON1<8>) = 0.

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

REGISTER 30-11: ETHRXFC: ETHERNET CONTROLLER RECEIVE FILTER CONFIGURATION REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	HTEN	MPEN	—	NOTPM	PMMODE<3:0>			
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CRCERREN	CRCOKEN	RUNTERREN	RUNTEN	UCEN	NOTMEEN	MCEN	BCEN

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **HTEN:** Enable Hash Table Filtering bit

1 = Enable Hash Table Filtering

0 = Disable Hash Table Filtering

bit 14 **MPEN:** Magic Packet™ Enable bit

1 = Enable Magic Packet Filtering

0 = Disable Magic Packet Filtering

bit 13 **Unimplemented:** Read as '0'

bit 12 **NOTPM:** Pattern Match Inversion bit

1 = The Pattern Match Checksum must not match for a successful Pattern Match to occur

0 = The Pattern Match Checksum must match for a successful Pattern Match to occur

This bit determines whether Pattern Match Checksum must match in order for a successful Pattern Match to occur.

bit 11-8 **PMMODE<3:0>:** Pattern Match Mode bits

1001 = Pattern match is successful if (NOTPM = 1 XOR Pattern Match Checksum matches) AND (Packet = Magic Packet)^(1,3)

1000 = Pattern match is successful if (NOTPM = 1 XOR Pattern Match Checksum matches) AND (Hash Table Filter match)^(1,1)

0111 = Pattern match is successful if (NOTPM = 1 XOR Pattern Match Checksum matches) AND (Destination Address = Broadcast Address)⁽¹⁾

0110 = Pattern match is successful if (NOTPM = 1 XOR Pattern Match Checksum matches) AND (Destination Address = Broadcast Address)⁽¹⁾

0101 = Pattern match is successful if (NOTPM = 1 XOR Pattern Match Checksum matches) AND (Destination Address = Unicast Address)⁽¹⁾

0100 = Pattern match is successful if (NOTPM = 1 XOR Pattern Match Checksum matches) AND (Destination Address = Unicast Address)⁽¹⁾

0011 = Pattern match is successful if (NOTPM = 1 XOR Pattern Match Checksum matches) AND (Destination Address = Station Address)⁽¹⁾

0010 = Pattern match is successful if (NOTPM = 1 XOR Pattern Match Checksum matches) AND (Destination Address = Station Address)⁽¹⁾

0001 = Pattern match is successful if (NOTPM = 1 XOR Pattern Match Checksum matches)⁽¹⁾

0000 = Pattern Match is disabled; pattern match is always unsuccessful

Note 1: XOR = True when either one or the other conditions are true, but not both.

2: This Hash Table Filter match is active regardless of the value of the HTEN bit.

3: This Magic Packet Filter match is active regardless of the value of the MPEN bit.

Note 1: This register is only used for RX operations.

2: The bits in this register may only be changed while the RXEN bit (ETHCON1<8>) = 0.

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

REGISTER 30-14: ETHIRQ: ETHERNET CONTROLLER INTERRUPT REQUEST REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	R/W-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0
	—	TXBUSE	RXBUSE	—	—	—	EWMARK	FWMARK
7:0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	RXDONE	PKTPEND	RXACT	—	TXDONE	TXABORT	RXBUFNA	RXOVFLW

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-15 **Unimplemented:** Read as '0'

bit 14 **TXBUSE:** Transmit BVC I Bus Error Interrupt bit⁽²⁾

1 = BVC I Bus Error has occurred

0 = BVC I Bus Error has not occurred

This bit is set when the TX DMA encounters a BVC I Bus error during a memory access. It is cleared by either a Reset or CPU write of a '1' to the CLR register.

bit 13 **RXBUSE:** Receive BVC I Bus Error Interrupt bit⁽²⁾

1 = BVC I Bus Error has occurred

0 = BVC I Bus Error has not occurred

This bit is set when the RX DMA encounters a BVC I Bus error during a memory access. It is cleared by either a Reset or CPU write of a '1' to the CLR register.

bit 12-10 **Unimplemented:** Read as '0'

bit 9 **EWMARK:** Empty Watermark Interrupt bit⁽²⁾

1 = Empty Watermark pointer reached

0 = No interrupt pending

This bit is set when the RX Descriptor Buffer Count is less than or equal to the value in the RXEWM bit (ETHRXWM<0:7>) value. It is cleared by BUFCNT bit (ETHSTAT<16:23>) being incremented by hardware. Writing a '0' or a '1' has no effect.

bit 8 **FWMARK:** Full Watermark Interrupt bit⁽²⁾

1 = Full Watermark pointer reached

0 = No interrupt pending

This bit is set when the RX Descriptor Buffer Count is greater than or equal to the value in the RXFWM bit (ETHRXWM<16:23>) field. It is cleared by writing the BUFCDEC (ETHCON1<0>) bit to decrement the BUFCNT counter. Writing a '0' or a '1' has no effect.

Note 1: This bit is only used for TX operations.

Note 2: This bit is are only used for RX operations.

Note: It is recommended to use the SET, CLR, or INV registers to set or clear any bit in this register. Setting or clearing any bits in this register should only be done for debug/test purposes.

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REGISTER 30-24: EMAC1CFG2: ETHERNET CONTROLLER MAC CONFIGURATION 2 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 25/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	RW-1	RW-0	RW-0	U-0	U-0	RW-0	RW-0
	—	EXCESS DFR	BPNBOK OFF	NOBK OFF	—	—	LONGPRE	PUREPRE
7:0	RW-1	RW-0	RW-1	RW-1	RW-0	RW-0	RW-1	RW-0
	AUTO PAD ^(1,2)	VLAN PAD ^(1,2)	PAD ENABLE ^(1,3)	CRC ENABLE	DELAYCRC	HUGEFRM	LENGTHCK	FULLDPLX

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-15 **Unimplemented:** Read as '0'

bit 14 **EXCESSDER:** Excess Defer bit

1 = The MAC will defer to carrier indefinitely as per the Standard

0 = The MAC will abort when the excessive deferral limit is reached

bit 13 **BPNBOKOFF:** Backpressure/No Backoff bit

1 = The MAC after incidentally causing a collision during backpressure will immediately retransmit without backoff reducing the chance of further collisions and ensuring transmit packets get sent

0 = The MAC will not remove the backoff

bit 12 **NOBKOFF:** No Backoff bit

1 = Following a collision, the MAC will immediately retransmit rather than using the Binary Exponential Backoff algorithm as specified in the Standard

0 = Following a collision, the MAC will use the Binary Exponential Backoff algorithm

bit 11-10 **Unimplemented:** Read as '0'

bit 9 **LONGPRE:** Long Preamble Enforcement bit

1 = The MAC only allows receive packets which contain preamble fields less than 12 bytes in length

0 = The MAC allows any length preamble as per the Standard

bit 8 **PUREPRE:** Pure Preamble Enforcement bit

1 = The MAC will verify the content of the preamble to ensure it contains 0x55 and is error-free. A packet with errors in its preamble is discarded

0 = The MAC does not perform any preamble checking

bit 7 **AUTOPAD:** Automatic Detect Pad Enable bit^(1,2)

1 = The MAC will automatically detect the type of frame, either tagged or untagged, by comparing the two octets following the source address with 0x8100 (VLAN Protocol ID) and pad accordingly

0 = The MAC does not perform automatic detection

Note 1: Table 30-6 provides a description of the pad function based on the configuration of this register.

2: This bit is ignored if the PADENABLE bit is cleared.

3: This bit is used in conjunction with the AUTOPAD and VLANPAD bits.

Note: Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware

REGISTER 34-4: DEVCFG1/ADEVCFG1: DEVICE CONFIGURATION WORD 1 (CONTINUED)

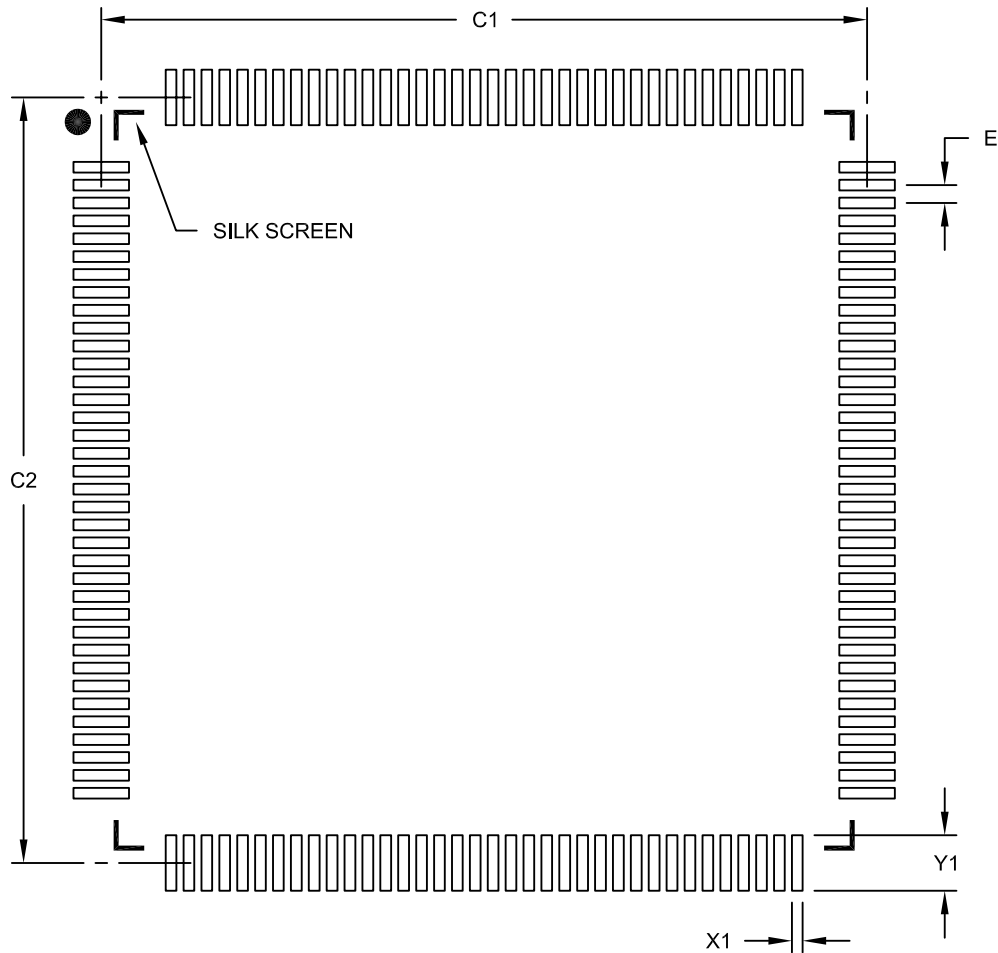
bit 2-0 **FNOSC<2:0>**: Oscillator Selection bits

- 111 = FRC divided by FRCDIV<2:0> bits (FRCDIV)
- 110 = Reserved
- 101 = LPRC
- 100 = Sosc
- 011 = Reserved
- 010 = Posc (HS, EC)
- 001 = SPLL
- 000 = FRC divided by FRCDIV<2:0> bits (FRCDIV)

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

144-Lead Plastic Low Profile Quad Flatpack (PL) - 20x20x1.40 mm Body [LQFP]
2.00 mm Footprint

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Units	Dimension Limits	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Contact Pad Spacing	C1		21.40	
Contact Pad Spacing	C2		21.40	
Contact Pad Width (X144)	X1			0.30
Contact Pad Length (X144)	Y1			1.55

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2044B