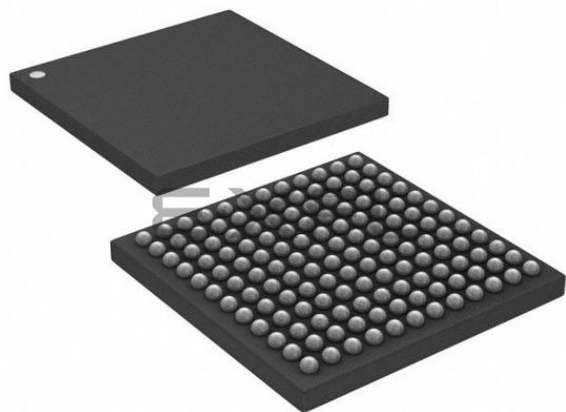




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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	MIPS32® M-Class
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, PMP, SPI, SQI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	120
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	2.1V ~ 3.6V
Data Converters	A/D 48x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-TFBGA
Supplier Device Package	144-TFBGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mz1024efk144-i-jwx

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

TABLE 1-4: OC1 THROUGH OC9 PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number				Pin Type	Buffer Type	Description
	64-pin QFN/ TQFP	100-pin TQFP	124-pin VTLA	144-pin TQFP/ LQFP			
Output Compare							
OC1	PPS	PPS	PPS	PPS	O	—	Output Compare Outputs 1-9
OC2	PPS	PPS	PPS	PPS	O	—	
OC3	PPS	PPS	PPS	PPS	O	—	
OC4	PPS	PPS	PPS	PPS	O	—	
OC5	PPS	PPS	PPS	PPS	O	—	
OC6	PPS	PPS	PPS	PPS	O	—	
OC7	PPS	PPS	PPS	PPS	O	—	
OC8	PPS	PPS	PPS	PPS	O	—	
OC9	PPS	PPS	PPS	PPS	O	—	
OCFA	PPS	PPS	PPS	PPS	I	ST	Output Compare Fault A Input
OCFB	30	44	B24	62	I	ST	Output Compare Fault B Input

Legend: CMOS = CMOS-compatible input or output
 ST = Schmitt Trigger input with CMOS levels
 TTL = Transistor-transistor Logic input buffer

Analog = Analog input
 O = Output
 PPS = Peripheral Pin Select

P = Power
 I = Input

TABLE 1-5: EXTERNAL INTERRUPTS PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number				Pin Type	Buffer Type	Description
	64-pin QFN/ TQFP	100-pin TQFP	124-pin VTLA	144-pin TQFP/ LQFP			
External Interrupts							
INT0	46	71	A48	104	I	ST	External Interrupt 0
INT1	PPS	PPS	PPS	PPS	I	ST	External Interrupt 1
INT2	PPS	PPS	PPS	PPS	I	ST	External Interrupt 2
INT3	PPS	PPS	PPS	PPS	I	ST	External Interrupt 3
INT4	PPS	PPS	PPS	PPS	I	ST	External Interrupt 4

Legend: CMOS = CMOS-compatible input or output
 ST = Schmitt Trigger input with CMOS levels
 TTL = Transistor-transistor Logic input buffer

Analog = Analog input
 O = Output
 PPS = Peripheral Pin Select

P = Power
 I = Input

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

TABLE 1-7: TIMER1 THROUGH TIMER9 AND RTCC PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number				Pin Type	Buffer Type	Description
	64-pin QFN/ TQFP	100-pin TQFP	124-pin VTLA	144-pin TQFP/ LQFP			
Timer1 through Timer9							
T1CK	48	73	A49	106	I	ST	Timer1 External Clock Input
T2CK	PPS	PPS	PPS	PPS	I	ST	Timer2 External Clock Input
T3CK	PPS	PPS	PPS	PPS	I	ST	Timer3 External Clock Input
T4CK	PPS	PPS	PPS	PPS	I	ST	Timer4 External Clock Input
T5CK	PPS	PPS	PPS	PPS	I	ST	Timer5 External Clock Input
T6CK	PPS	PPS	PPS	PPS	I	ST	Timer6 External Clock Input
T7CK	PPS	PPS	PPS	PPS	I	ST	Timer7 External Clock Input
T8CK	PPS	PPS	PPS	PPS	I	ST	Timer8 External Clock Input
T9CK	PPS	PPS	PPS	PPS	I	ST	Timer9 External Clock Input
Real-Time Clock and Calendar							
RTCC	46	71	A48	104	O	—	Real-Time Clock Alarm/Seconds Output

Legend: CMOS = CMOS-compatible input or output Analog = Analog input P = Power
ST = Schmitt Trigger input with CMOS levels O = Output I = Input
TTL = Transistor-transistor Logic input buffer PPS = Peripheral Pin Select

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

TABLE 1-8: UART1 THROUGH UART6 PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number				Pin Type	Buffer Type	Description
	64-pin QFN/ TQFP	100-pin TQFP	124-pin VTLA	144-pin TQFP/ LQFP			
Universal Asynchronous Receiver Transmitter 1							
U1RX	PPS	PPS	PPS	PPS	I	ST	UART1 Receive
U1TX	PPS	PPS	PPS	PPS	O	—	UART1 Transmit
U1CTS	PPS	PPS	PPS	PPS	I	ST	UART1 Clear to Send
U1RTS	PPS	PPS	PPS	PPS	O	—	UART1 Ready to Send
Universal Asynchronous Receiver Transmitter 2							
U2RX	PPS	PPS	PPS	PPS	I	ST	UART2 Receive
U2TX	PPS	PPS	PPS	PPS	O	—	UART2 Transmit
U2CTS	PPS	PPS	PPS	PPS	I	ST	UART2 Clear To Send
U2RTS	PPS	PPS	PPS	PPS	O	—	UART2 Ready To Send
Universal Asynchronous Receiver Transmitter 3							
U3RX	PPS	PPS	PPS	PPS	I	ST	UART3 Receive
U3TX	PPS	PPS	PPS	PPS	O	—	UART3 Transmit
U3CTS	PPS	PPS	PPS	PPS	I	ST	UART3 Clear to Send
U3RTS	PPS	PPS	PPS	PPS	O	—	UART3 Ready to Send
Universal Asynchronous Receiver Transmitter 4							
U4RX	PPS	PPS	PPS	PPS	I	ST	UART4 Receive
U4TX	PPS	PPS	PPS	PPS	O	—	UART4 Transmit
U4CTS	PPS	PPS	PPS	PPS	I	ST	UART4 Clear to Send
U4RTS	PPS	PPS	PPS	PPS	O	—	UART4 Ready to Send
Universal Asynchronous Receiver Transmitter 5							
U5RX	PPS	PPS	PPS	PPS	I	ST	UART5 Receive
U5TX	PPS	PPS	PPS	PPS	O	—	UART5 Transmit
U5CTS	PPS	PPS	PPS	PPS	I	ST	UART5 Clear to Send
U5RTS	PPS	PPS	PPS	PPS	O	—	UART5 Ready to Send
Universal Asynchronous Receiver Transmitter 6							
U6RX	PPS	PPS	PPS	PPS	I	ST	UART6 Receive
U6TX	PPS	PPS	PPS	PPS	O	—	UART6 Transmit
U6CTS	PPS	PPS	PPS	PPS	I	ST	UART6 Clear to Send
U6RTS	PPS	PPS	PPS	PPS	O	—	UART6 Ready to Send

Legend: CMOS = CMOS-compatible input or output
ST = Schmitt Trigger input with CMOS levels
TTL = Transistor-transistor Logic input buffer
Analog = Analog input
O = Output
PPS = Peripheral Pin Select
P = Power
I = Input

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

TABLE 1-13: EBI PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number				Pin Type	Buffer Type	Description
	64-pin QFN/TQFP	100-pin TQFP	124-pin VTLA	144-pin TQFP/LQFP			
EBIOE	—	9	A7	13	O	—	External Bus Interface Output Enable
EBIRDY1	—	60	B34	86	I	ST	External Bus Interface Ready Input
EBIRDY2	—	58	A39	84	I	ST	
EBIRDY3	—	57	B45	116	I	ST	
EBIRP	—	—	—	45	O	—	External Bus Interface Flash Reset Pin
EBIWE	—	8	B5	12	O	—	External Bus Interface Write Enable

Legend: CMOS = CMOS-compatible input or output
 ST = Schmitt Trigger input with CMOS levels
 TTL = Transistor-transistor Logic input buffer
 Analog = Analog input
 O = Output
 PPS = Peripheral Pin Select
 P = Power
 I = Input

The FPU implements a high-performance 7-stage pipeline:

- Decode, register read and unpack (FR stage)
- Multiply tree, double pumped for double (M1 stage)
- Multiply complete (M2 stage)
- Addition first step (A1 stage)
- Addition second and final step (A2 stage)
- Packing to IEEE format (FP stage)
- Register writeback (FW stage)

The FPU implements a bypass mechanism that allows the result of an operation to be forwarded directly to the instruction that needs it without having to write the result to the FPU register and then read it back.

Table 3-5 lists the Coprocessor 1 Registers for the FPU.

TABLE 3-5: FPU (CP1) REGISTERS

Register Number	Register Name	Function
0	FIR	Floating Point implementation register. Contains information that identifies the FPU.
25	FCCR	Floating Point condition codes register.
26	FEXR	Floating Point exceptions register.
28	FENR	Floating Point enables register.
31	FCSR	Floating Point Control and Status register.

3.2 Power Management

The processor core offers a number of power management features, including low-power design, active power management and power-down modes of operation. The core is a static design that supports slowing or halting the clocks, which reduces system power consumption during Idle periods.

3.2.1 INSTRUCTION-CONTROLLED POWER MANAGEMENT

The mechanism for invoking Power-Down mode is through execution of the WAIT instruction. For more information on power management, see **Section 33.0 “Power-Saving Features”**.

3.2.2 LOCAL CLOCK GATING

The majority of the power consumed by the processor core is in the clock tree and clocking registers. The PIC32MZ family makes extensive use of local gated-clocks to reduce this dynamic power consumption.

3.3 L1 Instruction and Data Caches

3.3.1 INSTRUCTION CACHE (I-CACHE)

The I-Cache is an on-core memory block of 16 Kbytes. Because the I-Cache is virtually indexed, the virtual-to-physical address translation occurs in parallel with the cache access rather than having to wait for the physical address translation. The tag holds 22 bits of physical address, a valid bit, and a lock bit. The LRU replacement bits are stored in a separate array.

The I-Cache block also contains and manages the instruction line fill buffer. Besides accumulating data to be written to the cache, instruction fetches that reference data in the line fill buffer are serviced either by a bypass of that data, or data coming from the external interface. The I-Cache control logic controls the bypass function.

The processor core supports I-Cache locking. Cache locking allows critical code or data segments to be locked into the cache on a per-line basis, enabling the system programmer to maximize the efficiency of the system cache.

The cache locking function is always available on all I-Cache entries. Entries can then be marked as locked or unlocked on a per entry basis using the CACHE instruction.

3.3.2 DATA CACHE (D-CACHE)

The D-Cache is an on-core memory block of 4 Kbytes. This virtually indexed, physically tagged cache is protected. Because the D-Cache is virtually indexed, the virtual-to-physical address translation occurs in parallel with the cache access. The tag holds 22 bits of physical address, a valid bit, and a lock bit. There is an additional array holding dirty bits and LRU replacement algorithm bits for each set of the cache.

In addition to I-Cache locking, the processor core also supports a D-Cache locking mechanism identical to the I-Cache. Critical data segments are locked into the cache on a per-line basis. The locked contents can be updated on a store hit, but cannot be selected for replacement on a cache miss.

The D-Cache locking function is always available on all D-Cache entries. Entries can then be marked as locked or unlocked on a per-entry basis using the CACHE instruction.

3.3.3 ATTRIBUTES

The processor core I-Cache and D-Cache attributes are listed in the Configuration registers (see Register 3-1 through Register 3-4).

The System Bus arbitration scheme implements a non-programmable, Least Recently Served (LRS) priority, which provides Quality Of Service (QOS) for most initiators. However, some initiators can use Fixed High Priority (HIGH) arbitration to guarantee their access to data.

The arbitration scheme for the available initiators is shown in Table 4-5.

TABLE 4-5: INITIATOR ID AND QOS

Name	ID	QOS
CPU	1	LRS ⁽¹⁾
CPU	2	HIGH ^(1,2)
DMA Read	3	LRS ⁽¹⁾
DMA Read	4	HIGH ^(1,2)
DMA Write	5	LRS ⁽¹⁾
DMA Write	6	HIGH ^(1,2)
USB	7	LRS
Ethernet Read	8	LRS
Ethernet Write	9	LRS
CAN1	10	LRS
CAN2	11	LRS
SQI1	12	LRS
Flash Controller	13	HIGH ⁽²⁾
Crypto	14	LRS

Note 1: When accessing SRAM, the DMAPRI bit (CFGCON<25>) and the CPUPRI bit (CFGCON<24>) provide arbitration control for the DMA and CPU (when servicing an interrupt (i.e., EXL = 1)), respectively, by selecting the use of LRS or HIGH. When using HIGH, the DMA and CPU get arbitration preference over all initiators using LRS.

- 2:** Using HIGH arbitration can have serious negative effects on other initiators. Therefore, it is recommended to not enable this type of arbitration for an initiator that uses significant system bandwidth. HIGH arbitration is intended to be used for low bandwidth applications that require low latency, such as LCC graphics applications.

4.3 Permission Access and System Bus Registers

The System Bus on PIC32MZ EF family of microcontrollers provides access control capabilities for the transaction initiators on the System Bus.

The System Bus divides the entire memory space into fourteen target regions and permits access to each target by initiators via permission groups. Four Permission Groups (0 through 3) can be assigned to each initiator. Each permission group is independent of the others and can have exclusive or shared access to a region.

Using the CFGPG register (see Register 34-10 in **Section 34.0 “Special Features”**), Boot firmware can assign a permission group to each initiator, which can make requests on the System Bus.

The available targets and their regions, as well as the associated control registers to assign protection, are described and listed in Table 4-6.

Register 4-2 through Register 4-10 are used for setting and controlling access permission groups and regions.

To change these registers, they must be unlocked in hardware. The register lock is controlled by the PGLOCK Configuration bit (CFGCON<11>). Setting PGLOCK prevents writes to the control registers; clearing PGLOCK allows writes.

To set or clear the PGLOCK bit, an unlock sequence must be executed. Refer to **Section 42. “Oscillators with Enhanced PLL”** in the *“PIC32 Family Reference Manual”* for details.

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

REGISTER 4-9: SBTxRDy: SYSTEM BUS TARGET 'x' REGION 'y' READ PERMISSIONS REGISTER ('x' = 0-13; 'y' = 0-8)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	R/W-0	R/W-1	R/W-1	R/W-1
	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

bit 31-4 **Unimplemented:** Read as '0'

bit 3 **Group3:** Group3 Read Permissions bits

1 = Privilege Group 3 has read permission

0 = Privilege Group 3 does not have read permission

bit 2 **Group2:** Group2 Read Permissions bits

1 = Privilege Group 2 has read permission

0 = Privilege Group 2 does not have read permission

bit 1 **Group1:** Group1 Read Permissions bits

1 = Privilege Group 1 has read permission

0 = Privilege Group 1 does not have read permission

bit 0 **Group0:** Group0 Read Permissions bits

1 = Privilege Group 0 has read permission

0 = Privilege Group 0 does not have read permission

Note 1: Refer to Table 4-6 for the list of available targets and their descriptions.

2: For some target regions, certain bits in this register are read-only with preset values. See Table 4-6 for more information.

TABLE 7-2: INTERRUPT IRQ, VECTOR, AND BIT LOCATION (CONTINUED)

Interrupt Source ⁽¹⁾	XC32 Vector Name	IRQ #	Vector #	Interrupt Bit Location				Persistent Interrupt
				Flag	Enable	Priority	Sub-priority	
ADC Data 19 ⁽²⁾	_ADC_DATA19_VECTOR	78	OFF078<17:1>	IFS2<14>	IEC2<14>	IPC19<20:18>	IPC19<17:16>	Yes
ADC Data 20 ⁽²⁾	_ADC_DATA20_VECTOR	79	OFF079<17:1>	IFS2<15>	IEC2<15>	IPC19<28:26>	IPC19<25:24>	Yes
ADC Data 21 ⁽²⁾	_ADC_DATA21_VECTOR	80	OFF080<17:1>	IFS2<16>	IEC2<16>	IPC20<4:2>	IPC20<1:0>	Yes
ADC Data 22 ⁽²⁾	_ADC_DATA22_VECTOR	81	OFF081<17:1>	IFS2<17>	IEC2<17>	IPC20<12:10>	IPC20<9:8>	Yes
ADC Data 23 ⁽²⁾	_ADC_DATA23_VECTOR	82	OFF082<17:1>	IFS2<18>	IEC2<18>	IPC20<20:18>	IPC20<17:16>	Yes
ADC Data 24 ⁽²⁾	_ADC_DATA24_VECTOR	83	OFF083<17:1>	IFS2<19>	IEC2<19>	IPC20<28:26>	IPC20<25:24>	Yes
ADC Data 25 ⁽²⁾	_ADC_DATA25_VECTOR	84	OFF084<17:1>	IFS2<20>	IEC2<20>	IPC21<4:2>	IPC21<1:0>	Yes
ADC Data 26 ⁽²⁾	_ADC_DATA26_VECTOR	85	OFF085<17:1>	IFS2<21>	IEC2<21>	IPC21<12:10>	IPC21<9:8>	Yes
ADC Data 27 ⁽²⁾	_ADC_DATA27_VECTOR	86	OFF086<17:1>	IFS2<22>	IEC2<22>	IPC21<20:18>	IPC21<17:16>	Yes
ADC Data 28 ⁽²⁾	_ADC_DATA28_VECTOR	87	OFF087<17:1>	IFS2<23>	IEC2<23>	IPC21<28:26>	IPC21<25:24>	Yes
ADC Data 29 ⁽²⁾	_ADC_DATA29_VECTOR	88	OFF088<17:1>	IFS2<24>	IEC2<24>	IPC22<4:2>	IPC22<1:0>	Yes
ADC Data 30 ⁽²⁾	_ADC_DATA30_VECTOR	89	OFF089<17:1>	IFS2<25>	IEC2<25>	IPC22<12:10>	IPC22<9:8>	Yes
ADC Data 31 ⁽²⁾	_ADC_DATA31_VECTOR	90	OFF090<17:1>	IFS2<26>	IEC2<26>	IPC22<20:18>	IPC22<17:16>	Yes
ADC Data 32 ⁽²⁾	_ADC_DATA32_VECTOR	91	OFF091<17:1>	IFS2<27>	IEC2<27>	IPC22<28:26>	IPC22<25:24>	Yes
ADC Data 33 ⁽²⁾	_ADC_DATA33_VECTOR	92	OFF092<17:1>	IFS2<28>	IEC2<28>	IPC23<4:2>	IPC23<1:0>	Yes
ADC Data 34 ⁽²⁾	_ADC_DATA34_VECTOR	93	OFF093<17:1>	IFS2<29>	IEC2<29>	IPC23<12:10>	IPC23<9:8>	Yes
ADC Data 35 ^(2,3)	_ADC_DATA35_VECTOR	94	OFF094<17:1>	IFS2<30>	IEC2<30>	IPC23<20:18>	IPC23<17:16>	Yes
ADC Data 36 ^(2,3)	_ADC_DATA36_VECTOR	95	OFF095<17:1>	IFS2<31>	IEC2<31>	IPC23<28:26>	IPC23<25:24>	Yes
ADC Data 37 ^(2,3)	_ADC_DATA37_VECTOR	96	OFF096<17:1>	IFS3<0>	IEC3<0>	IPC24<4:2>	IPC24<1:0>	Yes
ADC Data 38 ^(2,3)	_ADC_DATA38_VECTOR	97	OFF097<17:1>	IFS3<1>	IEC3<1>	IPC24<12:10>	IPC24<9:8>	Yes
ADC Data 39 ^(2,3)	_ADC_DATA39_VECTOR	98	OFF098<17:1>	IFS3<2>	IEC3<2>	IPC24<20:18>	IPC24<17:16>	Yes
ADC Data 40 ^(2,3)	_ADC_DATA40_VECTOR	99	OFF099<17:1>	IFS3<3>	IEC3<3>	IPC24<28:26>	IPC24<25:24>	Yes
ADC Data 41 ^(2,3)	_ADC_DATA41_VECTOR	100	OFF100<17:1>	IFS3<4>	IEC3<4>	IPC25<4:2>	IPC25<1:0>	Yes
ADC Data 42 ^(2,3)	_ADC_DATA42_VECTOR	101	OFF101<17:1>	IFS3<5>	IEC3<5>	IPC25<12:10>	IPC25<9:8>	Yes
ADC Data 43	_ADC_DATA43_VECTOR	102	OFF102<17:1>	IFS3<6>	IEC3<6>	IPC25<20:18>	IPC25<17:16>	Yes
ADC Data 44	_ADC_DATA44_VECTOR	103	OFF103<17:1>	IFS3<7>	IEC3<7>	IPC25<28:26>	IPC25<25:24>	Yes
Core Performance Counter Interrupt	_CORE_PERF_COUNT_VECTOR	104	OFF104<17:1>	IFS3<8>	IEC3<8>	IPC26<4:2>	IPC26<1:0>	No
Core Fast Debug Channel Interrupt	_CORE_FAST_DEBUG_CHAN_VECTOR	105	OFF105<17:1>	IFS3<9>	IEC3<9>	IPC26<12:10>	IPC26<9:8>	Yes

Note 1: Not all interrupt sources are available on all devices. See **TABLE 1: "PIC32MZ EF Family Features"** for the list of available peripherals.

Note 2: This interrupt source is not available on 64-pin devices.

Note 3: This interrupt source is not available on 100-pin devices.

Note 4: This interrupt source is not available on 124-pin devices.

TABLE 7-3: INTERRUPT REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name ⁽¹⁾	Bit Range	Bits																All Resets		
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0			
03D0	IPC41	31:16	—	—	—	FCEIP<2:0>			FCEIS<1:0>			—	—	—	RTCCIP<2:0>			RTCCIS<1:0>		0000	
		15:0	—	—	—	SPI4TXIP<2:0>			SPI4TXIS<1:0>			—	—	—	SPI4RXIP<2:0>			SPI4RXIS<1:0>		0000	
03E0	IPC42	31:16	—	—	—	U4RXIP<2:0>			U4RXIS<1:0>			—	—	—	U4EIP<2:0>			U4EIS<1:0>		0000	
		15:0	—	—	—	SQI1IP<2:0>			SQI1IS<1:0>			—	—	—	PREIP<2:0>			PREIS<1:0>		0000	
03F0	IPC43	31:16	—	—	—	I2C4MIP<2:0>			I2C4MIS<1:0>			—	—	—	I2C4SIP<2:0>			I2C4SIS<1:0>		0000	
		15:0	—	—	—	I2C4BIP<2:0>			I2C4BIS<1:0>			—	—	—	U4TXIP<2:0>			U4TXIS<1:0>		0000	
0400	IPC44	31:16	—	—	—	U5EIP<2:0>			U5EIS<1:0>			—	—	—	SPI5TXIP<2:0> ⁽²⁾			SPI5TXIS<1:0> ⁽²⁾		0000	
		15:0	—	—	—	SPI5RXIP<2:0> ⁽²⁾			SPI5RXIS<1:0> ⁽²⁾			—	—	—	SPI5EIP<2:0> ⁽²⁾			SPI5EIS<1:0> ⁽²⁾		0000	
0410	IPC45	31:16	—	—	—	I2C5SIP<2:0>			I2C5SIS<1:0>			—	—	—	I2C5BIP<2:0>			I2C5BIS<1:0>		0000	
		15:0	—	—	—	U5TXIP<2:0>			U5TXIS<1:0>			—	—	—	U5RXIP<2:0>			U5RXIS<1:0>		0000	
0420	IPC46	31:16	—	—	—	SPI6TXIP<2:0> ⁽²⁾			SPI6TXIS<1:0> ⁽²⁾			—	—	—	SPI6RXIP<2:0> ⁽²⁾			SPI6RXIS<1:0> ⁽²⁾		0000	
		15:0	—	—	—	SPI6EIP<2:0> ⁽²⁾			SPI6EIS<1:0> ⁽²⁾			—	—	—	I2C5MIP<2:0>			I2C5MIS<1:0>		0000	
0430	IPC47	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	U6TXIP<2:0>		U6TXIS<1:0>		0000
		15:0	—	—	—	U6RXIP<2:0>			U6RXIS<1:0>			—	—	—	U6EIP<2:0>			U6EIS<1:0>		0000	
0440	IPC48	31:16	—	—	—	—	—	—	—	—	—	—	—	—	ADCURDYP<2:0>			ADCURDYIS<1:0>		0000	
		15:0	—	—	—	ADCARDYP<2:0>			ADCARDYIS<1:0>			—	—	—	ADCEOSIP<2:0>			ADCEOSIS<1:0>		0000	
0450	IPC49	31:16	—	—	—	ADC1EIP<2:0>			ADC1EIS<1:0>			—	—	—	ADC0EIP<2:0>			ADC0EIS<1:0>		0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	ADCGRPIP<2:0>			ADCGRPIS<1:0>		0000		
0460	IPC50	31:16	—	—	—	—	—	—	—	—	—	—	—	—	ADC4EIP<2:0>			ADC4EIS<1:0>		0000	
		15:0	—	—	—	ADC3EIP<2:0>			ADC3EIS<1:0>			—	—	—	ADC2EIP<2:0>			ADC2EIS<1:0>		0000	
0470	IPC51	31:16	—	—	—	ADC1WIP<2:0>			ADC1WIS<1:0>			—	—	—	ADC0WIP<2:0>			ADC0WIS<1:0>		0000	
		15:0	—	—	—	ADC7EIP<2:0>			ADC7EIS<1:0>			—	—	—	—	—	—	—	—	0000	
0480	IPC52	31:16	—	—	—	—	—	—	—	—	—	—	—	—	ADC4WIP<2:0>			ADC4WIS<1:0>		0000	
		15:0	—	—	—	ADC3WIP<2:0>			ADC3WIS<1:0>			—	—	—	ADC2WIP<2:0>			ADC2WIS<1:0>		0000	
0490	IPC53	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	ADC7WIP<2:0>			ADC7WIS<1:0>			—	—	—	—	—	—	—	—	0000	
0540	OFF000	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>			0000	
		15:0	VOFF<15:1>																—	0000	
0544	OFF001	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>			0000	
		15:0	VOFF<15:1>																—	0000	

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

- Note** 1: All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 “CLR, SET, and INV Registers”** for more information.
- 2: This bit or register is not available on 64-pin devices.
- 3: This bit or register is not available on devices without a CAN module.
- 4: This bit or register is not available on 100-pin devices.
- 5: Bits 31 and 30 are not available on 64-pin and 100-pin devices; bits 29 through 14 are not available on 64-pin devices.
- 6: Bits 31, 30, 29, and bits 5 through 0 are not available on 64-pin and 100-pin devices; bit 31 is not available on 124-pin devices; bit 22 is not available on 64-pin devices.
- 7: This bit or register is not available on devices without a Crypto module.
- 8: This bit or register is not available on 124-pin devices.

TABLE 10-3: DMA CHANNEL 0 THROUGH CHANNEL 7 REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name ⁽¹⁾	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
14A0	DCH5DPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDPTR<15:0>																0000
14B0	DCH5CSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCSIZ<15:0>																0000
14C0	DCH5CPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCPTR<15:0>																0000
14D0	DCH5DAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHPDAT<15:0>																0000
14E0	DCH6CON	31:16	CHPIGN<7:0>								—	—	—	—	—	—	—	—	0000
		15:0	CHBUSY	—	CHPIGNEN	—	CHPATLEN	—	—	—	CHCHNS	CHEN	CHAED	CHCHN	CHAEN	—	CHEDET	CHPRI<1:0>	0000
14F0	DCH6ECON	31:16	—	—	—	—	—	—	—	—	CHAIRQ<7:0>								00FF
		15:0	CHSIRQ<7:0>								CFORCE	CABORT	PATEN	SIRQEN	AIRQEN	—	—	—	FF00
1500	DCH6INT	31:16	—	—	—	—	—	—	—	—	CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE	CHERIE	0000
		15:0	—	—	—	—	—	—	—	—	CHSDIF	CHSHIF	CHDDIF	CHDHIF	CHBCIF	CHCCIF	CHTAIF	CHERIF	0000
1510	DCH6SSA	31:16	CHSSA<31:0>																0000
		15:0	CHSSA<31:0>																0000
1520	DCH6DSA	31:16	CHDSA<31:0>																0000
		15:0	CHDSA<31:0>																0000
1530	DCH6SSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSSIZ<15:0>																0000
1540	DCH6DSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDSIZ<15:0>																0000
1550	DCH6SPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSPTR<15:0>																0000
1560	DCH6DPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDPTR<15:0>																0000
1570	DCH6CSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCSIZ<15:0>																0000
1580	DCH6CPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCPTR<15:0>																0000
1590	DCH6DAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHPDAT<15:0>																0000
15A0	DCH7CON	31:16	CHPIGN<7:0>								—	—	—	—	—	—	—	—	0000
		15:0	CHBUSY	—	CHPIGNEN	—	CHPATLEN	—	—	—	CHCHNS	CHEN	CHAED	CHCHN	CHAEN	—	CHEDET	CHPRI<1:0>	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 12.3 "CLR, SET, and INV Registers" for more information.

12.2 Registers for Slew Rate Control

Some I/O pins can be configured for various types of slew rate control on its associated port. This is controlled by the Slew Rate Control bits in the SRCON1x and SRCON0x registers that are associated with each I/O port. The slew rate control is configured using the corresponding bit in each register, as shown in Table 12-1.

As an example, writing 0x0001, 0x0000 to SRCON1A and SRCON0A, respectively, will enable slew rate control on the RA0 pin and sets the slew rate to the slow edge rate.

TABLE 12-1: SLEW RATE CONTROL BIT SETTINGS

SRCON1x	SRCON0x	Description
1	1	Slew rate control is enabled and is set to the slowest edge rate.
1	0	Slew rate control is enabled and is set to the slow edge rate.
0	1	Slew rate control is enabled and is set to the medium edge rate.
0	0	Slew rate control is disabled and is set to the fastest edge rate.

Note: By default, all of the Port pins are set to the fastest edge rate.

12.3 CLR, SET, and INV Registers

Every I/O module register has a corresponding CLR (clear), SET (set) and INV (invert) register designed to provide fast atomic bit manipulations. As the name of the register implies, a value written to a SET, CLR or INV register effectively performs the implied operation, but only on the corresponding base register and only bits specified as '1' are modified. Bits specified as '0' are not modified.

Reading SET, CLR and INV registers returns undefined values. To see the affects of a write operation to a SET, CLR or INV register, the base register must be read.

12.4 Peripheral Pin Select (PPS)

A major challenge in general purpose devices is providing the largest possible set of peripheral features while minimizing the conflict of features on I/O pins. The challenge is even greater on low pin-count devices. In an application where more than one peripheral needs to be assigned to a single pin, inconvenient workarounds in application code or a complete redesign may be the only option.

PPS configuration provides an alternative to these choices by enabling peripheral set selection and their placement on a wide range of I/O pins. By increasing the pinout options available on a particular device, users can better tailor the device to their entire application, rather than trimming the application to fit the device.

The PPS configuration feature operates over a fixed subset of digital I/O pins. Users may independently map the input and/or output of most digital peripherals to these I/O pins. PPS is performed in software and generally does not require the device to be reprogrammed. Hardware safeguards are included that prevent accidental or spurious changes to the peripheral mapping once it has been established.

12.4.1 AVAILABLE PINS

The number of available pins is dependent on the particular device and its pin count. Pins that support the PPS feature include the designation "RPn" in their full pin designation, where "RP" designates a remappable peripheral and "n" is the remappable port number.

12.4.2 AVAILABLE PERIPHERALS

The peripherals managed by the PPS are all digital-only peripherals. These include general serial communications (UART, SPI, and CAN), general purpose timer clock inputs, timer-related peripherals (input capture and output compare), interrupt-on-change inputs, and reference clocks (input and output).

In comparison, some digital-only peripheral modules are never included in the PPS feature. This is because the peripheral's function requires special I/O circuitry on a specific port and cannot be easily connected to multiple pins. These modules include I²C among others. A similar requirement excludes all modules with analog inputs, such as the Analog-to-Digital Converter (ADC).

A key difference between remappable and non-remappable peripherals is that remappable peripherals are not associated with a default I/O pin. The peripheral must always be assigned to a specific I/O pin before it can be used. In contrast, non-remappable peripherals are always available on a default pin, assuming that the peripheral is active and not conflicting with another peripheral.

When a remappable peripheral is active on a given I/O pin, it takes priority over all other digital I/O and digital communication peripherals associated with the pin. Priority is given regardless of the type of peripheral that is mapped. Remappable peripherals never take priority over any analog functions associated with the pin.

12.5 I/O Ports Control Registers

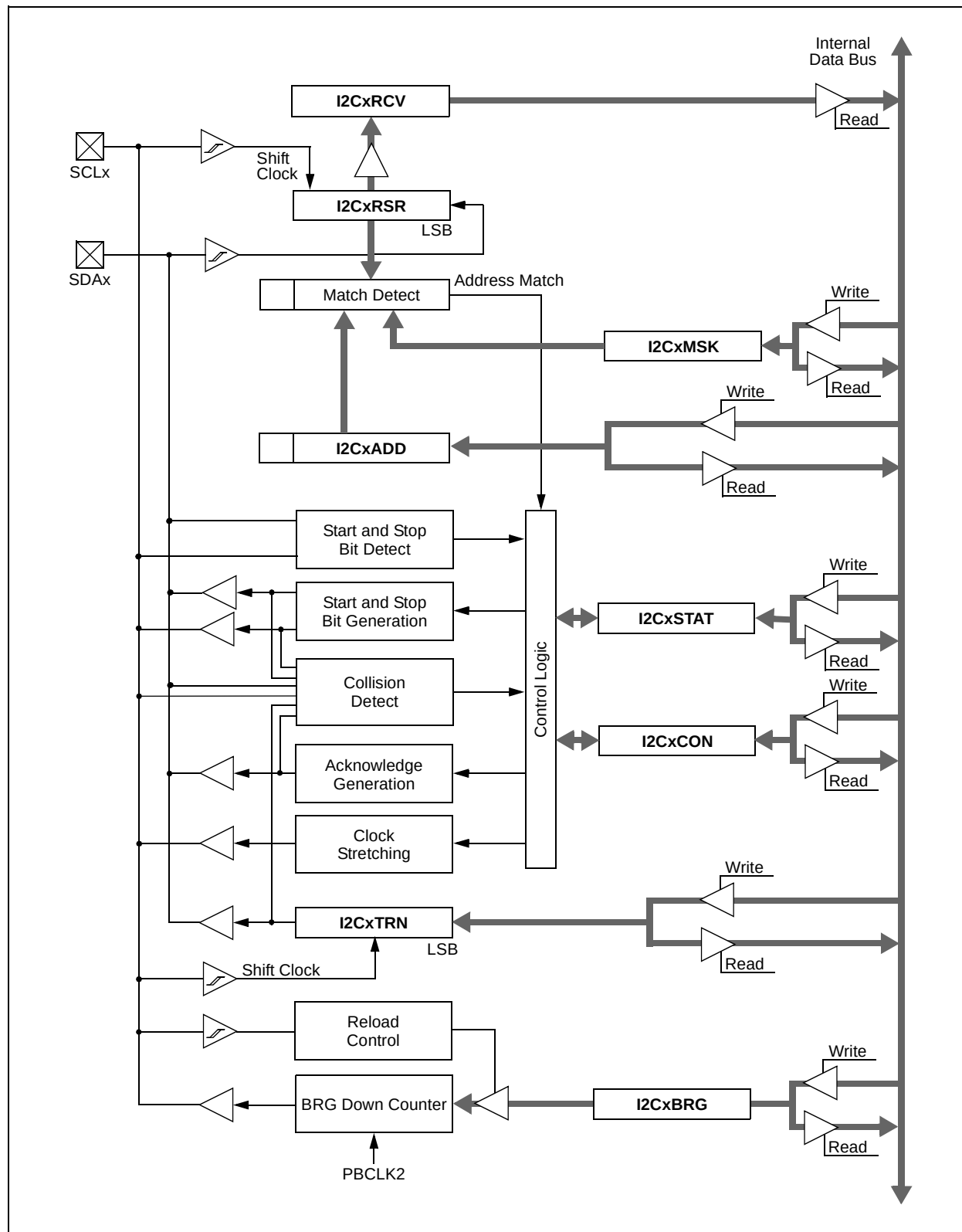
TABLE 12-4: PORTA REGISTER MAP FOR 100-PIN, 124-PIN, AND 144-PIN DEVICES ONLY

Virtual Address (BF86..#)	Register Name ⁽¹⁾	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0000	ANSELA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	ANSA10	ANSA9	—	—	—	ANSA5	—	—	—	ANSA1	ANSA0	0623
0010	TRISA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRISA15	TRISA14	—	—	—	TRISA10	TRISA9	—	TRISA7	TRISA6	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	C6FF
0020	PORTA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RA15	RA14	—	—	—	RA10	RA9	—	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	xxxx
0030	LATA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	LATA15	LATA14	—	—	—	LATA10	LATA9	—	LATA7	LATA6	LATA5	LATA4	LATA3	LATA2	LATA1	LATA0	xxxx
0040	ODCA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ODCA15	ODCA14	—	—	—	ODCA10	ODCA9	—	ODCA7	ODCA6	ODCA5	ODCA4	ODCA3	ODCA2	ODCA1	ODCA0	0000
0050	CNPUA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPUA15	CNPUA14	—	—	—	CNPUA10	CNPUA9	—	CNPUA7	CNPUA6	CNPUA5	CNPUA4	CNPUA3	CNPUA2	CNPUA1	CNPUA0	0000
0060	CNPDA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPDA15	CNPDA14	—	—	—	CNPDA10	CNPDA9	—	CNPDA7	CNPDA6	CNPDA5	CNPDA4	CNPDA3	CNPDA2	CNPDA1	CNPDA0	0000
0070	CNCONA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	EDGEDETECT	—	—	—	—	—	—	—	—	—	—	—	0000
0080	CNENA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNENA15	CNENA14	—	—	—	CNENA10	CNENA9	—	CNENA7	CNENA6	CNENA5	CNENA4	CNENA3	CNENA2	CNENA1	CNENA0	0000
0090	CNSTATA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CN STATA15	CN STATA14	—	—	—	CN STATA10	CN STATA9	—	CN STATA7	CN STATA6	CN STATA5	CN STATA4	CN STATA3	CN STATA2	CN STATA1	CN STATA0	0000
00A0	CNNEA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNNEA15	CNNEA14	—	—	—	CNNEA10	CNNEA9	—	CNNEA7	CNNEA6	CNNEA5	CNNEA4	CNNEA3	CNNEA2	CNNEA1	CNNEA0	0000
00B0	CNFA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNFA15	CNFA14	—	—	—	CNFA10	CNFA9	—	CNFA7	CNFA6	CNFA5	CNFA4	CNFA3	CNFA2	CNFA1	CNFA0	0000
00C0	SRCON0A	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	SR0A7	SR0A6	—	—	—	—	—	—	0000
00D0	SRCON1A	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	SR1A7	SR0A6	—	—	—	—	—	—	0000

Legend: x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 “CLR, SET, and INV Registers”** for more information.

FIGURE 21-1: I²C BLOCK DIAGRAM



28.1 ADC Control Registers

TABLE 28-1: ADC REGISTER MAP

Virtual Address (BF84_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
B000	ADCCON1	31:16	TRBEN	TRBERR	TRBMST<2:0>			TRBSLV<2:0>			FRACT	SELRES<1:0>			STRGSRC<4:0>				0060
		15:0	ON	—	SIDL	AICMPEN	CVDEN	FSSCLKEN	FSPBCLKEN	—	—	IRQVS<2:0>			STRGLVL	—	—	—	1000
B004	ADCCON2	31:16	BGVRRDY	REFFLT	EOSRDY	CVDCLP<2:0>			SAMC<9:0>										0000
		15:0	BGVRIEN	REFFLTEN	EOSIEN	ADCEIOVR	—	ADCEIS<2:0>			—	ADCCDIV<6:0>						0000	
B008	ADCCON3	31:16	ADCSEL<1:0>		CONCLKDIV<5:0>					DIGEN7	—	—	—	DIGEN4	DIGEN3	DIGEN2	DIGEN1	DIGEN0	0000
		15:0	VREFSEL<2:0>			TRGSUSP	UPDIEN	UPDRDY	SAMP	RQCNVRT	GLSWTRG	GSWTRG	ADINSEL<5:0>						
B00C	ADCTRGMODE	31:16	—	—	—	—	—	—	SH4ALT<1:0>		SH3ALT<1:0>		SH2ALT<1:0>		SH1ALT<1:0>		SH0ALT<1:0>		0000
		15:0	—	—	—	STRGEN4	STRGEN3	STRGEN2	STRGEN1	STRGEN0	—	—	—	SSAMPEN4	SSAMPEN3	SSAMPEN2	SSAMPEN1	SSAMPEN0	0000
B010	ADCIMCON1	31:16	DIFF15	SIGN15	DIFF14	SIGN14	DIFF13	SIGN13	DIFF12	SIGN12	DIFF11	SIGN11	DIFF10	SIGN10	DIFF9	SIGN9	DIFF8	SIGN8	0000
		15:0	DIFF7	SIGN7	DIFF6	SIGN6	DIFF5	SIGN5	DIFF4	SIGN4	DIFF3	SIGN3	DIFF2	SIGN2	DIFF1	SIGN1	DIFF0	SIGN0	0000
B014	ADCIMCON2	31:16	DIFF31 ⁽¹⁾	SIGN31 ⁽¹⁾	DIFF30 ⁽¹⁾	SIGN30 ⁽¹⁾	DIFF29 ⁽¹⁾	SIGN29 ⁽¹⁾	DIFF28 ⁽¹⁾	SIGN28 ⁽¹⁾	DIFF27 ⁽¹⁾	SIGN27 ⁽¹⁾	DIFF26 ⁽¹⁾	SIGN26 ⁽¹⁾	DIFF25 ⁽¹⁾	SIGN25 ⁽¹⁾	DIFF24 ⁽¹⁾	SIGN24 ⁽¹⁾	0000
		15:0	DIFF23 ⁽¹⁾	SIGN23 ⁽¹⁾	DIFF22 ⁽¹⁾	SIGN22 ⁽¹⁾	DIFF21 ⁽¹⁾	SIGN21 ⁽¹⁾	DIFF20 ⁽¹⁾	SIGN20 ⁽¹⁾	DIFF19 ⁽¹⁾	SIGN19 ⁽¹⁾	DIFF18	SIGN18	DIFF17	SIGN17	DIFF16	SIGN16	0000
B018	ADCIMCON3	31:16	—	—	—	—	—	—	DIFF44	SIGN44	DIFF43	SIGN43	DIFF42 ⁽²⁾	SIGN42 ⁽²⁾	DIFF41 ⁽²⁾	SIGN41 ⁽²⁾	DIFF40 ⁽²⁾	SIGN40 ⁽²⁾	0000
		15:0	DIFF39 ⁽²⁾	SIGN39 ⁽²⁾	DIFF38 ⁽²⁾	SIGN38 ⁽²⁾	DIFF37 ⁽²⁾	SIGN37 ⁽²⁾	DIFF36 ⁽²⁾	SIGN36 ⁽²⁾	DIFF35 ⁽²⁾	SIGN35 ⁽²⁾	DIFF34 ⁽¹⁾	SIGN34 ⁽¹⁾	DIFF33 ⁽¹⁾	SIGN33 ⁽¹⁾	DIFF32 ⁽¹⁾	SIGN32 ⁽¹⁾	0000
B020	ADCGIRQEN1	31:16	AGIEN31 ⁽¹⁾	AGIEN30 ⁽¹⁾	AGIEN29 ⁽¹⁾	AGIEN28 ⁽¹⁾	AGIEN27 ⁽¹⁾	AGIEN26 ⁽¹⁾	AGIEN25 ⁽¹⁾	AGIEN24 ⁽¹⁾	AGIEN23 ⁽¹⁾	AGIEN22 ⁽¹⁾	AGIEN21 ⁽¹⁾	AGIEN20 ⁽¹⁾	AGIEN19 ⁽¹⁾	AGIEN18	AGIEN17	AGIEN16	0000
		15:0	AGIEN15	AGIEN14	AGIEN13	AGIEN12	AGIEN11	AGIEN10	AGIEN9	AGIEN8	AGIEN7	AGIEN6	AGIEN5	AGIEN4	AGIEN3	AGIEN2	AGIEN1	AGIEN0	0000
B024	ADCGIRQEN2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	AGIEN44	AGIEN43	AGIEN42 ⁽²⁾	AGIEN41 ⁽²⁾	AGIEN40 ⁽²⁾	AGIEN39 ⁽²⁾	AGIEN38 ⁽²⁾	AGIEN37 ⁽²⁾	AGIEN36 ⁽²⁾	AGIEN35 ⁽²⁾	AGIEN34 ⁽¹⁾	AGIEN33 ⁽¹⁾	AGIEN32 ⁽¹⁾	0000
B028	ADCCSS1	31:16	CSS31 ⁽¹⁾	CSS30 ⁽¹⁾	CSS29 ⁽¹⁾	CSS28 ⁽¹⁾	CSS27 ⁽¹⁾	CSS26 ⁽¹⁾	CSS25 ⁽¹⁾	CSS24 ⁽¹⁾	CSS23 ⁽¹⁾	CSS22 ⁽¹⁾	CSS21 ⁽¹⁾	CSS20 ⁽¹⁾	CSS19 ⁽¹⁾	CSS18	CSS17	CSS16	0000
		15:0	CSS15	CSS14	CSS13	CSS12	CSS11	CSS10	CSS9	CSS8	CSS7	CSS6	CSS5	CSS4	CSS3	CSS2	CSS1	CSS0	0000
B02C	ADCCSS2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	CSS44	CSS43	CSS42 ⁽²⁾	CSS41 ⁽²⁾	CSS40 ⁽²⁾	CSS39 ⁽²⁾	CSS38 ⁽²⁾	CSS37 ⁽²⁾	CSS36 ⁽²⁾	CSS35 ⁽²⁾	CSS34 ⁽¹⁾	CSS33 ⁽¹⁾	CSS32 ⁽¹⁾	0000
B030	ADCDSTAT1	31:16	ARDY31 ⁽¹⁾	ARDY30 ⁽¹⁾	ARDY29 ⁽¹⁾	ARDY28 ⁽¹⁾	ARDY27 ⁽¹⁾	ARDY26 ⁽¹⁾	ARDY25 ⁽¹⁾	ARDY24 ⁽¹⁾	ARDY23 ⁽¹⁾	ARDY22 ⁽¹⁾	ARDY21 ⁽¹⁾	ARDY20 ⁽¹⁾	ARDY19 ⁽¹⁾	ARDY18	ARDY17	ARDY16	0000
		15:0	ARDY15	ARDY14	ARDY13	ARDY12	ARDY11	ARDY10	ARDY9	ARDY8	ARDY7	ARDY6	ARDY5	ARDY4	ARDY3	ARDY2	ARDY1	ARDY0	0000
B034	ADCDSTAT2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	ARDY44	ARDY43	ARDY42 ⁽²⁾	ARDY41 ⁽²⁾	ARDY40 ⁽²⁾	ARDY39 ⁽²⁾	ARDY38 ⁽²⁾	ARDY37 ⁽²⁾	ARDY36 ⁽²⁾	ARDY35 ⁽²⁾	ARDY34 ⁽¹⁾	ARDY33 ⁽¹⁾	ARDY32 ⁽¹⁾	0000
B038	ADCCMPEN1	31:16	CMPE31 ⁽¹⁾	CMPE30 ⁽¹⁾	CMPE29 ⁽¹⁾	CMPE28 ⁽¹⁾	CMPE27 ⁽¹⁾	CMPE26 ⁽¹⁾	CMPE25 ⁽¹⁾	CMPE24 ⁽¹⁾	CMPE23 ⁽¹⁾	CMPE22 ⁽¹⁾	CMPE21 ⁽¹⁾	CMPE20 ⁽¹⁾	CMPE19 ⁽¹⁾	CMPE18	CMPE17	CMPE16	0000
		15:0	CMPE15	CMPE14	CMPE13	CMPE12	CMPE11	CMPE10	CMPE9	CMPE8	CMPE7	CMPE6	CMPE5	CMPE4	CMPE3	CMPE2	CMPE1	CMPE0	0000
B03C	ADCCMP1	31:16	DCMPHI<15:0>																0000
		15:0	DCMPLO<15:0>																0000
B040	ADCCMPEN2	31:16	CMPE31 ⁽¹⁾	CMPE30 ⁽¹⁾	CMPE29 ⁽¹⁾	CMPE28 ⁽¹⁾	CMPE27 ⁽¹⁾	CMPE26 ⁽¹⁾	CMPE25 ⁽¹⁾	CMPE24 ⁽¹⁾	CMPE23 ⁽¹⁾	CMPE22 ⁽¹⁾	CMPE21 ⁽¹⁾	CMPE20 ⁽¹⁾	CMPE19 ⁽¹⁾	CMPE18	CMPE17	CMPE16	0000
		15:0	CMPE15	CMPE14	CMPE13	CMPE12	CMPE11	CMPE10	CMPE9	CMPE8	CMPE7	CMPE6	CMPE5	CMPE4	CMPE3	CMPE2	CMPE1	CMPE0	0000
B044	ADCCMP2	31:16	DCMPHI<15:0>																0000
		15:0	DCMPLO<15:0>																0000
B048	ADCCMPEN3	31:16	CMPE31 ⁽¹⁾	CMPE30 ⁽¹⁾	CMPE29 ⁽¹⁾	CMPE28 ⁽¹⁾	CMPE27 ⁽¹⁾	CMPE26 ⁽¹⁾	CMPE25 ⁽¹⁾	CMPE24 ⁽¹⁾	CMPE23 ⁽¹⁾	CMPE22 ⁽¹⁾	CMPE21 ⁽¹⁾	CMPE20 ⁽¹⁾	CMPE19 ⁽¹⁾	CMPE18	CMPE17	CMPE16	0000
		15:0	CMPE15	CMPE14	CMPE13	CMPE12	CMPE11	CMPE10	CMPE9	CMPE8	CMPE7	CMPE6	CMPE5	CMPE4	CMPE3	CMPE2	CMPE1	CMPE0	0000

Note

- 1: This bit or register is not available on 64-pin devices.
- 2: This bit or register is not available on 64-pin and 100-pin devices.
- 3: Before enabling the ADC, the user application must initialize the ADC calibration values by copying them from the factory-programmed DEVADCx Flash registers into the corresponding ADCxCFG registers.

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REGISTER 28-1: ADCCON1: ADC CONTROL REGISTER 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0 TRBEN	R-0, HS, HC TRBERR	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			TRBMST<2:0>			TRBSLV<2:0>		
23:16	R/W-0 FRACT	R/W-1 SELRES<1:0>	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			STRGSRC<4:0>					
15:8	R/W-0 ON	U-0	R/W-0 SIDL	R/W-1 AICPMPEN	R/W-0 CVDEN	R/W-0 FSSCLKEN	R/W-0 FSPBCLKEN	U-0 —
7:0	U-0 —	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0
		IRQVS<2:0>			STRGLVL	—	—	—

Legend:	HC = Hardware Set	HS = Hardware Cleared
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 31 **TRBEN:** Turbo Channel Enable bit
1 = Enable the Turbo channel
0 = Disable the Turbo channel

bit 30 **TRBERR:** Turbo Channel Error Status bit
1 = An error occurred while setting the Turbo channel and Turbo channel function to be disabled regardless of the TRBEN bit being set to '1'.
0 = Turbo channel error did not occur

Note: The status of this bit is valid only after the TRBEN bit is set.

bit 29-27 **TRBMST<2:0>:** Turbo Master ADCx bits
111 = Reserved
110 = ADC4 is selected as the Turbo Master
.
.
.
000 = ADC0 is selected as the Turbo Master

bit 26-24 **TRBSLV<2:0>:** Turbo Slave ADCx bits
111 = Reserved
110 = ADC4 is selected as the Turbo Slave
.
.
.
000 = ADC0 is selected as the Turbo Slave

bit 23 **FRACT:** Fractional Data Output Format bit
1 = Fractional
0 = Integer

bit 22-21 **SELRES<1:0>:** Shared ADC (ADC7) Resolution bits
11 = 12 bits (default)
10 = 10 bits
01 = 8 bits
00 = 6 bits

Note: Changing the resolution of the ADC does not shift the result in the corresponding ADCDATAx register. The result will still occupy 12 bits, with the corresponding lower unused bits set to '0'. For example, a resolution of 6 bits will result in ADCDATAx<5:0> being set to '0', and ADCDATAx<11:6> holding the result.

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REGISTER 28-26: ADCTRGSNS: ADC TRIGGER LEVEL/EDGE SENSITIVITY REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	LVL11	LVL10	LVL9	LVL8
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	LVL7	LVL6	LVL5	LVL4	LVL3	LVL2	LVL1	LVL0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-12 **Unimplemented:** Read as '0'

bit 11 **LVL11:LVL0:** Trigger Level and Edge Sensitivity bits

1 = Analog input is sensitive to the high level of its trigger (level sensitivity implies retriggering as long as the trigger signal remains high)

0 = Analog input is sensitive to the positive edge of its trigger (this is the value after a reset)

Note 1: This register specifies the trigger level for analog inputs 0 to 31.

2: The higher analog input ID belongs to Class 3, and therefore, is only scan triggered. All Class 3 analog inputs use the Scan Trigger, for which the level/edge is defined by the STRGLVL bit (ADCCON1<3>).

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REGISTER 29-20: CiFIFOCONn: CAN FIFO CONTROL REGISTER 'n' ('n' = 0-31)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	FSIZE<4:0> ⁽¹⁾				
15:8	U-0	S/HC-0	S/HC-0	R/W-0	U-0	U-0	U-0	U-0
	—	FRESET	UINC	DONLY ⁽¹⁾	—	—	—	—
7:0	R/W-0	R-0	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0
	TXEN	TXABAT ⁽²⁾	TXLAR ⁽³⁾	TXERR ⁽³⁾	TXREQ	RTREN	TXPR<1:0>	

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-21 **Unimplemented:** Read as '0'

bit 20-16 **FSIZE<4:0>:** FIFO Size bits⁽¹⁾

11111 = FIFO is 32 messages deep

•
•
•

00010 = FIFO is 3 messages deep

00001 = FIFO is 2 messages deep

00000 = FIFO is 1 message deep

bit 15 **Unimplemented:** Read as '0'

bit 14 **FRESET:** FIFO Reset bits

1 = FIFO will be reset when bit is set, cleared by hardware when FIFO is reset. After setting, the user application should poll whether this bit is clear before taking any action

0 = No effect

bit 13 **UINC:** Increment Head/Tail bit

TXEN = 1: (FIFO configured as a Transmit FIFO)

When this bit is set, the FIFO head will increment by a single message

TXEN = 0: (FIFO configured as a Receive FIFO)

When this bit is set, the FIFO tail will increment by a single message

bit 12 **DONLY:** Store Message Data Only bit⁽¹⁾

TXEN = 1: (FIFO configured as a Transmit FIFO)

This bit is not used and has no effect.

TXEN = 0: (FIFO configured as a Receive FIFO)

1 = Only data bytes will be stored in the FIFO

0 = Full message is stored, including identifier

bit 11-8 **Unimplemented:** Read as '0'

bit 7 **TXEN:** TX/RX Buffer Selection bit

1 = FIFO is a Transmit FIFO

0 = FIFO is a Receive FIFO

Note 1: These bits can only be modified when the CAN module is in Configuration mode (OPMOD<2:0> bits (CiCON<23:21>) = 100).

2: This bit is updated when a message completes (or aborts) or when the FIFO is reset.

3: This bit is reset on any read of this register or when the FIFO is reset.

FIGURE 37-5: EXTERNAL RESET TIMING CHARACTERISTICS

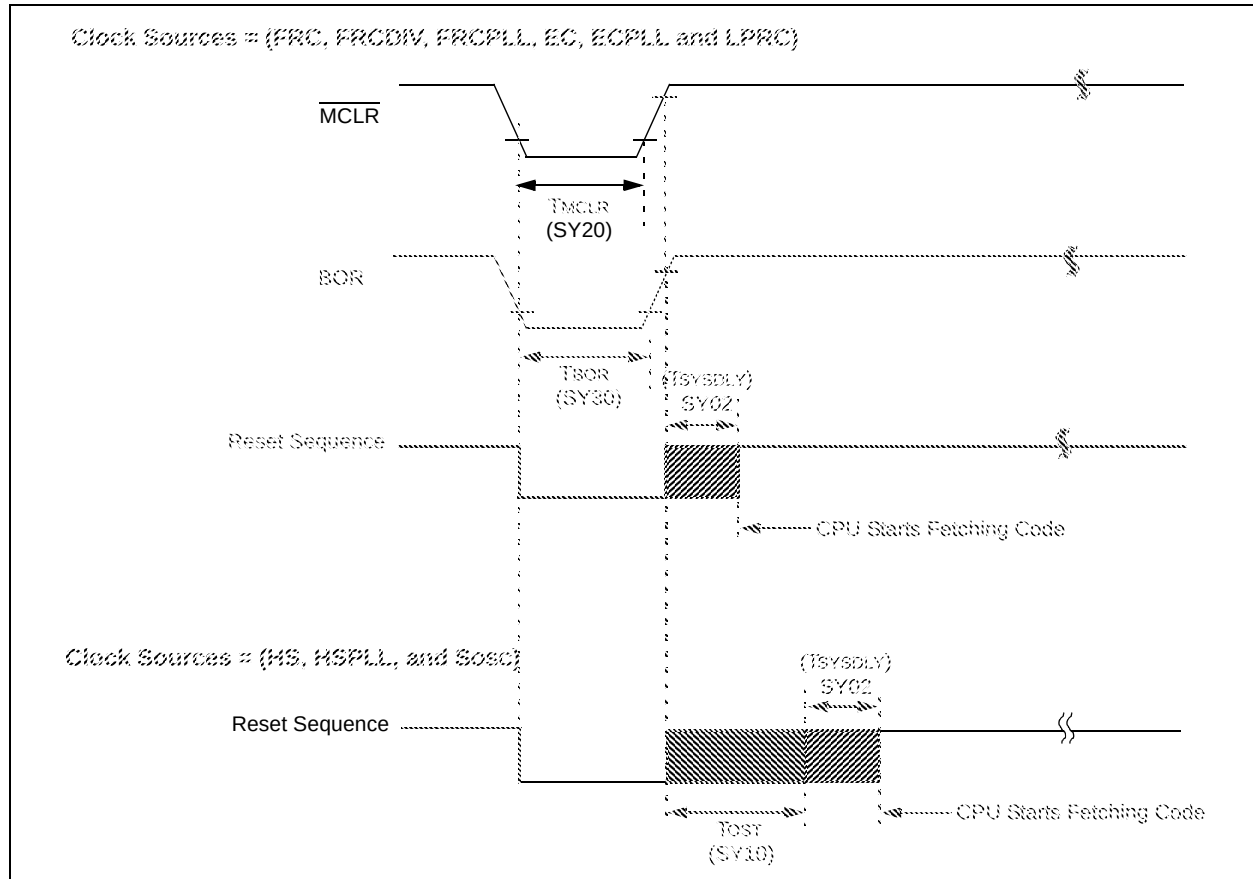


TABLE 37-24: RESETS TIMING

AC CHARACTERISTICS			Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	Symbol	Characteristics ⁽¹⁾	Min.	Typical ⁽²⁾	Max.	Units	Conditions
SY00	TPU	Power-up Period Internal Voltage Regulator Enabled	—	400	600	μs	—
SY02	TSYSDLY	System Delay Period: Time Required to Reload Device Configuration Fuses plus SYSCLK Delay before First instruction is Fetched.	—	1 μs + 8 SYSCLK cycles	—	—	—
SY20	TMCLR	MCLR Pulse Width (low)	2	—	—	μs	—
SY30	TBOR	BOR Pulse Width (low)	—	1	—	μs	—

Note 1: These parameters are characterized, but not tested in manufacturing.

Note 2: Data in "Typ" column is at 3.3V, +25°C unless otherwise stated. Characterized by design but not tested.

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

TABLE 37-33: SPIx MODULE SLAVE MODE (CKE = 1) TIMING REQUIREMENTS (CONTINUED)

AC CHARACTERISTICS			Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	Symbol	Characteristics ⁽¹⁾	Min.	Typical ⁽²⁾	Max.	Units	Conditions
SP50	TssL2scH, TssL2scL	$\overline{SSx}$ ↓ to SCKx ↓ or SCKx ↑ Input	88	—	—	ns	—
SP51	TssH2boZ	$\overline{SSx}$ ↑ to SDOx Output High-Impedance (Note 4)	2.5	—	12	ns	—
SP52	Tsch2ssH TscL2ssH	$\overline{SSx}$ ↑ after SCKx Edge	10	—	—	ns	—
SP60	TssL2boV	SDOx Data Output Valid after $\overline{SSx}$ Edge	—	—	12.5	ns	—

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: The minimum clock period for SCKx is 20 ns.

4: Assumes 30 pF load on all SPIx pins.

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TABLE 37-45: USB OTG ELECTRICAL SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	Symbol	Characteristics ⁽¹⁾	Min.	Typ.	Max.	Units	Conditions
USB313	VUSB3V3	USB Voltage	3.0	—	3.6	V	Voltage on VUSB3V3 must be in this range for proper USB operation
Low-Speed and Full-Speed Modes							
USB315	VILUSB	Input Low Voltage for USB Buffer	—	—	0.8	V	—
USB316	VIHUSB	Input High Voltage for USB Buffer	2.0	—	—	V	—
USB318	VDIFS	Differential Input Sensitivity	0.2	—	—	V	The difference between D+ and D- must exceed this value while VCM is met
USB319	VCM	Differential Common Mode Range	0.8	—	2.5	V	—
USB321	VoL	Voltage Output Low	0.0	—	0.3	V	1.425 kΩ load connected to VUSB3V3
USB322	VoH	Voltage Output High	2.8	—	3.6	V	14.25 kΩ load connected to ground
Hi-Speed Mode							
USB323	VHSDI	Differential input signal level	150	—	—	mV	—
USB324	VHSSQ	SQ detection threshold	100	—	150	mV	—
USB325	VHSCM	Common mode voltage range	-50	—	500	mV	—
USB326	VHSH	Data signaling high	360	—	440	mV	—
USB327	VHSL	Data signaling low	-10	—	10	mV	—
USB328	VCHIRPJ	Chirp J level	700	—	1100	mV	—
USB329	VCHIRPK	Chirp K level	-900	—	-500	mV	—
USB330	ZHSDRV	Driver output resistance	—	45	—	Ω	—

Note 1: These parameters are characterized, but not tested in manufacturing.