Microchip Technology - PIC32MZ1024EFK144T-I/PH Datasheet

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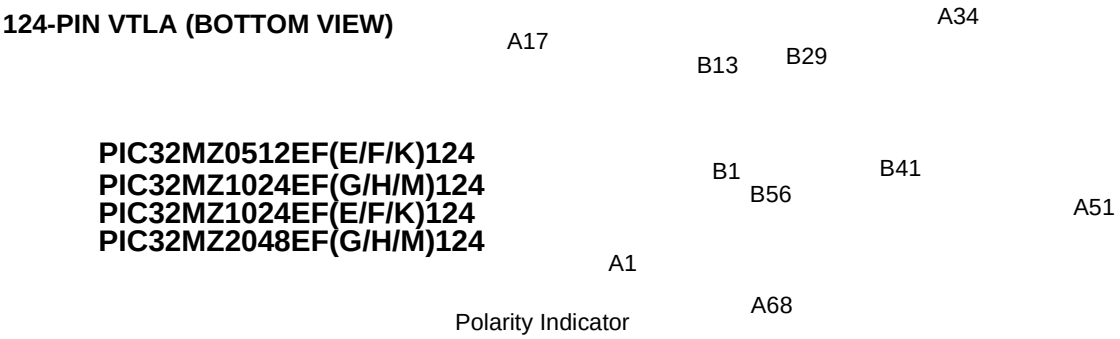
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® M-Class
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, PMP, SPI, SQI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	120
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	2.1V ~ 3.6V
Data Converters	A/D 48x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-TQFP
Supplier Device Package	144-TQFP (16x16)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mz1024efk144t-i-ph

TABLE 4: PIN NAMES FOR 124-PIN DEVICES (CONTINUED)

124-PIN VTLA (BOTTOM VIEW)



Package Pin #	Full Pin Name	Package Pin #	Full Pin Name
B1	EBIA5/AN34/PMA5/RA5	B29	VSS
B2	EBID6/AN16/PMD6/RE6	B30	D+
B3	EBIA6/AN22/RPC1/PMA6/RC1	B31	RPF2/SDA3/RF2
B4	AN36/ETXD1/RJ9	B32	ERXD0/RH8
B5	$\overline{\text{EBIWE}}$/AN20/RPC3/PMWR/RC3	B33	ECOL/RH10
B6	AN14/C1IND/RPG6/SCK2/RG6	B34	EBIRDY1/SDA2/RA3
B7	EBIA3/AN12/C2IND/RPG8/SCL4/PMA3/RG8	B35	VDD
B8	VDD	B36	EBIA9/RPF4/SDA5/PMA9/RF4
B9	EBIA2/AN11/C2INC/RPG9/PMA2/RG9	B37	RPA14/SCL1/RA14
B10	AN25/RPE8/RE8	B38	EBIA15/RPD9/PMCS2/PMA15/RD9
B11	AN45/C1INA/RPB5/RB5	B39	EMDC/RPD11/RD11
B12	AN37/ERXCLK/EREFCLK/RJ11	B40	ERXDV/ECRSDV/RH13
B13	VSS	B41	SOSCI/RPC13/RC13
B14	PGEC2/AN46/RPB6/RB6	B42	EBID14/RPD2/PMD14/RD2
B15	VREF-/CVREF-/AN27/RA9	B43	EBID12/RPD12/PMD12/RD12
B16	AVDD	B44	ETXERR/RJ0
B17	AN38/ETXD2/RH0	B45	EBIRDY3/RJ2
B18	EBIA10/AN48/RPB8/PMA10/RB8	B46	$\overline{\text{SQICS1}}$/RPD5/RD5
B19	EBIA13/CVREFOUT/AN5/RPB10/PMA13/RB10	B47	ETXCLK/RPD7/RD7
B20	VSS	B48	VSS
B21	TCK/EBIA19/AN29/RA1	B49	EBID10/RPF1/PMD10/RF1
B22	TDO/EBIA17/AN31/RPF12/RF12	B50	EBID8/RPG0/PMD8/RG0
B23	AN8/RB13	B51	TRD3/SQID3/RA7
B24	EBIA0/AN10/RPB15/OCFB/PMA0/RB15	B52	EBID0/PMD0/RE0
B25	VDD	B53	VDD
B26	AN41/ERXD1/RH5	B54	TRD2/SQID2/RG14
B27	AN32/AETXD0/RPD14/RD14	B55	TRD0/SQID0/RG13
B28	OSC1/CLKI/RC12	B56	EBID3/RPE3/PMD3/RE3

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and **Section 12.4 "Peripheral Pin Select (PPS)"** for restrictions.

2: Every I/O port pin (RAx-RJx) can be used as a change notification pin (CNAx-CNJx). See **Section 12.0 "I/O Ports"** for more information.

3: Shaded pins are 5V tolerant.

4: The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

TABLE 7-2: INTERRUPT IRQ, VECTOR, AND BIT LOCATION (CONTINUED)

Interrupt Source(1)	XC32 Vector Name	IRQ #	Vector #	Interrupt Bit Location				Persistent Interrupt
				Flag	Enable	Priority	Sub-priority	
UART6 Transfer Done	_UART6_TX_VECTOR	190	OFF190<17:1>	IFS5<30>	IEC5<30>	IPC47<20:18>	IPC47<17:16>	Yes
Reserved	—	191	—	—	—	—	—	—
ADC End of Scan Ready	_ADC_EOS_VECTOR	192	OFF192<17:1>	IFS6<0>	IEC6<0>	IPC48<4:2>	IPC48<1:0>	Yes
ADC Analog Circuits Ready	_ADC_ARDY_VECTOR	193	OFF193<17:1>	IFS6<1>	IEC6<1>	IPC48<12:10>	IPC48<9:8>	Yes
ADC Update Ready	_ADC_URDY_VECTOR	194	OFF194<17:1>	IFS6<2>	IEC6<2>	IPC48<20:18>	IPC48<17:16>	Yes
Reserved	—	195	—	—	—	—	—	—
ADC Group Early Interrupt Request	_ADC_EARLY_VECTOR	196	OFF196<17:1>	IFS6<4>	IEC6<4>	IPC49<4:2>	IPC49<1:0>	Yes
Reserved	—	197	—	—	—	—	—	—
ADC0 Early Interrupt	_ADC0_EARLY_VECTOR	198	OFF198<17:1>	IFS6<6>	IEC6<6>	IPC49<20:18>	IPC49<17:16>	Yes
ADC1 Early Interrupt	_ADC1_EARLY_VECTOR	199	OFF199<17:1>	IFS6<7>	IEC6<7>	IPC49<28:26>	IPC49<25:24>	Yes
ADC2 Early Interrupt	_ADC2_EARLY_VECTOR	200	OFF200<17:1>	IFS6<8>	IEC6<8>	IPC50<4:2>	IPC50<1:0>	Yes
ADC3 Early Interrupt	_ADC2_EARLY_VECTOR	201	OFF201<17:1>	IFS6<9>	IEC6<9>	IPC50<12:10>	IPC50<9:8>	Yes
ADC4 Early Interrupt	_ADC4_EARLY_VECTOR	202	OFF202<17:1>	IFS6<10>	IEC6<10>	IPC50<20:18>	IPC50<17:16>	Yes
Reserved	—	203	—	—	—	—	—	—
Reserved	—	204	—	—	—	—	—	—
ADC7 Early Interrupt	_ADC7_EARLY_VECTOR	205	OFF205<17:1>	IFS6<13>	IEC6<13>	IPC51<12:10>	IPC51<9:8>	Yes
ADC0 Warm Interrupt	_ADC0_WARM_VECTOR	206	OFF206<17:1>	IFS6<14>	IEC6<14>	IPC51<20:18>	IPC51<17:16>	Yes
ADC1 Warm Interrupt	_ADC1_WARM_VECTOR	207	OFF207<17:1>	IFS6<15>	IEC6<15>	IPC51<28:26>	IPC51<25:24>	Yes
ADC2 Warm Interrupt	_ADC2_WARM_VECTOR	208	OFF208<17:1>	IFS6<16>	IEC6<16>	IPC52<4:2>	IPC52<1:0>	Yes
ADC3 Warm Interrupt	_ADC3_WARM_VECTOR	209	OFF209<17:1>	IFS6<17>	IEC6<17>	IPC52<12:10>	IPC52<9:8>	Yes
ADC4 Warm Interrupt	_ADC4_WARM_VECTOR	210	OFF210<17:1>	IFS6<18>	IEC6<18>	IPC52<20:18>	IPC52<17:16>	Yes
Reserved	—	211	—	—	—	—	—	—
Reserved	—	212	—	—	—	—	—	—
ADC7 Warm Interrupt	_ADC7_WARM_VECTOR	213	OFF213<17:1>	IFS6<21>	IEC6<21>	IPC53<12:10>	IPC53<9:8>	Yes
Lowest Natural Order Priority								

Note 1: Not all interrupt sources are available on all devices. See **TABLE 1: "PIC32MZ EF Family Features"** for the list of available peripherals.

2: This interrupt source is not available on 64-pin devices.

3: This interrupt source is not available on 100-pin devices.

4: This interrupt source is not available on 124-pin devices.

REGISTER 10-4: DCRCCON: DMA CRC CONTROL REGISTER (CONTINUED)

bit 6 **CRCAPP:** CRC Append Mode bit(1)
1 = The DMA transfers data from the source into the CRC but NOT to the destination. When a block transfer completes the DMA writes the calculated CRC value to the location given by CHxDSA
0 = The DMA transfers data from the source through the CRC obeying WBO as it writes the data to the destination

bit 5 **CRCTYP:** CRC Type Selection bit
1 = The CRC module will calculate an IP header checksum
0 = The CRC module will calculate a LFSR CRC

bit 4-3 **Unimplemented:** Read as '0'

bit 2-0 **CRCCH<2:0>:** CRC Channel Select bits
111 = CRC is assigned to Channel 7
110 = CRC is assigned to Channel 6
101 = CRC is assigned to Channel 5
100 = CRC is assigned to Channel 4
011 = CRC is assigned to Channel 3
010 = CRC is assigned to Channel 2
001 = CRC is assigned to Channel 1
000 = CRC is assigned to Channel 0

Note 1: When WBO = 1, unaligned transfers are not supported and the CRCAPP bit cannot be set.

REGISTER 10-7: DCHxCON: DMA CHANNEL x CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHPIGN<7:0>							
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	R/W-0	U-0	R/W-0	U-0	U-0	R/W-0
	CHBUSY	—	CHIPGNEN	—	CHPATLEN	—	—	CHCHNS(1)
7:0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R-0	R/W-0	R/W-0
	CHEN(2)	CHAED	CHCHN	CHAEN	—	CHEDET	CHPRI<1:0>	

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-24 **CHPIGN<7:0>:** Channel Register Data bits
Pattern Terminate mode:
Any byte matching these bits during a pattern match may be ignored during the pattern match determination when the CHPIGNEN bit is set. If a byte is read that is identical to this data byte, the pattern match logic will treat it as a "don't care" when the pattern matching logic is enabled and the CHPIGEN bit is set.

bit 23-16 **Unimplemented:** Read as '0'

bit 15 **CHBUSY:** Channel Busy bit
1 = Channel is active or has been enabled
0 = Channel is inactive or has been disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **CHPIGNEN:** Enable Pattern Ignore Byte bit
1 = Treat any byte that matches the CHPIGN<7:0> bits as a "don't care" when pattern matching is enabled
0 = Disable this feature

bit 12 **Unimplemented:** Read as '0'

bit 11 **CHPATLEN:** Pattern Length bit
1 = 2 byte length
0 = 1 byte length

bit 10-9 **Unimplemented:** Read as '0'

bit 8 **CHCHNS:** Chain Channel Selection bit(1)
1 = Chain to channel lower in natural priority (CH1 will be enabled by CH2 transfer complete)
0 = Chain to channel higher in natural priority (CH1 will be enabled by CH0 transfer complete)

bit 7 **CHEN:** Channel Enable bit(2)
1 = Channel is enabled
0 = Channel is disabled

bit 6 **CHAED:** Channel Allow Events If Disabled bit
1 = Channel start/abort events will be registered, even if the channel is disabled
0 = Channel start/abort events will be ignored if the channel is disabled

bit 5 **CHCHN:** Channel Chain Enable bit
1 = Allow channel to be chained
0 = Do not allow channel to be chained

Note 1: The chain selection bit takes effect when chaining is enabled (i.e., CHCHN = 1).

2: When the channel is suspended by clearing this bit, the user application should poll the CHBUSY bit (if available on the device variant) to see when the channel is suspended, as it may take some clock cycles to complete a current transaction before the channel is suspended.

REGISTER 11-3: USBCSR2: USB CONTROL STATUS REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-1	R/W-0
	VBUSERRIE	SESSRQIE	DISCONIE	CONNIE	SOFIE	RESETIE	RESUMEIE	SUSPIE
23:16	R-0, HS	R-0, HS	R-0, HS	R-0, HS	R-0, HS	R-0, HS	R-0, HS	R-0, HS
	VBUSERRIF	SESSRQIF	DISCONIF	CONNIF	SOFIF	RESETIF	RESUMEIF	SUSPIF
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	U-0
	EP7RXIE	EP6RXIE	EP5RXIE	EP4RXIE	EP3RXIE	EP2RXIE	EP1RXIE	—

Legend:	HS = Hardware Set		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **VBUSERRIE:** VBUS Error Interrupt Enable bit
1 = VBUS error interrupt is enabled
0 = VBUS error interrupt is disabled

bit 30 **SESSRQIE:** Session Request Interrupt Enable bit
1 = Session request interrupt is enabled
0 = Session request interrupt is disabled

bit 29 **DISCONIE:** Device Disconnect Interrupt Enable bit
1 = Device disconnect interrupt is enabled
0 = Device disconnect interrupt is disabled

bit 28 **CONNIE:** Device Connection Interrupt Enable bit
1 = Device connection interrupt is enabled
0 = Device connection interrupt is disabled

bit 27 **SOFIE:** Start of Frame Interrupt Enable bit
1 = Start of Frame event interrupt is enabled
0 = Start of Frame event interrupt is disabled

bit 26 **RESETIE:** Reset/Babble Interrupt Enable bit
1 = Interrupt when reset (*Device mode*) or Babble (*Host mode*) is enabled
0 = Reset/Babble interrupt is disabled

bit 25 **RESUMEIE:** Resume Interrupt Enable bit
1 = Resume signaling interrupt is enabled
0 = Resume signaling interrupt is disabled

bit 24 **SUSPIE:** Suspend Interrupt Enable bit
1 = Suspend signaling interrupt is enabled
0 = Suspend signaling interrupt is disabled

bit 23 **VBUSERRIF:** VBUS Error Interrupt bit
1 = VBUS has dropped below the VBUS valid threshold during a session
0 = No interrupt

bit 22 **SESSRQIF:** Session Request Interrupt bit
1 = Session request signaling has been detected
0 = No session request detected

bit 21 **DISCONIF:** Device Disconnect Interrupt bit
1 = In *Host mode*, indicates when a device disconnect is detected. In *Device mode*, indicates when a session ends.
0 = No device disconnect detected

bit 20 **CONNIF:** Device Connection Interrupt bit
1 = In *Host mode*, indicates when a device connection is detected
0 = No device connection detected

REGISTER 11-11: USBIENCSR3: USB INDEXED ENDPOINT CONTROL STATUS REGISTER 3 (ENDPOINT 1-7) (CONTINUED)

bit 15-8 **RXINTERV<7:0>:** Endpoint RX Polling Interval/NAK Limit bits

For Interrupt and Isochronous transfers, this field defines the polling interval for the endpoint. For Bulk endpoints, this field sets the number of frames/microframes after which the endpoint should time out on receiving a stream of NAK responses.

The following table describes the valid values and meaning for this field:

Transfer Type	Speed	Valid Values (m)	Interpretation
Interrupt	Low/Full	0x01 to 0xFF	Polling interval is 'm' frames.
	High	0x01 to 0x10	Polling interval is $2^{(m-1)}$ frames.
Isochronous	Full or High	0x01 to 0x10	Polling interval is $2^{(m-1)}$ frames/microframes.
Bulk	Full or High	0x02 to 0x10	NAK limit is $2^{(m-1)}$ frames/microframes. A value of '0' or '1' disables the NAK time-out function.

bit 7-6 **SPEED<1:0>:** RX Endpoint Operating Speed Control bits
11 = Low-Speed
10 = Full-Speed
01 = Hi-Speed
00 = Reserved

bit 5-4 **PROTOCOL<1:0>:** RX Endpoint Protocol Control bits
11 = Interrupt
10 = Bulk
01 = Isochronous
00 = Control

bit 3-0 **TEP<3:0>:** RX Target Endpoint Number bits

This value is the endpoint number contained in the TX endpoint descriptor returned to the USB module during device enumeration.

TABLE 12-8: PORTD REGISTER MAP FOR 124-PIN AND 144-PIN DEVICES ONLY

Virtual Address (BF86_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0300	ANSELD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ANSD15	ANSD14	—	—	—	—	—	—	—	—	—	—	—	—	—	—	C000
0310	TRISD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRISD15	TRISD14	TRISD13	TRISD12	TRISD11	TRISD10	TRISD9	—	TRISD7	TRISD6	TRISD5	TRISD4	TRISD3	TRISD2	TRISD1	TRISD0	FEFF
0320	PORTD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RD15	RD14	RD13	RD12	RD11	RD10	RD9	—	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	xxxx
0330	LATD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	LATD15	LATD14	LATD13	LATD12	LATD11	LATD10	LATD9	—	LATD7	LATD6	LATD5	LATD4	LATD3	LATD2	LATD1	LATD0	xxxx
0340	ODCD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ODCD15	ODCD14	ODCD13	ODCD12	ODCD11	ODCD10	ODCD9	—	ODCD7	ODCD6	ODCD5	ODCD4	ODCD3	ODCD2	ODCD1	ODCD0	0000
0350	CNPUD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPUD15	CNPUD14	CNPUD13	CNPUD12	CNPUD11	CNPUD10	CNPUD9	—	CNPUD7	CNPUD6	CNPUD5	CNPUD4	CNPUD3	CNPUD2	CNPUD1	CNPUD0	0000
0360	CNPDD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPDD15	CNPDD14	CNPDD13	CNPDD12	CNPDD11	CNPDD10	CNPDD9	—	CNPDD7	CNPDD6	CNPDD5	CNPDD4	CNPDD3	CNPDD2	CNPDD1	CNPDD0	0000
0370	CNCOND	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	EDGE DETECT	—	—	—	—	—	—	—	—	—	—	—	0000
0380	CNEND	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNEND15	CNEND14	CNEND13	CNEND12	CNEND11	CNEND10	CNEND9	—	CNEND7	CNEND6	CNEND5	CNEND4	CNEND3	CNEND2	CNEND1	CNEND0	0000
0390	CNSTATD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CN STATD15	CN STATD14	CN STATD13	CN STATD12	CN STATD11	CN STATD10	CN STATD9	—	CN STATD7	CN STATD6	CN STATD5	CN STATD4	CN STATD3	CN STATD2	CN STATD1	CN STATD0	0000
03A0	CNNED	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNNED15	CNNED14	CNNED13	CNNED12	CNNED11	CNNED10	CNNED9	—	CNNED7	CNNED6	CNNED5	CNNED4	CNNED3	CNNED2	CNNED1	CNNED0	0000
03B0	CNFD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNFD15	CNFD14	CNFD13	CNFD12	CNFD11	CNFD10	CNFD9	—	CNFD7	CNFD6	CNFD5	CNFD4	CNFD3	CNFD2	CNFD1	CNFD0	0000

Legend: x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 "CLR, SET, and INV Registers"** for more information.

TABLE 12-21: PORTK REGISTER MAP FOR 144-PIN DEVICES ONLY

Virtual Address (BF86_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0910	TRISK	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	TRISK7	TRISK6	TRISK5	TRISK4	TRISK3	TRISK2	TRISK1	TRISK0	00FF
0920	PORTK	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	RK7	RK6	RK5	RK4	RK3	RK2	RK1	RK0	xxxx
0930	LATK	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	LATK7	LATK6	LATK5	LATK4	LATK3	LATK2	LATK1	LATK0	xxxx
0940	ODCK	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	ODCK7	ODCK6	ODCK5	ODCK4	ODCK3	ODCK2	ODCK1	ODCK0	0000
0950	CNPUK	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CNPUK7	CNPUK6	CNPUK5	CNPUK4	CNPUK3	CNPUK2	CNPUK1	CNPUK0	0000
0960	CNPDK	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CNPDK7	CNPDK6	CNPDK5	CNPDK4	CNPDK3	CNPDK2	CNPDK1	CNPDK0	0000
0970	CNCONK	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	EDGE DETECT	—	—	—	—	—	—	—	—	—	—	—	0000
0980	CNENK	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CNENK7	CNENK6	CNENK5	CNENK4	CNENK3	CNENK2	CNENK1	CNENK0	0000
0990	CNSTATK	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CN STATK7	CN STATK6	CN STATK5	CN STATK4	CN STATK3	CN STATK2	CN STATK1	CN STATK0	0000
09A0	CNNEK	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CNNEK7	CNNEK6	CNNEK5	CNNEK4	CNNEK3	CNNEK2	CNNEK1	CNNEK0	0000
09B0	CNFK	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CNFK7	CNFK6	CNFK5	CNFK4	CNFK3	CNFK2	CNFK1	CNFK0	0000

Legend: x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8, and 0xC, respectively. See **Section 12.3 "CLR, SET, and INV Registers"** for more information.

15.1 Deadman Timer Control Registers

TABLE 15-1: DEADMAN TIMER REGISTER MAP

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0A00	DMTCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	x000
0A10	DMTPRECLR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	STEP1<7:0>								—	—	—	—	—	—	—	—	0000
0A20	DMTCLR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	STEP2<7:0>								0000
0A30	DMTSTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	BAD1	BAD2	DMTEVENT	—	—	—	—	WINOPN	0000
0A40	DMTCNT	31:16	COUNTER<31:0>																0000
		15:0																	0000
0A60	DMTPSCNT	31:16	PSCNT<31:0>																0000
		15:0																	00xx
0A70	DMTPSINTV	31:16	PSINTV<31:0>																0000
		15:0																	000x

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

REGISTER 28-6: ADCIMCON2: ADC INPUT MODE CONTROL REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DIFF31(1)	SIGN31(1)	DIFF30(1)	SIGN30(1)	DIFF29(1)	SIGN29(1)	DIFF28(1)	SIGN28(1)
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DIFF27(1)	SIGN27(1)	DIFF26(1)	SIGN26(1)	DIFF25(1)	SIGN25(1)	DIFF24(1)	SIGN24(1)
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DIFF23(1)	SIGN23(1)	DIFF22(1)	SIGN22(1)	DIFF21(1)	SIGN21(1)	DIFF20(1)	SIGN20(1)
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DIFF19(1)	SIGN19(1)	DIFF18	SIGN18	DIFF17	SIGN17	DIFF16	SIGN16

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **DIFF31:** AN31 Mode bit(1)
1 = AN31 is using Differential mode
0 = AN31 is using Single-ended mode

bit 30 **SIGN31:** AN31 Signed Data Mode bit(1)
1 = AN31 is using Signed Data mode
0 = AN31 is using Unsigned Data mode

bit 29 **DIFF30:** AN30 Mode bit(1)
1 = AN30 is using Differential mode
0 = AN30 is using Single-ended mode

bit 28 **SIGN30:** AN30 Signed Data Mode bit(1)
1 = AN30 is using Signed Data mode
0 = AN30 is using Unsigned Data mode

bit 27 **DIFF29:** AN29 Mode bit(1)
1 = AN29 is using Differential mode
0 = AN29 is using Single-ended mode

bit 26 **SIGN29:** AN29 Signed Data Mode bit(1)
1 = AN29 is using Signed Data mode
0 = AN29 is using Unsigned Data mode

bit 25 **DIFF28:** AN28 Mode bit(1)
1 = AN28 is using Differential mode
0 = AN28 is using Single-ended mode

bit 24 **SIGN28:** AN28 Signed Data Mode bit(1)
1 = AN28 is using Signed Data mode
0 = AN28 is using Unsigned Data mode

bit 23 **DIFF27:** AN27 Mode bit(1)
1 = AN27 is using Differential mode
0 = AN27 is using Single-ended mode

bit 22 **SIGN27:** AN27 Signed Data Mode bit(1)
1 = AN27 is using Signed Data mode
0 = AN27 is using Unsigned Data mode

Note 1: This bit is not available on 64-pin devices.

REGISTER 28-24: ADCBASE: ADC BASE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ADCBASE<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ADCBASE<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **Unimplemented:** Read as '0'

bit 15-0 **ADCBASE<15:0>:** ADC ISR Base Address bits

This register, when read, contains the base address of the user's ADC ISR jump table. The interrupt vector address is determined by the IRQVS<2:0> bits of the ADCCON1 register specifying the amount of left shift done to the ARDYx status bits in the ADCDSTAT1 and ADCDSTAT2 registers, prior to adding with ADCBASE register.

Interrupt Vector Address = Read Value of ADCBASE and Read Value of ADCBASE = Value written to ADCBASE + x << IRQVS<2:0>, where 'x' is the smallest active analog input ID from the ADCDSTAT1 or ADCDSTAT2 registers (which has highest priority).

REGISTER 29-5: CiTREC: CAN TRANSMIT/RECEIVE ERROR COUNT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	R-0	R-0	R-0	R-0	R-0	R-0
	—	—	TXBO	TXBP	RXBP	TXWARN	RXWARN	EWARN
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	TERRCNT<7:0>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	RERRCNT<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-22 **Unimplemented:** Read as '0'

bit 21 **TXBO:** Transmitter in Error State Bus OFF (TERRCNT ≥ 256)

bit 20 **TXBP:** Transmitter in Error State Bus Passive (TERRCNT ≥ 128)

bit 19 **RXBP:** Receiver in Error State Bus Passive (RERRCNT ≥ 128)

bit 18 **TXWARN:** Transmitter in Error State Warning (128 > TERRCNT ≥ 96)

bit 17 **RXWARN:** Receiver in Error State Warning (128 > RERRCNT ≥ 96)

bit 16 **EWARN:** Transmitter or Receiver is in Error State Warning

bit 15-8 **TERRCNT<7:0>:** Transmit Error Counter

bit 7-0 **RERRCNT<7:0>:** Receive Error Counter

REGISTER 29-6: CiFSTAT: CAN FIFO STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	FIFOIP31	FIFOIP30	FIFOIP29	FIFOIP28	FIFOIP27	FIFOIP26	FIFOIP25	FIFOIP24
23:16	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	FIFOIP23	FIFOIP22	FIFOIP21	FIFOIP20	FIFOIP19	FIFOIP18	FIFOIP17	FIFOIP16
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	FIFOIP15	FIFOIP14	FIFOIP13	FIFOIP12	FIFOIP11	FIFOIP10	FIFOIP9	FIFOIP8
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	FIFOIP7	FIFOIP6	FIFOIP5	FIFOIP4	FIFOIP3	FIFOIP2	FIFOIP1	FIFOIP0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **FIFOIP<31:0>:** FIFOx Interrupt Pending bits

1 = One or more enabled FIFO interrupts are pending

0 = No FIFO interrupts are pending

REGISTER 30-7: ETHPMM0: ETHERNET CONTROLLER PATTERN MATCH MASK 0 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PMM<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PMM<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PMM<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PMM<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-24 **PMM<31:24>:** Pattern Match Mask 3 bits
bit 23-16 **PMM<23:16>:** Pattern Match Mask 2 bits
bit 15-8 **PMM<15:8>:** Pattern Match Mask 1 bits
bit 7-0 **PMM<7:0>:** Pattern Match Mask 0 bits

Note 1: This register is only used for RX operations.
2: The bits in this register may only be changed while the RXEN bit (ETHCON1<8>) = 0 or the PMMODE bit (ETHRXFC<11:8>) = 0.

REGISTER 30-8: ETHPMM1: ETHERNET CONTROLLER PATTERN MATCH MASK 1 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PMM<63:56>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PMM<55:48>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PMM<47:40>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PMM<39:32>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-24 **PMM<63:56>:** Pattern Match Mask 7 bits
bit 23-16 **PMM<55:48>:** Pattern Match Mask 6 bits
bit 15-8 **PMM<47:40>:** Pattern Match Mask 5 bits
bit 7-0 **PMM<39:32>:** Pattern Match Mask 4 bits

Note 1: This register is only used for RX operations.
2: The bits in this register may only be changed while the RXEN bit (ETHCON1<8>) = 0 or the PMMODE bit (ETHRXFC<11:8>) = 0.

REGISTER 30-15: ETHSTAT: ETHERNET CONTROLLER STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BUFCNT<7:0>(1)							
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0
	ETHBUSY(5)	TXBUSY(2,6)	RXBUSY(3,6)	—	—	—	—	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-24 **Unimplemented:** Read as '0'

bit 23-16 **BUFCNT<7:0>:** Packet Buffer Count bits(1)

Number of packet buffers received in memory. Once a packet has been successfully received, this register is incremented by hardware based on the number of descriptors used by the packet. Software decrements the counter (by writing to the BUFCDEC bit (ETHCON1<0>) for each descriptor used) after a packet has been read out of the buffer. The register does not roll over (0xFF to 0x00) when hardware tries to increment the register and the register is already at 0xFF. Conversely, the register does not roll under (0x00 to 0xFF) when software tries to decrement the register and the register is already at 0x0000. When software attempts to decrement the counter at the same time that the hardware attempts to increment the counter, the counter value will remain unchanged.

When this register value reaches 0xFF, the RX logic will halt (only if automatic Flow Control is enabled) awaiting software to write the BUFCDEC bit in order to decrement the register below 0xFF.

If automatic Flow Control is disabled, the RXDMA will continue processing and the BUFCNT will saturate at a value of 0xFF.

When this register is non-zero, the PKTPEND status bit will be set and an interrupt may be generated, depending on the value of the ETHIEN bit <PKTPENDIE> register.

When the ETHRXST register is written, the BUFCNT counter is automatically cleared to 0x00.

Note: BUFCNT will not be cleared when ON is set to '0'. This enables software to continue to utilize and decrement this count.

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **ETHBUSY:** Ethernet Module busy bit(5)

1 = Ethernet logic has been turned on (ON (ETHCON1<15>) = 1) or is completing a transaction
0 = Ethernet logic is idle

This bit indicates that the module has been turned on or is completing a transaction after being turned off.

Note 1: This bit is only used for RX operations.
2: This bit is only affected by TX operations.
3: This bit is only affected by RX operations.
4: This bit is affected by TX and RX operations.
5: This bit will be *set* when the ON bit (ETHCON1<15>) = 1.
6: This bit will be *cleared* when the ON bit (ETHCON1<15>) = 0.

33.3 Peripheral Module Disable

The Peripheral Module Disable (PMD) registers provide a method to disable a peripheral module by stopping all clock sources supplied to that module. When a peripheral is disabled using the appropriate PMD control bit, the peripheral is in a minimum power consumption state. The control and status registers associated with the peripheral are also disabled, so writes to those registers do not have effect and read values are invalid.

To disable a peripheral, the associated PMDx bit must be set to '1'. To enable a peripheral, the associated PMDx bit must be cleared (default). See Table 33-1 for more information.

Note:	Disabling a peripheral module while it's ON bit is set, may result in undefined behavior. The ON bit for the associated peripheral module must be cleared prior to disable a module via the PMDx bits.

TABLE 33-1: PERIPHERAL MODULE DISABLE BITS AND LOCATIONS(1)

Peripheral	PMDx bit Name	Register Name and Bit Location
ADC	ADCMD	PMD1<0>
Comparator Voltage Reference	CVRMD	PMD1<12>
Comparator 1	CMP1MD	PMD2<0>
Comparator 2	CMP2MD	PMD2<1>
Input Capture 1	IC1MD	PMD3<0>
Input Capture 2	IC2MD	PMD3<1>
Input Capture 3	IC3MD	PMD3<2>
Input Capture 4	IC4MD	PMD3<3>
Input Capture 5	IC5MD	PMD3<4>
Input Capture 6	IC6MD	PMD3<5>
Input Capture 7	IC7MD	PMD3<6>
Input Capture 8	IC8MD	PMD3<7>
Input Capture 9	IC9MD	PMD3<8>
Output Compare 1	OC1MD	PMD3<16>
Output Compare 2	OC2MD	PMD3<17>
Output Compare 3	OC3MD	PMD3<18>
Output Compare 4	OC4MD	PMD3<19>
Output Compare 5	OC5MD	PMD3<20>
Output Compare 6	OC6MD	PMD3<21>
Output Compare 7	OC7MD	PMD3<22>
Output Compare 8	OC8MD	PMD3<23>
Output Compare 9	OC9MD	PMD3<24>
Timer1	T1MD	PMD4<0>
Timer2	T2MD	PMD4<1>
Timer3	T3MD	PMD4<2>
Timer4	T4MD	PMD4<3>
Timer5	T5MD	PMD4<4>
Timer6	T6MD	PMD4<5>
Timer7	T7MD	PMD4<6>
Timer8	T8MD	PMD4<7>
Timer9	T9MD	PMD4<8>
UART1	U1MD	PMD5<0>
UART2	U2MD	PMD5<1>

Note 1: Not all modules and associated PMDx bits are available on all devices. See **TABLE 1: "PIC32MZ EF Family Features"** for the lists of available peripherals.

2: Module must not be busy after clearing the associated ON bit and prior to setting the USBMD bit.

REGISTER 34-3: DEVCFG0/ADEVCFG0: DEVICE CONFIGURATION WORD 0 (CONTINUED)

bit 10 **FSLEEP:** Flash Sleep Mode bit
1 = Flash is powered down when the device is in Sleep mode
0 = Flash remains powered when the device is in Sleep mode

bit 9-8 **FECCCON<1:0>:** Dynamic Flash ECC Configuration bits
Upon a device Reset, the value of these bits is copied to the ECCCON<1:0> bits (CFGCON<5:4>).
11 = ECC and dynamic ECC are disabled (ECCCON<1:0> bits are writable)
10 = ECC and dynamic ECC are disabled (ECCCON<1:0> bits are locked)
01 = Dynamic Flash ECC is enabled (ECCCON<1:0> bits are locked)
00 = Flash ECC is enabled (ECCCON<1:0> bits are locked; disables word Flash writes)

bit 7 **Reserved:** Write as '1'

bit 6 **BOOTISA:** Boot ISA Selection bit
1 = Boot code and Exception code is MIPS32®
(ISAONEXC bit is set to '0' and the ISA<1:0> bits are set to '10' in the CP0 Config3 register)
0 = Boot code and Exception code is microMIPS™
(ISAONEXC bit is set to '1' and the ISA<1:0> bits are set to '11' in the CP0 Config3 register)

bit 5 **TRCEN:** Trace Enable bit
1 = Trace features in the CPU are enabled
0 = Trace features in the CPU are disabled

bit 4-3 **ICESEL<1:0>:** In-Circuit Emulator/Debugger Communication Channel Select bits
11 = PGEC1/PGED1 pair is used
10 = PGEC2/PGED2 pair is used
01 = Reserved
00 = Reserved

bit 2 **JTAGEN:** JTAG Enable bit(1)
1 = JTAG is enabled
0 = JTAG is disabled

bit 1-0 **DEBUG<1:0>:** Background Debugger Enable bits (forced to '11' if code-protect is enabled)
1x = Debugger is disabled
0x = Debugger is enabled

Note 1: This bit sets the value of the JTAGEN bit in the CFGCON register.

TABLE 37-33: SPIx MODULE SLAVE MODE (CKE = 1) TIMING REQUIREMENTS (CONTINUED)

AC CHARACTERISTICS			Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typical(2)**	**Max.**	**Units**	**Conditions**
SP50	TssL2scH, TssL2scL	$\overline{SSx}$ ↓ to SCKx ↓ or SCKx ↑ Input	88	—	—	ns	—
SP51	TssH2doZ	$\overline{SSx}$ ↑ to SDOx Output High-Impedance **(Note 4)**	2.5	—	12	ns	—
SP52	TscH2ssH TscL2ssH	$\overline{SSx}$ ↑ after SCKx Edge	10	—	—	ns	—
SP60	TssL2doV	SDOx Data Output Valid after $\overline{SSx}$ Edge	—	—	12.5	ns	—

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: The minimum clock period for SCKx is 20 ns.

4: Assumes 30 pF load on all SPIx pins.

A.9 Other Peripherals and Features

Most of the remaining peripherals on PIC32MZ EF devices act identical to their counterparts on PIC32MX-5XX/6XX/7XX devices. The main differences have to do with handling the increased peripheral bus clock speed and additional clock sources.

Table A-10 lists the differences (indicated by **Bold** type) that will affect software and hardware migration.

TABLE A-10: PERIPHERAL DIFFERENCES

PIC32MX5XX/6XX/7XX Feature	PIC32MZ EF Feature
I^2C	
On PIC32MX devices, all pins are 5V-tolerant.	On PIC32MZ EF devices, the I2C4 port uses non-5V tolerant pins, and will have different VOL/VOH specifications.
I2CxBRG<**11**:0>	The Baud Rate Generator register has been expanded from 12 bits to 16 bits. I2CxBRG<**15**:0>
Watchdog Timer	
Clearing the Watchdog Timer on PIC32MX5XX/6XX/7XX devices required writing a '1' to the WDTCLR bit. **WDTCLR** (WDTCON<**0**>)	On PIC32MZ EF devices, the WDTCLR bit has been replaced with the 16-bit WDTCLRKEY, which must be written with a specific value (0x5743) to clear the Watchdog Timer. In addition, the WDTSPGM (DEVCFG1<21>) bit is used to control operation of the Watchdog Timer during Flash programming. **WDTCLRKEY<15:0>** (WDTCON<**31:16**>)
RTCC	
On PIC32MX devices, the output of the RTCC pin was selected between the Seconds Clock or the Alarm Pulse. RTCSECSEL (RTCCON<7>) 1 = RTCC Seconds Clock is selected for the RTCC pin 0 = RTCC Alarm Pulse is selected for the RTCC pin	On PIC32MZ EF devices, the RTCC Clock is added as an option. RTCSECSEL has been renamed RTCOUTSEL and expanded to two bits. **RTCOUTSEL<1:0>** (RTCCON<**8:**7>) **11 = Reserved** **10 = RTCC Clock is presented on the RTCC pin** 01 = Seconds Clock is presented on the RTCC pin 00 = Alarm Pulse is presented on the RTCC pin when the alarm interrupt is triggered
On PIC32MX devices, the Secondary Oscillator (SOSC) serves as the input clock for the RTCC module.	On PIC32MZ EF devices, an additional clock source, LPRC, is available as a choice for the input clock. **RTCCLKSEL<1:0> (RTCCON<10:9>)** **11 = Reserved** **10 = Reserved** **01 = RTCC uses the external 32.768 kHz SOSC** **00 = RTCC uses the internal 32 kHz oscillator (LPRC)**

NOTES:

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