Microchip Technology - PIC32MZ1024EFK144T-I/PL Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® M-Class
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, PMP, SPI, SQI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	120
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	2.1V ~ 3.6V
Data Converters	A/D 48x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mz1024efk144t-i-pl

TABLE 5: PIN NAMES FOR 144-PIN DEVICES (CONTINUED)

144-PIN LQFP AND TQFP (TOP VIEW)

PIC32MZ0512EF(E/F/K)144
PIC32MZ1024EF(G/H/M)144
PIC32MZ1024EF(E/F/K)144
PIC32MZ2048EF(G/H/M)144

144

1

Pin Number	Full Pin Name	Pin Number	Full Pin Name
73	VBUS	109	RPD1/SCK1/RD1
74	VUSB3V3	110	EBID14/RPD2/PMD14/RD2
75	VSS	111	EBID15/RPD3/PMD15/RD3
76	D-	112	EBID12/RPD12/PMD12/RD12
77	D+	113	EBID13/PMD13/RD13
78	RPF3/USBID/RF3	114	ETXERR/RJ0
79	SDA3/RPF2/RF2	115	EMDIO/RJ1
80	SCL3/RPF8/RF8	116	EBIRDY3/RJ2
81	ERXD0/RH8	117	EBIA22/RJ3
82	ERXD3/RH9	118	$\overline{\text{SQICS0}}$/RPD4/RD4
83	ECOL/RH10	119	$\overline{\text{SQICS1}}$/RPD5/RD5
84	EBIRDY2/RH11	120	ETXEN/RPD6/RD6
85	SCL2/RA2	121	ETXCLK/RPD7/RD7
86	EBIRDY1/SDA2/RA3	122	VDD
87	EBIA14/PMCS1/PMA14/RA4	123	VSS
88	VDD	124	EBID11/RPF0/PMD11/RF0
89	VSS	125	EBID10/RPF1/PMD10/RF1
90	EBIA9/RPF4/SDA5/PMA9/RF4	126	EBIA21/RK7
91	EBIA8/RPF5/SCL5/PMA8/RF5	127	EBID9/RPG1/PMD9/RG1
92	EBIA18/RK4	128	EBID8/RPG0/PMD8/RG0
93	EBIA19/RK5	129	TRCLK/SQICLK/RA6
94	EBIA20/RK6	130	TRD3/SQID3/RA7
95	RPA14/SCL1/RA14	131	$\overline{\text{EBICS0}}$/RJ4
96	RPA15/SDA1/RA15	132	$\overline{\text{EBICS1}}$/RJ5
97	EBIA15/RPD9/PMCS2/PMA15/RD9	133	$\overline{\text{EBICS2}}$/RJ6
98	RPD10/SCK4/RD10	134	$\overline{\text{EBICS3}}$/RJ7
99	EMDC/RPD11/RD11	135	EBID0/PMD0/RE0
100	ECRS/RH12	136	VSS
101	ERXDV/ECRSDV/RH13	137	VDD
102	RH14	138	EBID1/PMD1/RE1
103	EBIA23/RH15	139	TRD2/SQID2/RG14
104	RPD0/RTCC/INT0/RD0	140	TRD1/SQID1/RG12
105	SOSCI/RPC13/RC13	141	TRD0/SQID0/RG13
106	SOSCO/RPC14/T1CK/RC14	142	EBID2/PMD2/RE2
107	VDD	143	EBID3/RPE3/PMD3/RE3
108	VSS	144	EBID4/AN18/PMD4/RE4

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and **Section 12.4 "Peripheral Pin Select (PPS)"** for restrictions.

2: Every I/O port pin (RAx-RKx) can be used as a change notification pin (CNAx-CNKx). See **Section 12.0 "I/O Ports"** for more information.

3: Shaded pins are 5V tolerant.

TABLE 1-1: ADC PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number				Pin Type	Buffer Type	Description
	64-pin QFN/ TQFP	100-pin TQFP	124-pin VTLA	144-pin TQFP/ LQFP			
AN36	—	—	B4	8	I	Analog	Analog Input Channels
AN37	—	—	B12	27	I	Analog	
AN38	—	—	B17	43	I	Analog	
AN39	—	—	A22	44	I	Analog	
AN40	—	—	A30	65	I	Analog	
AN41	—	—	B26	66	I	Analog	
AN42	—	—	A31	67	I	Analog	
AN45	11	20	B11	25	I	Analog	
AN46	17	26	B14	37	I	Analog	
AN47	18	27	A19	38	I	Analog	
AN48	21	32	B18	47	I	Analog	
AN49	22	33	A23	48	I	Analog	

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

TABLE 4-9: SYSTEM BUS TARGET 1 REGISTER MAP

Virtual Address (BF8F_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
8420	SBT1ELOG1	31:16	MULTI	—	—	—	CODE<3:0>				—	—	—	—	—	—	—	—	0000
		15:0	INITID<7:0>								REGION<3:0>				—	CMD<2:0>			0000
8424	SBT1ELOG2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	GROUP<1:0>		0000
8428	SBT1ECON	31:16	—	—	—	—	—	—	—	ERRP	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
8430	SBT1ECLRS	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
8438	SBT1ECLRM	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
8440	SBT1REG0	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
8450	SBT1RD0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8458	SBT1WR0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8480	SBT1REG2	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
8490	SBT1RD2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8498	SBT1WR2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
84A0	SBT1REG3	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
84B0	SBT1RD3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
84B8	SBT1WR3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
84C0	SBT1REG4	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
84D0	SBT1RD4	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
84D8	SBT1WR4	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.
Note: For reset values listed as 'xxxx', please refer to Table 4-6 for the actual reset values.

5.1 Flash Control Registers

TABLE 5-1: FLASH CONTROLLER REGISTER MAP

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0600	NVMCON(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	WR	WREN	WRERR	LVDERR	—	—	—	—	PFSWAP	BFSWAP	—	—	NVMOP<3:0>				00x0
0610	NVMKEY	31:16	NVMKEY<31:0>																0000
		15:0																	0000
0620	NVMADDR(1)	31:16	NVMADDR<31:0>																0000
		15:0																	0000
0630	NVMDATA0	31:16	NVMDATA0<31:0>																0000
		15:0																	0000
0640	NVMDATA1	31:16	NVMDATA1<31:0>																0000
		15:0																	0000
0650	NVMDATA2	31:16	NVMDATA2<31:0>																0000
		15:0																	0000
0660	NVMDATA3	31:16	NVMDATA3<31:0>																0000
		15:0																	0000
0670	NVMSRC ADDR	31:16	NVMSRCADDR<31:0>																0000
		15:0																	0000
0680	NVMPWP(1)	31:16	PWPULOCK	—	—	—	—	—	—	—	PWP<23:16>								8000
		15:0	PWP<15:0>																0000
0690	NVMBWP(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	LBWPULOCK	—	—	LBWP4	LBWP3	LBWP2	LBWP1	LBWP0	UBWPULOCK	—	—	UBWP4	UBWP3	UBWP2	UBWP1	UBWP0	9FDF
06A0	NVMCON2(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	001F
		15:0	—	—	—	—	—	—	—	—	SWAPLOCK<1:0>		—	—	—	—	—	—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 "CLR, SET, and INV Registers"** for more information.

TABLE 7-3: INTERRUPT REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
02E0	IPC26	31:16	—	—	—	CRPTIP<2:0>(7)			CRPTIS<1:0>(7)		—	—	—	SBIP<2:0>			SBIS<1:0>		0000
		15:0	—	—	—	CFDCIP<2:0>			CFDCIS<1:0>		—	—	—	CPCIP<2:0>			CPCIS<1:0>		0000
02F0	IPC27	31:16	—	—	—	SPI1TXIP<2:0>			SPI1TXIS<1:0>		—	—	—	SPI1RXIP<2:0>			SPI1RXIS<1:0>		0000
		15:0	—	—	—	SPI1EIP<2:0>			SPI1EIS<1:0>		—	—	—	—	—	—	—	—	0000
0300	IPC28	31:16	—	—	—	I2C1BIP<2:0>			I2C1BIS<1:0>		—	—	—	U1TXIP<2:0>			U1TXIS<1:0>		0000
		15:0	—	—	—	U1RXIP<2:0>			U1RXIS<1:0>		—	—	—	U1EIP<2:0>			U1EIS<1:0>		0000
0310	IPC29	31:16	—	—	—	CNBIP<2:0>			CNBIS<1:0>		—	—	—	CNAIP<2:0>(2)			CNAIS<1:0>(2)		0000
		15:0	—	—	—	I2C1MIP<2:0>			I2C1MIS<1:0>		—	—	—	I2C1SIP<2:0>			I2C1SIS<1:0>		0000
0320	IPC30	31:16	—	—	—	CNFIP<2:0>			CNFIS<1:0>		—	—	—	CNEIP<2:0>			CNEIS<1:0>		0000
		15:0	—	—	—	CNDIP<2:0>			CNDIS<1:0>		—	—	—	CNCIP<2:0>			CNCIS<1:0>		0000
0330	IPC31	31:16	—	—	—	CNKIP<2:0>(2,4,8)			CNKIS<1:0>(2,4,8)		—	—	—	CNJIP<2:0>(2,4)			CNJIS<1:0>(2,4)		0000
		15:0	—	—	—	CNHIP<2:0>(2,4)			CNHIS<1:0>(2,4)		—	—	—	CNGIP<2:0>			CNGIS<1:0>		0000
0340	IPC32	31:16	—	—	—	CMP2IP<2:0>			CMP2IS<1:0>		—	—	—	CMP1IP<2:0>			CMP1IS<1:0>		0000
		15:0	—	—	—	PMPEIP<2:0>			PMPEIS<1:0>		—	—	—	PMPIP<2:0>			PMPIS<1:0>		0000
0350	IPC33	31:16	—	—	—	DMA1IP<2:0>			DMA1IS<1:0>		—	—	—	DMA0IP<2:0>			DMA0IS<1:0>		0000
		15:0	—	—	—	USBDMAIP<2:0>			USBDMAIS<1:0>		—	—	—	USBIP<2:0>			USBIS<1:0>		0000
0360	IPC34	31:16	—	—	—	DMA5IP<2:0>			DMA5IS<1:0>		—	—	—	DMA4IP<2:0>			DMA4IS<1:0>		0000
		15:0	—	—	—	DMA3IP<2:0>			DMA3IS<1:0>		—	—	—	DMA2IP<2:0>			DMA2IS<1:0>		0000
0370	IPC35	31:16	—	—	—	SPI2RXIP<2:0>			SPI2RXIS<1:0>		—	—	—	SPI2EIP<2:0>			SPI2EIS<1:0>		0000
		15:0	—	—	—	DMA7IP<2:0>			DMA7IS<1:0>		—	—	—	DMA6IP<2:0>			DMA6IS<1:0>		0000
0380	IPC36	31:16	—	—	—	U2TXIP<2:0>			U2TXIS<1:0>		—	—	—	U2RXIP<2:0>			U2RXIS<1:0>		0000
		15:0	—	—	—	U2EIP<2:0>			U2EIS<1:0>		—	—	—	SPI2TXIP<2:0>			SPI2TXIS<1:0>		0000
0390	IPC37	31:16	—	—	—	CAN1IP<2:0>(3)			CAN1IS<1:0>(3)		—	—	—	I2C2MIP<2:0>(2)			I2C2MIS<1:0>(2)		0000
		15:0	—	—	—	I2C2SIP<2:0>(2)			I2C2SIS<1:0>(2)		—	—	—	I2C2BIP<2:0>(2)			I2C2BIS<1:0>(2)		0000
03A0	IPC38	31:16	—	—	—	SPI3RXIP<2:0>			SPI3RXIS<1:0>		—	—	—	SPI3EIP<2:0>			SPI3EIS<1:0>		0000
		15:0	—	—	—	ETHIP<2:0>			ETHIS<1:0>		—	—	—	CAN2IP<2:0>(3)			CAN2IS<1:0>(3)		0000
03B0	IPC39	31:16	—	—	—	U3TXIP<2:0>			U3TXIS<1:0>		—	—	—	U3RXIP<2:0>			U3RXIS<1:0>		0000
		15:0	—	—	—	U3EIP<2:0>			U3EIS<1:0>		—	—	—	SPI3TXIP<2:0>			SPI3TXIS<1:0>		0000
03C0	IPC40	31:16	—	—	—	SPI4EIP<2:0>			SPI4EIS<1:0>		—	—	—	I2C3MIP<2:0>			I2C3MIS<1:0>		0000
		15:0	—	—	—	I2C3SIP<2:0>			I2C3SIS<1:0>		—	—	—	I2C3BIP<2:0>			I2C3BIS<1:0>		0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 "CLR, SET, and INV Registers"** for more information.
2: This bit or register is not available on 64-pin devices.
3: This bit or register is not available on devices without a CAN module.
4: This bit or register is not available on 100-pin devices.
5: Bits 31 and 30 are not available on 64-pin and 100-pin devices; bits 29 through 14 are not available on 64-pin devices.
6: Bits 31, 30, 29, and bits 5 through 0 are not available on 64-pin and 100-pin devices; bit 31 is not available on 124-pin devices; bit 22 is not available on 64-pin devices.
7: This bit or register is not available on devices without a Crypto module.
8: This bit or register is not available on 124-pin devices.

10.0 DIRECT MEMORY ACCESS (DMA) CONTROLLER

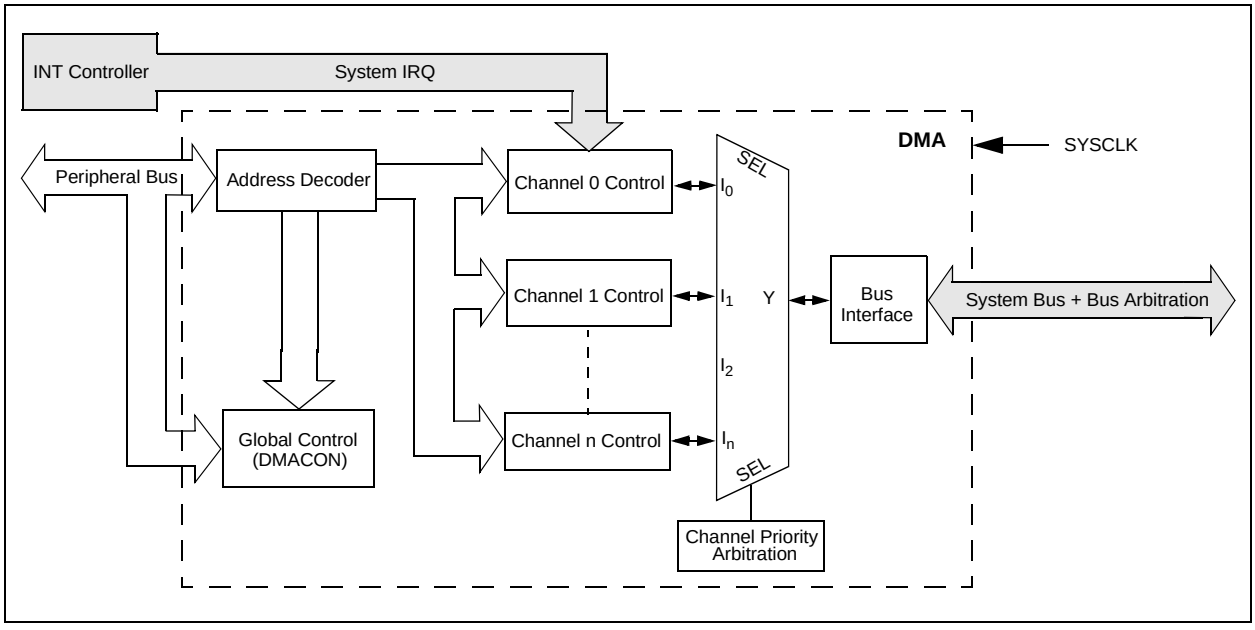
Note: This data sheet summarizes the features of the PIC32MZ EF family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 31. "Direct Memory Access (DMA) Controller"** (DS60001117) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

The Direct Memory Access (DMA) Controller is a bus master module useful for data transfers between different devices without CPU intervention. The source and destination of a DMA transfer can be any of the memory mapped modules existent in the device such as SPI, UART, PMP, etc., or memory itself.

The following are key features of the DMA Controller:

- Eight identical channels, each featuring:
  - Auto-increment source and destination address registers
  - Source and destination pointers
  - Memory to memory and memory to peripheral transfers
- Automatic word-size detection:
  - Transfer granularity, down to byte level
  - Bytes need not be word-aligned at source and destination
- Fixed priority channel arbitration
- Flexible DMA channel operating modes:
  - Manual (software) or automatic (interrupt) DMA requests
  - One-Shot or Auto-Repeat Block Transfer modes
  - Channel-to-channel chaining
- Flexible DMA requests:
  - A DMA request can be selected from any of the peripheral interrupt sources
  - Each channel can select any (appropriate) observable interrupt as its DMA request source
  - A DMA transfer abort can be selected from any of the peripheral interrupt sources
  - Up to 2-byte Pattern (data) match transfer termination
- Multiple DMA channel status interrupts:
  - DMA channel block transfer complete
  - Source empty or half empty
  - Destination full or half full
  - DMA transfer aborted due to an external event
  - Invalid DMA address generated
- DMA debug support features:
  - Most recent error address accessed by a DMA channel
  - Most recent DMA channel to transfer data
- CRC Generation module:
  - CRC module can be assigned to any of the available channels
  - CRC module is highly configurable

FIGURE 10-1: DMA BLOCK DIAGRAM



REGISTER 11-13: USBOTG: USB OTG CONTROL/STATUS REGISTER (CONTINUED)

bit 0 **SESSION:** Active Session Control/Status bit

'A' device:

1 = Start a session

0 = End a session

'B' device:

1 = (Read) Session has started or is in progress, (Write) Initiate the Session Request Protocol

0 = When USB module is in Suspend mode, clearing this bit will cause a software disconnect

Clearing this bit when the USB module is not suspended will result in undefined behavior.

REGISTER 11-26: USBTMCON1: USB TIMING CONTROL REGISTER 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-1
	THHSRTN<15:8>							
23:16	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0	R/W-1	R/W-1	R/W-0
	THHSRTN<7:0>							
15:8	R/W-0	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	TUCH<15:8>							
7:0	R/W-0	R/W-1	R/W-1	R/W-1	R/W-0	R/W-1	R/W-0	R/W-0
	TUCH<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **THHSRTN:<15:0>:** Hi-Speed Resume Signaling Delay bits
These bits set the delay from the end of Hi-Speed resume signaling (acting as a Host) to enable the UTM normal operating mode.

bit 15-0 **TUCH<15:0>:** Chirp Time-out bits
These bits set the chirp time-out. This number, when multiplied by 4, represents the number of USB module clock cycles before the time-out occurs.

Note: Use of this register will allow the Hi-Speed time-out to be set to values that are greater than the maximum specified in the USB 2.0 specification, making the USB module non-compliant.

REGISTER 11-27: USBTMCON2: USB TIMING CONTROL REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	THBST<3:0>			

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-4 **Unimplemented:** Read as '0'

bit 3-0 **THBST<3:0>:** High Speed Time-out Adder bits
These bits represent the value to be added to the minimum high speed time-out period of 736 bit times. The time-out period can be increased in increments of 64 Hi-Speed bit times (133 ns).

Note: Use of this register will allow the Hi-Speed time-out to be set to values that are greater than the maximum specified in the USB 2.0 specification, making the USB module non-compliant.

12.0 I/O PORTS

Note: This data sheet summarizes the features of the PIC32MZ EF family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 12. "I/O Ports"** (DS60001120) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

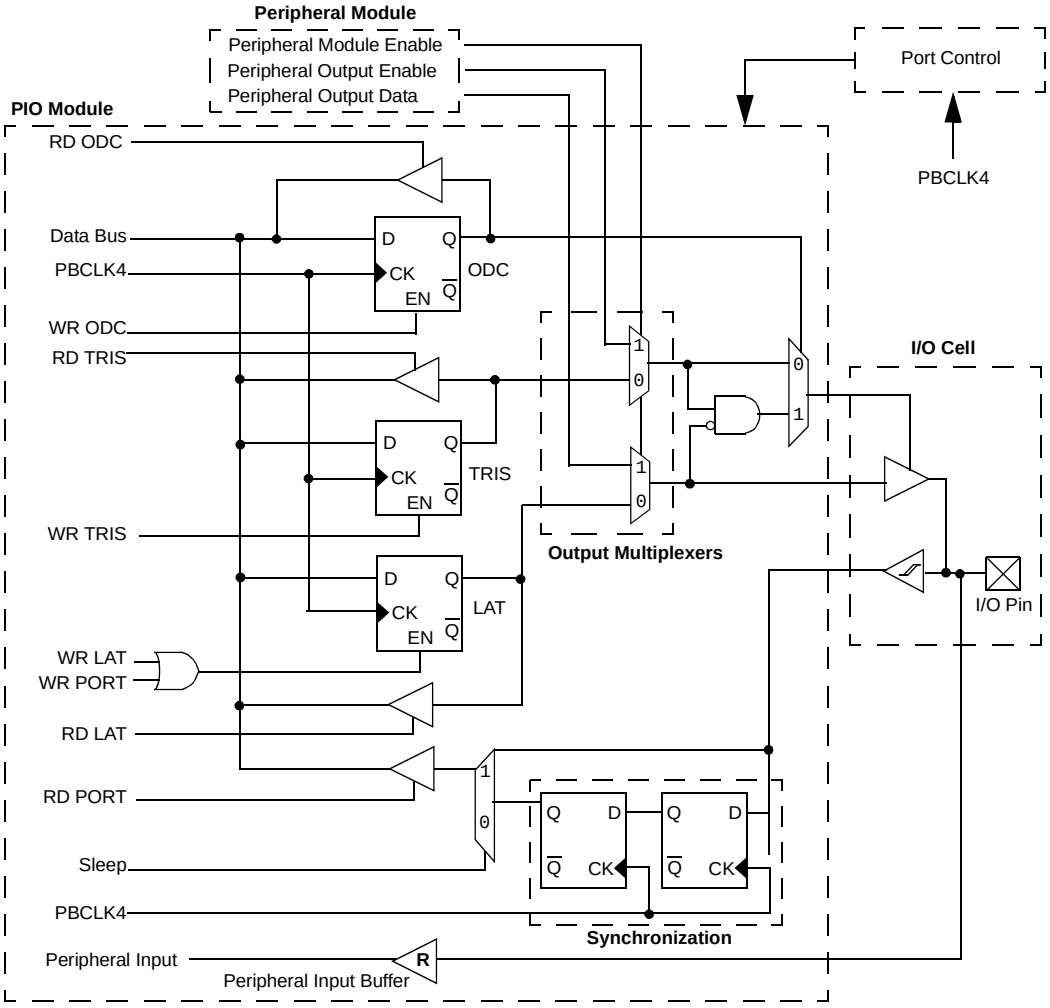
General purpose I/O pins are the simplest of peripherals. They allow the PIC32MZ EF family device to monitor and control other devices. To add flexibility and functionality, some pins are multiplexed with alternate function(s). These functions depend on which peripheral features are on the device. In general, when a peripheral is functioning, that pin may not be used as a general purpose I/O pin.

Some of the key features of the I/O ports are:

- Individual output pin open-drain enable/disable
- Individual input pin weak pull-up and pull-down
- Monitor selective inputs and generate interrupt when change in pin state is detected
- Operation during Sleep and Idle modes
- Fast bit manipulation using CLR, SET and INV registers

Figure 12-1 illustrates a block diagram of a typical multiplexed I/O port.

FIGURE 12-1: BLOCK DIAGRAM OF A TYPICAL MULTIPLEXED PORT STRUCTURE



Legend: R = Peripheral input buffer types may vary. Refer to Table 1-1 for peripheral details.

Note: This block diagram is a general representation of a shared port/peripheral structure for illustration purposes only. The actual structure for any specific port/peripheral combination may be different than it is shown here.

TABLE 12-13: PORTF REGISTER MAP FOR 100-PIN, 124-PIN, AND 144-PIN DEVICES ONLY

Virtual Address (BF86_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0500	ANSELF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	ANSF13	ANSF12	—	—	—	—	—	—	—	—	—	—	—	—	3000
0510	TRISF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	TRISF13	TRISF12	—	—	—	TRISF8	—	—	TRISF5	TRISF4	TRISF3	TRISF2	TRISF1	TRISF0	313F
0520	PORTF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	RF13	RF12	—	—	—	RF8	—	—	RF5	RF4	RF3	RF2	RF1	RF0	xxxx
0530	LATF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	LATF13	LATF12	—	—	—	LATF8	—	—	LATF5	LATF4	LATF3	LATF2	LATF1	LATF0	xxxx
0540	ODCF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	ODCF13	ODCF12	—	—	—	ODCF8	—	—	ODCF5	ODCF4	ODCF3	ODCF2	ODCF1	ODCF0	0000
0550	CNPUF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	CNPUF13	CNPUF12	—	—	—	CNPUF8	—	—	CNPUF5	CNPUF4	CNPUF3	CNPUF2	CNPUF1	CNPUF0	0000
0560	CNPDF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	CNPDF13	CNPDF12	—	—	—	CNPDF8	—	—	CNPDF5	CNPDF4	CNPDF3	CNPDF2	CNPDF1	CNPDF0	0000
0570	CNCONF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	EDGE DETECT	—	—	—	—	—	—	—	—	—	—	—	0000
0580	CNENF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	CNENF13	CNENF12	—	—	—	CNENF8	—	—	CNENF5	CNENF4	CNENF3	CNENF2	CNENF1	CNENF0	0000
0590	CNSTATF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	CN STATF13	CN STATF12	—	—	—	CN STATF8	—	—	CN STATF5	CN STATF4	CN STATF3	CN STATF2	CN STATF1	CN STATF0	0000
05A0	CNNEF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	CNNEF13	CNNEF12	—	—	—	CNNEF8	—	—	CNNEF5	CNNEF4	CNNEF3	CNNEF2	CNNEF1	CNNEF0	0000
05B0	CNFF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	CNFF13	CNFF12				CNFF8			CNFF5	CNFF4	CNFF3	CNFF2	CNFF1	CNFF0	0000
05C0	SRCON0F	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SR0F1	SR0F0	0000
05D0	SRCON1F	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SR1F1	SR1F0	0000

Legend: x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 "CLR, SET, and INV Registers"** for more information.

TABLE 14-1: TIMER2 THROUGH TIMER9 REGISTER MAP (CONTINUED)

Virtual Address (BF84_#)	Register Name(1)	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0C10	TMR7	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TMR7<15:0>																0000
0C20	PR7	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PR7<15:0>																FFFF
0E00	T8CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	TGATE	TCKPS<2:0>			T32	—	TCS	—	0000
0E10	TMR8	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TMR8<15:0>																0000
0E20	PR8	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PR8<15:0>																FFFF
1000	T9CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	TGATE	TCKPS<2:0>			—	—	TCS	—	0000
1010	TMR9	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TMR9<15:0>																0000
1020	PR9	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PR9<15:0>																FFFF

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 "CLR, SET, and INV Registers"** for more information.

REGISTER 15-3: DMTCLR: DEADMAN TIMER CLEAR REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	STEP2<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7-0 **STEP2<7:0>:** Clear Timer bits

00001000 = Clears STEP1<7:0>, STEP2<7:0> and the Deadman Timer if, and only if, preceded by correct loading of STEP1<7:0> bits in the correct sequence. The write to these bits may be verified by reading DMTCNT and observing the counter being reset.

All other write patterns = Set BAD2 bit, the value of STEP1<7:0> will remain unchanged, and the new value being written STEP2<7:0> will be captured. These bits are also cleared when a DMT reset event occurs.

REGISTER 20-12: SQI1STAT1: SQI STATUS REGISTER 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	TXFIFOFREE<7:0>							
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	RXFIFOCNT<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-24 **Unimplemented:** Read as '0'

bit 23-16 **TXFIFOFREE<7:0>:** Transmit FIFO Available Word Space bits

bit 15-8 **Unimplemented:** Read as '0'

bit 7-0 **RXFIFOCNT<7:0>:** Number of words of read data in the FIFO

REGISTER 28-32: ADCANCON: ADC ANALOG WARM-UP CONTROL REGISTER (CONTINUED)

bit 7 **ANEN7:** Shared ADC (ADC7) Analog and Bias Circuitry Enable bit

1 = Analog and bias circuitry enabled. Once the analog and bias circuit is enabled, the ADC module needs a warm-up time, as defined by the WKUPCLKCNT<3:0> bits.

0 = Analog and bias circuitry disabled

bit 5-6 **Unimplemented:** Read as '0'

bit 4-0 **ANEN4:ANEN0:** ADC4-ADC0 Analog and Bias Circuitry Enable bits

1 = Analog and bias circuitry enabled. Once the analog and bias circuit is enabled, the ADC module needs a warm-up time, as defined by the WKUPCLKCNT<3:0> bits.

0 = Analog and bias circuitry disabled

REGISTER 29-2: CiCFG: CAN BAUD RATE CONFIGURATION REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	WAKFIL	—	—	—	SEG2PH<2:0>(1,4)		
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SEG2PHTS(1)	SAM(2)	SEG1PH<2:0>			PRSEG<2:0>		
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SJW<1:0>(3)		BRP<5:0>					

Legend:	HC = Hardware Clear	S = Settable bit	
R = Readable bit	W = Writable bit	P = Programmable bit	r = Reserved bit
U = Unimplemented bit	-n = Bit Value at POR: (‘0’, ‘1’, x = Unknown)		

bit 31-23 **Unimplemented:** Read as ‘0’

bit 22 **WAKFIL:** CAN Bus Line Filter Enable bit
1 = Use CAN bus line filter for wake-up
0 = CAN bus line filter is not used for wake-up

bit 21-19 **Unimplemented:** Read as ‘0’

bit 18-16 **SEG2PH<2:0>:** Phase Buffer Segment 2 bits(1,4)
111 = Length is 8 x TQ
•
•
•
000 = Length is 1 x TQ

bit 15 **SEG2PHTS:** Phase Segment 2 Time Select bit(1)
1 = Freely programmable
0 = Maximum of SEG1PH or Information Processing Time, whichever is greater

bit 14 **SAM:** Sample of the CAN Bus Line bit(2)
1 = Bus line is sampled three times at the sample point
0 = Bus line is sampled once at the sample point

bit 13-11 **SEG1PH<2:0>:** Phase Buffer Segment 1 bits(4)
111 = Length is 8 x TQ
•
•
•
000 = Length is 1 x TQ

Note 1: SEG2PH ≤ SEG1PH. If SEG2PHTS is clear, SEG2PH will be set automatically.
2: 3 Time bit sampling is not allowed for BRP < 2.
3: SJW ≤ SEG2PH.
4: The Time Quanta per bit must be greater than 7 (that is, TQBIT > 7).

Note: This register can only be modified when the CAN module is in Configuration mode (OPMOD<2:0> (CiCON<23:21>) = 100).

34.3 On-Chip Voltage Regulator

The core and digital logic for all PIC32MZ EF devices is designed to operate at a nominal 1.8V. To simplify system designs, devices in the PIC32MZ EF family incorporate an on-chip regulator providing the required core logic voltage from VDD.

34.3.1 ON-CHIP REGULATOR AND POR

It takes a fixed delay for the on-chip regulator to generate an output. During this time, designated as TPU, code execution is disabled. TPU is applied every time the device resumes operation after any power-down, including Sleep mode.

34.3.2 ON-CHIP REGULATOR AND BOR

PIC32MZ EF devices also have a simple brown-out capability. If the voltage supplied to the regulator is inadequate to maintain a regulated level, the regulator Reset circuitry will generate a Brown-out Reset. This event is captured by the BOR flag bit (RCON<1>). The brown-out voltage levels are specific in **Section 37.1 "DC Characteristics"**.

34.4 On-chip Temperature Sensor

PIC32MZ EF devices include a temperature sensor that provides accurate measurement of a device's junction temperature (see **Section 37.2 "AC Characteristics and Timing Parameters"** for more information).

The temperature sensor is connected to the ADC module and can be measured using the shared S&H circuit (see **Section 28.0 "12-bit High-Speed Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC)"** for more information).

34.5 Programming and Diagnostics

PIC32MZ EF devices provide a complete range of programming and diagnostic features that can increase the flexibility of any application using them. These features allow system designers to include:

- Simplified field programmability using two-wire In-Circuit Serial Programming™ (ICSP™) interfaces
- Debugging using ICSP
- Programming and debugging capabilities using the EJTAG extension of JTAG
- JTAG boundary scan testing for device and board diagnostics

PIC32 devices incorporate two programming and diagnostic modules, and a trace controller, that provide a range of functions to the application developer.

FIGURE 34-1: BLOCK DIAGRAM OF PROGRAMMING, DEBUGGING AND TRACE PORTS

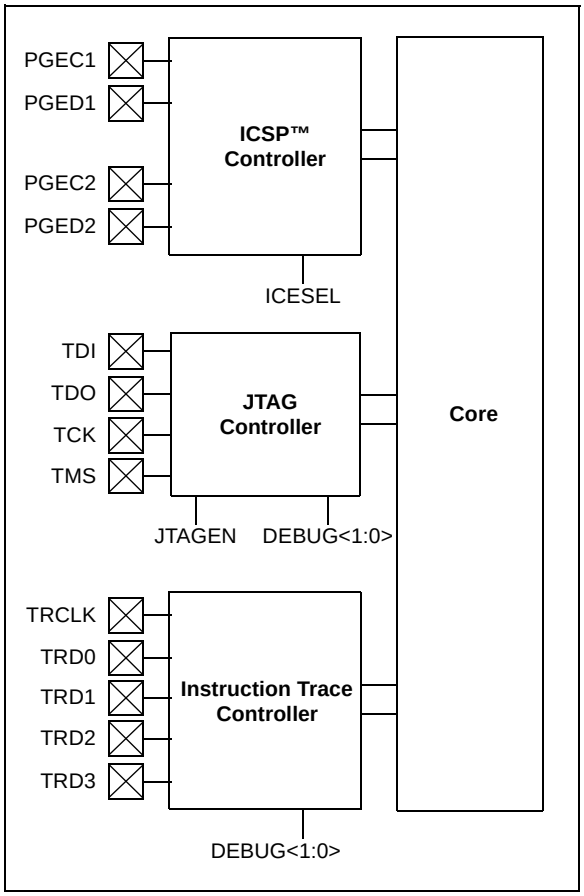


TABLE 37-39: ANALOG-TO-DIGITAL CONVERSION TIMING REQUIREMENTS

AC CHARACTERISTICS(2)			Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Symbol**	**Characteristics**	**Min.**	**Typ.(1)**	**Max.**	**Units**	**Conditions**
Clock Parameters							
AD50	TAD	ADC Clock Period	20	—	6250	ns	—
Throughput Rate							
AD51	FTP	Sample Rate for ADC0-ADC4 (Class 1 Inputs)	— — — —	— — — —	3.125 3.57 4.16 5	Msps Msps Msps Msps	12-bit resolution Source Impedance ≤ 200Ω 10-bit resolution Source Impedance ≤ 200Ω 8-bit resolution Source Impedance ≤ 200Ω 6-bit resolution Source Impedance ≤ 200Ω
		Sample Rate for ADC7 (Class 2 and Class 3 Inputs)	— — — —	— — — —	2.94 3.33 3.84 4.55	Msps Msps Msps Msps	12-bit resolution Source Impedance ≤ 200Ω 10-bit resolution Source Impedance ≤ 200Ω 8-bit resolution Source Impedance ≤ 200Ω 6-bit resolution Source Impedance ≤ 200Ω
Timing Parameters							
AD60	TSAMP	Sample Time for ADC0-ADC4 (Class 1 Inputs)	3 4 5 13	—	—	TAD	Source Impedance ≤ 200Ω, Max ADC clock Source Impedance ≤ 500Ω, Max ADC clock Source Impedance ≤ 1 KΩ, Max ADC clock Source Impedance ≤ 5 KΩ, Max ADC clock
		Sample Time for ADC7 (Class 2 and 3 Inputs)	4 5 6 14	—	—	TAD	Source Impedance ≤ 200Ω, Max ADC clock Source Impedance ≤ 500Ω, Max ADC clock Source Impedance ≤ 1 KΩ, Max ADC clock Source Impedance ≤ 5 KΩ, Max ADC clock
		Sample Time for ADC7 (Class 2 and 3 Inputs)	See Table 37-40	—	—	TAD	CVDEN (ADCCON1<11>) = 1
AD62	TCONV	Conversion Time (after sample time is complete)	— — — —	— — — —	13 11 9 7	TAD	12-bit resolution 10-bit resolution 8-bit resolution 6-bit resolution
AD65	TWAKE	Wake-up time from Low-Power Mode	— —	500 20	— —	TAD µs	Lesser of 500 TAD or 20 µs.

Note 1: These parameters are characterized, but not tested in manufacturing.

2: The ADC module is functional at VBORMIN < VDD < VDDMIN, but with degraded performance. Unless otherwise stated, module functionality is guaranteed, but not characterized.

TABLE 38-4: DC CHARACTERISTICS: POWER-DOWN CURRENT (I_{PD})

DC CHARACTERISTICS			Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ T_A ≤ +125°C for Extended		
Param. No.	**Typical(2)**	**Maximum(5)**	**Units**	**Conditions**	
Power-Down Current (I_{PD}) (Note 1)					
EDC40m	20	46	mA	+125ºC	Base Power-Down Current
Module Differential Current					
EDC41e	15	50	µA	3.6V	Watchdog Timer Current: ΔI_{WDT} **(Note 3)**
EDC42e	25	50	µA	3.6V	RTCC + Timer1 w/32 kHz Crystal: ΔI_{RTCC} **(Note 3)**
EDC43d	3	3.8	mA	3.6V	ADC: ΔI_{ADC} **(Notes 3, 4)**
EDC44	15	50	µA	3.6V	Deadman Timer Current: ΔI_{DMT} **(Note 3)**

Note 1: The test conditions for I_{PD} current measurements are as follows:

- Oscillator mode is EC (for 8 MHz and below) and EC+PLL (for above 8 MHz) with OSC1 driven by external square wave from rail-to-rail, (OSC1 input clock input over/undershoot < 100 mV required)
- OSC2/CLKO is configured as an I/O input pin
- USB PLL is disabled (USBMD = 1), V_{USB3V3} is connected to V_{SS}
- CPU is in Sleep mode
- L1 Cache and Prefetch modules are disabled
- No peripheral modules are operating, (ON bit = 0), and the associated PMD bit is set. All clocks are disabled ON bit (PBxDIV<15>) = 0 (x ≠ 1,7)
- WDT, DMT, Clock Switching, Fail-Safe Clock Monitor, and Secondary Oscillator are disabled
- All I/O pins are configured as inputs and pulled to V_{SS}
- $\overline{MCLR}$ = V_{DD}
- RTCC and JTAG are disabled
- Voltage regulator is in Stand-by mode (VREGS = 0)

2: Data in the "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

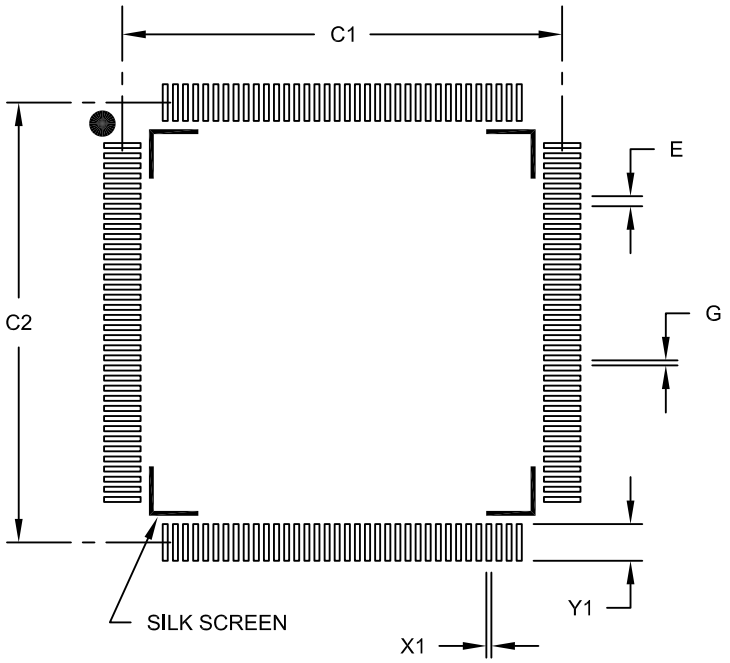
3: The Δ current is the additional current consumed when the module is enabled. This current should be added to the base I_{PD} current.

4: Voltage regulator is operational (VREGS = 1).

5: Data in the "Maximum" column is at 3.3V, +125ºC at specified operating frequency, unless otherwise stated. Parameters are for design guidance only and are not tested.

144-Lead Plastic Thin Quad Flat Pack (PH) - 16x16 mm Body, 2.00 mm Footprint [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.40 BSC	
Contact Pad Spacing	C1		17.40	
Contact Pad Spacing	C2		17.40	
Contact Pad Width (X144)	X1			0.20
Contact Pad Length (X144)	Y1			1.45
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

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TABLE A-3: ADC DIFFERENCES (CONTINUED)

PIC32MX5XX/6XX/7XX Feature	PIC32MZ EF Feature
ADC Calibration	
On PIC32MX devices, the ADC module can be used immediately, once it is enabled.	PIC32MZ devices require a calibration step prior to operation. This is done by copying the calibration data from DEVADCx to the corresponding ADCxCFG register.
I/O Pin Analog Function Selection	
On PIC32MX devices, the analog function of an I/O pin was determined by the PCFGx bit in the AD1PCFG register. PCFGx (AD1PCFG<x>) 1 = Analog input pin in Digital mode 0 = Analog input pin in Analog mode	On PIC32MZ EF devices, the analog selection function has been moved into a separate register on each I/O port. Note that the sense of the bit is different. ANSxy (ANSELx<y>) 1 = Analog input pin in Analog mode 0 = Analog input pin in Digital mode
Electrical Specifications and Timing Requirements	
Refer to **"Section 31. Electrical Characteristics"** in the PIC32MX5XX/6XX/7XX Data Sheet for ADC module specifications and timing requirements.	On PIC32MZ EF devices, the ADC module sampling and conversion time and other specifications have changed. Refer to **37.0 "Electrical Characteristics"** for more information.