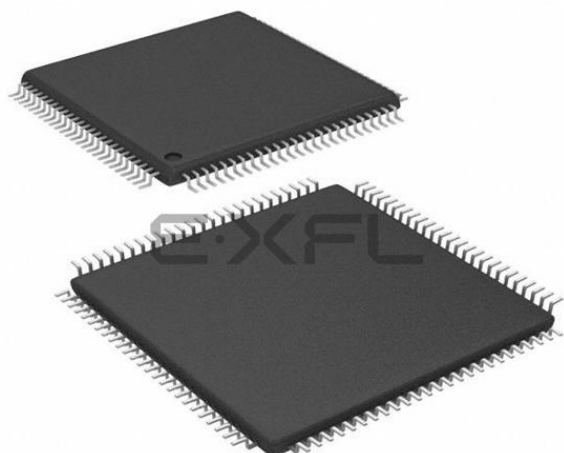




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Details

Product Status	Active
Core Processor	MIPS32® M-Class
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, PMP, SPI, SQI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	78
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	2.1V ~ 3.6V
Data Converters	A/D 40x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mz1024efm100t-i-pf

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

TABLE 5: PIN NAMES FOR 144-PIN DEVICES (CONTINUED)

144-PIN LQFP AND TQFP (TOP VIEW)			
PIC32MZ0512EF(E/F/K)144 PIC32MZ1024EF(G/H/M)144 PIC32MZ1024EF(E/F/K)144 PIC32MZ2048EF(G/H/M)144			
		144	
		1	
Pin Number	Full Pin Name	Pin Number	Full Pin Name
73	VBUS	109	RPD1/SCK1/RD1
74	VUSB3V3	110	EBID14/RPD2/PMD14/RD2
75	VSS	111	EBID15/RPD3/PMD15/RD3
76	D-	112	EBID12/RPD12/PMD12/RD12
77	D+	113	EBID13/PMD13/RD13
78	RPF3/USBID/RF3	114	ETXERR/RJ0
79	SDA3/RPF2/RF2	115	EMDIO/RJ1
80	SCL3/RPF8/RF8	116	EBIRDY3/RJ2
81	ERXD0/RH8	117	EBIA22/RJ3
82	ERXD3/RH9	118	SQICS0/RPD4/RD4
83	ECOL/RH10	119	SQICS1/RPD5/RD5
84	EBIRDY2/RH11	120	ETXEN/RPD6/RD6
85	SCL2/RA2	121	ETXCLK/RPD7/RD7
86	EBIRDY1/SDA2/RA3	122	VDD
87	EBIA14/PMCS1/PMA14/RA4	123	VSS
88	VDD	124	EBID11/RPF0/PMD11/RF0
89	VSS	125	EBID10/RPF1/PMD10/RF1
90	EBIA9/RPF4/SDA5/PMA9/RF4	126	EBIA21/RK7
91	EBIA8/RPF5/SCL5/PMA8/RF5	127	EBID9/RPG1/PMD9/RG1
92	EBIA18/RK4	128	EBID8/RPG0/PMD8/RG0
93	EBIA19/RK5	129	TRCLK/SQICLK/RA6
94	EBIA20/RK6	130	TRD3/SQID3/RA7
95	RPA14/SCL1/RA14	131	EBICS0/RJ4
96	RPA15/SDA1/RA15	132	EBICS1/RJ5
97	EBIA15/RPD9/PMCS2/PMA15/RD9	133	EBICS2/RJ6
98	RPD10/SCK4/RD10	134	EBICS3/RJ7
99	EMDC/RPD11/RD11	135	EBID0/PMD0/RE0
100	ECRS/RH12	136	VSS
101	ERXDV/ECRSV/RH13	137	VDD
102	RH14	138	EBID1/PMD1/RE1
103	EBIA23/RH15	139	TRD2/SQID2/RG14
104	RPD0/RTCC/INT0/RD0	140	TRD1/SQID1/RG12
105	SOSCI/IPC13/RC13	141	TRD0/SQID0/RG13
106	SOSCO/IPC14/T1CK/RC14	142	EBID2/PMD2/RE2
107	VDD	143	EBID3/RPE3/PMD3/RE3
108	VSS	144	EBID4/AN18/PMD4/RE4

Note	1: The RPN pins can be used by remappable peripherals. See Table 1 for the available peripherals and Section 12.4 “Peripheral Pin Select (PPS)” for restrictions. 2: Every I/O port pin (RAX-RKx) can be used as a change notification pin (CNAX-CNKx). See Section 12.0 “I/O Ports” for more information. 3: Shaded pins are 5V tolerant.
-------------	---

TABLE 4-21: SYSTEM BUS TARGET 13 REGISTER MAP

Virtual Address (BF8F_#)	Register Name	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	
B420	SBT13ELOG1	31:16	MULTI	—	—	—	CODE<3:0>				—	—	—	—	—	—	—	0000
		15:0	INITID<7:0>							REGION<3:0>				—	CMD<2:0>			0000
B424	SBT13ELOG2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	GROUP<1:0>		0000
B428	SBT13ECON	31:16	—	—	—	—	—	—	—	ERRP	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
B430	SBT13ECLRS	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
B438	SBT13ECLRM	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
B440	SBT13REG0	31:16	BASE<21:6>															xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—
B450	SBT13RD0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0
B458	SBT13WR0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note: For reset values listed as 'xxxx', please refer to Table 4-6 for the actual reset values.

TABLE 7-2: INTERRUPT IRQ, VECTOR, AND BIT LOCATION (CONTINUED)

Interrupt Source ⁽¹⁾	XC32 Vector Name	IRQ #	Vector #	Interrupt Bit Location				Persistent Interrupt
				Flag	Enable	Priority	Sub-priority	
I2C3 Master Event	_I2C3_MASTER_VECTOR	162	OFF162<17:1>	IFS5<2>	IEC5<2>	IPC40<20:18>	IPC40<17:16>	Yes
SPI4 Fault	_SPI4_FAULT_VECTOR	163	OFF163<17:1>	IFS5<3>	IEC5<3>	IPC40<28:26>	IPC40<25:24>	Yes
SPI4 Receive Done	_SPI4_RX_VECTOR	164	OFF164<17:1>	IFS5<4>	IEC5<4>	IPC41<4:2>	IPC41<1:0>	Yes
SPI4 Transfer Done	_SPI4_TX_VECTOR	165	OFF165<17:1>	IFS5<5>	IEC5<5>	IPC41<12:10>	IPC41<9:8>	Yes
Real Time Clock	_RTCC_VECTOR	166	OFF166<17:1>	IFS5<6>	IEC5<6>	IPC41<20:18>	IPC41<17:16>	No
Flash Control Event	_FLASH_CONTROL_VECTOR	167	OFF167<17:1>	IFS5<7>	IEC5<7>	IPC41<28:26>	IPC41<25:24>	No
Prefetch Module SEC Event	_PREFETCH_VECTOR	168	OFF168<17:1>	IFS5<8>	IEC5<8>	IPC42<4:2>	IPC42<1:0>	Yes
SQ11 Event	_SQ11_VECTOR	169	OFF169<17:1>	IFS5<9>	IEC5<9>	IPC42<12:10>	IPC42<9:8>	Yes
UART4 Fault	_UART4_FAULT_VECTOR	170	OFF170<17:1>	IFS5<10>	IEC5<10>	IPC42<20:18>	IPC42<17:16>	Yes
UART4 Receive Done	_UART4_RX_VECTOR	171	OFF171<17:1>	IFS5<11>	IEC5<11>	IPC42<28:26>	IPC42<25:24>	Yes
UART4 Transfer Done	_UART4_TX_VECTOR	172	OFF172<17:1>	IFS5<12>	IEC5<12>	IPC43<4:2>	IPC43<1:0>	Yes
I2C4 Bus Collision Event	_I2C4_BUS_VECTOR	173	OFF173<17:1>	IFS5<13>	IEC5<13>	IPC43<12:10>	IPC43<9:8>	Yes
I2C4 Slave Event	_I2C4_SLAVE_VECTOR	174	OFF174<17:1>	IFS5<14>	IEC5<14>	IPC43<20:18>	IPC43<17:16>	Yes
I2C4 Master Event	_I2C4_MASTER_VECTOR	175	OFF175<17:1>	IFS5<15>	IEC5<15>	IPC43<28:26>	IPC43<25:24>	Yes
SPI5 Fault ⁽²⁾	_SPI5_FAULT_VECTOR	176	OFF176<17:1>	IFS5<16>	IEC5<16>	IPC44<4:2>	IPC44<1:0>	Yes
SPI5 Receive Done ⁽²⁾	_SPI5_RX_VECTOR	177	OFF177<17:1>	IFS5<17>	IEC5<17>	IPC44<12:10>	IPC44<9:8>	Yes
SPI5 Transfer Done ⁽²⁾	_SPI5_TX_VECTOR	178	OFF178<17:1>	IFS5<18>	IEC5<18>	IPC44<20:18>	IPC44<17:16>	Yes
UART5 Fault	_UART5_FAULT_VECTOR	179	OFF179<17:1>	IFS5<19>	IEC5<19>	IPC44<28:26>	IPC44<25:24>	Yes
UART5 Receive Done	_UART5_RX_VECTOR	180	OFF180<17:1>	IFS5<20>	IEC5<20>	IPC45<4:2>	IPC45<1:0>	Yes
UART5 Transfer Done	_UART5_TX_VECTOR	181	OFF181<17:1>	IFS5<21>	IEC5<21>	IPC45<12:10>	IPC45<9:8>	Yes
I2C5 Bus Collision Event	_I2C5_BUS_VECTOR	182	OFF182<17:1>	IFS5<22>	IEC5<22>	IPC45<20:18>	IPC45<17:16>	Yes
I2C5 Slave Event	_I2C5_SLAVE_VECTOR	183	OFF183<17:1>	IFS5<23>	IEC5<23>	IPC45<28:26>	IPC45<25:24>	Yes
I2C5 Master Event	_I2C5_MASTER_VECTOR	184	OFF184<17:1>	IFS5<24>	IEC5<24>	IPC46<4:2>	IPC46<1:0>	Yes
SPI6 Fault ⁽²⁾	_SPI6_FAULT_VECTOR	185	OFF185<17:1>	IFS5<25>	IEC5<25>	IPC46<12:10>	IPC46<9:8>	Yes
SPI6 Receive Done ⁽²⁾	_SPI6_RX_VECTOR	186	OFF186<17:1>	IFS5<26>	IEC5<26>	IPC46<20:18>	IPC46<17:16>	Yes
SPI6 Transfer Done ⁽²⁾	_SPI6_TX_VECTOR	187	OFF187<17:1>	IFS5<27>	IEC5<27>	IPC46<28:26>	IPC46<25:24>	Yes
UART6 Fault	_UART6_FAULT_VECTOR	188	OFF188<17:1>	IFS5<28>	IEC5<28>	IPC47<4:2>	IPC47<1:0>	Yes
UART6 Receive Done	_UART6_RX_VECTOR	189	OFF189<17:1>	IFS5<29>	IEC5<29>	IPC47<12:10>	IPC47<9:8>	Yes

Note 1: Not all interrupt sources are available on all devices. See **TABLE 1: "PIC32MZ EF Family Features"** for the list of available peripherals.

2: This interrupt source is not available on 64-pin devices.

3: This interrupt source is not available on 100-pin devices.

4: This interrupt source is not available on 124-pin devices.

TABLE 7-2: INTERRUPT IRQ, VECTOR, AND BIT LOCATION (CONTINUED)

Interrupt Source ⁽¹⁾	XC32 Vector Name	IRQ #	Vector #	Interrupt Bit Location				Persistent Interrupt
				Flag	Enable	Priority	Sub-priority	
UART6 Transfer Done	_UART6_TX_VECTOR	190	OFF190<17:1>	IFS5<30>	IEC5<30>	IPC47<20:18>	IPC47<17:16>	Yes
Reserved	—	191	—	—	—	—	—	—
ADC End of Scan Ready	_ADC_EOS_VECTOR	192	OFF192<17:1>	IFS6<0>	IEC6<0>	IPC48<4:2>	IPC48<1:0>	Yes
ADC Analog Circuits Ready	_ADC_ARDY_VECTOR	193	OFF193<17:1>	IFS6<1>	IEC6<1>	IPC48<12:10>	IPC48<9:8>	Yes
ADC Update Ready	_ADC_URDY_VECTOR	194	OFF194<17:1>	IFS6<2>	IEC6<2>	IPC48<20:18>	IPC48<17:16>	Yes
Reserved	—	195	—	—	—	—	—	—
ADC Group Early Interrupt Request	_ADC_EARLY_VECTOR	196	OFF196<17:1>	IFS6<4>	IEC6<4>	IPC49<4:2>	IPC49<1:0>	Yes
Reserved	—	197	—	—	—	—	—	—
ADC0 Early Interrupt	_ADC0_EARLY_VECTOR	198	OFF198<17:1>	IFS6<6>	IEC6<6>	IPC49<20:18>	IPC49<17:16>	Yes
ADC1 Early Interrupt	_ADC1_EARLY_VECTOR	199	OFF199<17:1>	IFS6<7>	IEC6<7>	IPC49<28:26>	IPC49<25:24>	Yes
ADC2 Early Interrupt	_ADC2_EARLY_VECTOR	200	OFF200<17:1>	IFS6<8>	IEC6<8>	IPC50<4:2>	IPC50<1:0>	Yes
ADC3 Early Interrupt	_ADC2_EARLY_VECTOR	201	OFF201<17:1>	IFS6<9>	IEC6<9>	IPC50<12:10>	IPC50<9:8>	Yes
ADC4 Early Interrupt	_ADC4_EARLY_VECTOR	202	OFF202<17:1>	IFS6<10>	IEC6<10>	IPC50<20:18>	IPC50<17:16>	Yes
Reserved	—	203	—	—	—	—	—	—
Reserved	—	204	—	—	—	—	—	—
ADC7 Early Interrupt	_ADC7_EARLY_VECTOR	205	OFF205<17:1>	IFS6<13>	IEC6<13>	IPC51<12:10>	IPC51<9:8>	Yes
ADC0 Warm Interrupt	_ADC0_WARM_VECTOR	206	OFF206<17:1>	IFS6<14>	IEC6<14>	IPC51<20:18>	IPC51<17:16>	Yes
ADC1 Warm Interrupt	_ADC1_WARM_VECTOR	207	OFF207<17:1>	IFS6<15>	IEC6<15>	IPC51<28:26>	IPC51<25:24>	Yes
ADC2 Warm Interrupt	_ADC2_WARM_VECTOR	208	OFF208<17:1>	IFS6<16>	IEC6<16>	IPC52<4:2>	IPC52<1:0>	Yes
ADC3 Warm Interrupt	_ADC3_WARM_VECTOR	209	OFF209<17:1>	IFS6<17>	IEC6<17>	IPC52<12:10>	IPC52<9:8>	Yes
ADC4 Warm Interrupt	_ADC4_WARM_VECTOR	210	OFF210<17:1>	IFS6<18>	IEC6<18>	IPC52<20:18>	IPC52<17:16>	Yes
Reserved	—	211	—	—	—	—	—	—
Reserved	—	212	—	—	—	—	—	—
ADC7 Warm Interrupt	_ADC7_WARM_VECTOR	213	OFF213<17:1>	IFS6<21>	IEC6<21>	IPC53<12:10>	IPC53<9:8>	Yes
Lowest Natural Order Priority								

Note 1: Not all interrupt sources are available on all devices. See **TABLE 1: “PIC32MZ EF Family Features”** for the list of available peripherals.

- 2:** This interrupt source is not available on 64-pin devices.
3: This interrupt source is not available on 100-pin devices.
4: This interrupt source is not available on 124-pin devices.

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

REGISTER 7-3: INTSTAT: INTERRUPT STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	R-0	R-0	R-0
	—	—	—	—	—	SRIPL<2:0> ⁽¹⁾		
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	SIRQ<7:0>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-11 **Unimplemented:** Read as '0'

bit 10-8 **SRIPL<2:0>:** Requested Priority Level bits for Single Vector Mode bits⁽¹⁾

111-000 = The priority level of the latest interrupt presented to the CPU

bit 7-6 **Unimplemented:** Read as '0'

bit 7-0 **SIRQ<7:0>:** Last Interrupt Request Serviced Status bits

11111111-00000000 = The last interrupt request number serviced by the CPU

Note 1: This value should only be used when the interrupt controller is configured for Single Vector mode.

REGISTER 7-4: IPTMR: INTERRUPT PROXIMITY TIMER REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IPTMR<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IPTMR<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IPTMR<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IPTMR<7:0>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-0 **IPTMR<31:0>:** Interrupt Proximity Timer Reload bits

Used by the Interrupt Proximity Timer as a reload value when the Interrupt Proximity timer is triggered by an interrupt event.

9.1 Prefetch Control Registers

TABLE 9-1: PREFETCH REGISTER MAP

Virtual Address (BF8E_#)	Register Name ⁽¹⁾	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0000	PRECON	31:16	—	—	—	—	—	PFMSECEN	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	PREFEN<1:0>		—	PFMWS<2:0>			0007
0010	PRESTAT	31:16	—	—	—	—	PFMDDED	PFMSEC	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	PFMSECCNT<7:0>								0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 “CLR, SET, and INV Registers”** for more information.

TABLE 12-23: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP (CONTINUED)

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
15B4	RPC13R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPC13R<3:0>				0000
15B8	RPC14R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPC14R<3:0>				0000
15C0	RPD0R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPD0R<3:0>				0000
15C4	RPD1R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPD1R<3:0>				0000
15C8	RPD2R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPD2R<3:0>				0000
15CC	RPD3R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPD3R<3:0>				0000
15D0	RPD4R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPD4R<3:0>				0000
15D4	RPD5R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPD5R<3:0>				0000
15D8	RPD6R ⁽²⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPD6R<3:0>				0000
15DC	RPD7R ⁽²⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPD7R<3:0>				0000
15E4	RPD9R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPD9R<3:0>				0000
15E8	RPD10R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPD10R<3:0>				0000
15EC	RPD11R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPD11R<3:0>				0000
15F0	RPD12R ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPD12R<3:0>				0000
15F8	RPD14R ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPD14R<3:0>				0000
15FC	RPD15R ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPD15R<3:0>				0000
160C	RPE3R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPE3R<3:0>				0000
1614	RPE5R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPE5R<3:0>				0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

- Note** 1: This register is not available on 64-pin devices.
 2: This register is not available on 64-pin and 100-pin devices.

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

REGISTER 15-4: DMTSTAT: DEADMAN TIMER STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R-0, HC, HS	R-0, HC, HS	R-0, HC, HS	U-0	U-0	U-0	U-0	R-0, HC, HS
	BAD1	BAD2	DMTEVENT	—	—	—	—	WINOPN

Legend:

R = Readable bit

-n = Value at POR

HC = Hardware Cleared

W = Writable bit

'1' = Bit is set

HS = Hardware Set

U = Unimplemented bit, read as '0'

'0' = Bit is cleared

x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **BAD1:** Bad STEP1<7:0> Value Detect bit

1 = Incorrect STEP1<7:0> value was detected

0 = Incorrect STEP1<7:0> value was not detected

bit 6 **BAD2:** Bad STEP2<7:0> Value Detect bit

1 = Incorrect STEP2<7:0> value was detected

0 = Incorrect STEP2<7:0> value was not detected

bit 5 **DMTEVENT:** Deadman Timer Event bit

1 = Deadman timer event was detected (counter expired or bad STEP1<7:0> or STEP2<7:0> value was entered prior to counter increment)

0 = Deadman timer even was not detected

bit 4-1 **Unimplemented:** Read as '0'

bit 0 **WINOPN:** Deadman Timer Clear Window bit

1 = Deadman timer clear window is open

0 = Deadman timer clear window is not open

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

REGISTER 21-2: I2CxSTAT: I²C STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —
23:16	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —
15:8	R-0, HS, HC ACKSTAT	R-0, HS, HC TRSTAT	R/C-0, HS, HC ACKTIM	U-0 —	U-0 —	R/C-0, HS BCL	R-0, HS, HC GCSTAT	R-0, HS, HC ADD10
7:0	R/C-0, HS, SC IWCOL	R/C-0, HS, SC I2COV	R-0, HS, HC D_A	R/C-0, HS, HC P	R/C-0, HS, HC S	R-0, HS, HC R_W	R-0, HS, HC RBF	R-0, HS, HC TBF

Legend:	HS = Hardware Set	HC = Hardware Cleared	SC = Software Cleared
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	C = Clearable bit

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ACKSTAT:** Acknowledge Status bit
(when operating as I²C master, applicable to master transmit operation)
1 = NACK received from slave
0 = ACK received from slave
Hardware set or clear at end of slave Acknowledge.

bit 14 **TRSTAT:** Transmit Status bit (when operating as I²C master, applicable to master transmit operation)
1 = Master transmit is in progress (8 bits + ACK)
0 = Master transmit is not in progress
Hardware set at beginning of master transmission. Hardware clear at end of slave Acknowledge.

bit 13 **ACKTIM:** Acknowledge Time Status bit (Valid in I²C Slave mode only)
1 = I²C bus is in an Acknowledge sequence, set on the eight falling edge of SCL clock
0 = Not an Acknowledge sequence, cleared on 9th rising edge of SCL clock

bit 12-11 **Unimplemented:** Read as '0'

bit 10 **BCL:** Master Bus Collision Detect bit
1 = A bus collision has been detected during a master operation
0 = No collision
Hardware set at detection of bus collision.

bit 9 **GCSTAT:** General Call Status bit
1 = General call address was received
0 = General call address was not received
Hardware set when address matches general call address. Hardware clear at Stop detection.

bit 8 **ADD10:** 10-bit Address Status bit
1 = 10-bit address was matched
0 = 10-bit address was not matched
Hardware set at match of 2nd byte of matched 10-bit address. Hardware clear at Stop detection.

bit 7 **IWCOL:** Write Collision Detect bit
1 = An attempt to write the I2CxTRN register failed because the I²C module is busy
0 = No collision
Hardware set at occurrence of write to I2CxTRN while busy (cleared by software).

bit 6 **I2COV:** Receive Overflow Flag bit
1 = A byte was received while the I2CxRCV register is still holding the previous byte
0 = No overflow
Hardware set at attempt to transfer I2CxRSR to I2CxRCV (cleared by software).

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

REGISTER 23-3: PMADDR: PARALLEL PORT ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CS2 ⁽¹⁾	CS1 ⁽³⁾	ADDR<13:8>					
	ADDR15 ⁽²⁾	ADDR14 ⁽⁴⁾						
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ADDR<7:0>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **CS2:** Chip Select 2 bit⁽¹⁾

1 = Chip Select 2 is active

0 = Chip Select 2 is inactive

bit 15 **ADDR<15>:** Target Address bit 15⁽²⁾

bit 14 **CS1:** Chip Select 1 bit⁽³⁾

1 = Chip Select 1 is active

0 = Chip Select 1 is inactive

bit 14 **ADDR<14>:** Target Address bit 14⁽⁴⁾

bit 13-0 **ADDR<13:0>:** Address bits

Note 1: When the CSF<1:0> bits (PMCON<7:6>) = 10 or 01.

2: When the CSF<1:0> bits (PMCON<7:6>) = 00.

3: When the CSF<1:0> bits (PMCON<7:6>) = 10.

4: When the CSF<1:0> bits (PMCON<7:6>) = 00 or 01.

Note: If the DUALBUF bit (PMCON<17>) = 0, the bits in this register control both read and write target addressing. If the DUALBUF bit = 1, the bits in this register are not used. In this instance, use the PMRADDR register for Read operations and the PMWADDR register for Write operations.

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

REGISTER 26-3: CEBDADDR: CRYPTO ENGINE BUFFER DESCRIPTOR REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	BDPADDR<31:24>							
23:16	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	BDPADDR<23:16>							
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	BDPADDR<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	BDPADDR<7:0>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-0 **BDPADDR<31:0>**: Current Buffer Descriptor Process Address Status bits

These bits contain the current descriptor address that is being processed by the Buffer Descriptor Processor (BDP).

REGISTER 26-4: CEBDPADDR: CRYPTO ENGINE BUFFER DESCRIPTOR PROCESSOR REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BASEADDR<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BASEADDR<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BASEADDR<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BASEADDR<7:0>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-0 **BASEADDR<31:0>**: Buffer Descriptor Base Address bits

These bits contain the physical address of the first Buffer Descriptor in the Buffer Descriptor chain. When enabled, the Crypto DMA begins fetching Buffer Descriptors from this address.

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

REGISTER 26-6: CEINTSRC: CRYPTO ENGINE INTERRUPT SOURCE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	R-0	R-0	R-0	R-0
	—	—	—	—	AREIF	PKTIF	CBDIF	PENDIF

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-4 **Unimplemented:** Read as '0'

bit 3 **AREIF:** Access Response Error Interrupt bit

1 = Error occurred trying to access memory outside the Crypto Engine

0 = No error has occurred

bit 2 **PKTIF:** DMA Packet Completion Interrupt Status bit

1 = DMA packet was completed

0 = DMA packet was not completed

bit 1 **CBDIF:** BD Transmit Status bit

1 = Last BD transmit was processed

0 = Last BD transmit has not been processed

bit 0 **PENDIF:** Crypto Engine Interrupt Pending Status bit

1 = Crypto Engine interrupt is pending (this value is the result of an OR of all interrupts in the Crypto Engine)

0 = Crypto Engine interrupt is not pending

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

REGISTER 28-12: ADCDSTAT1: ADC DATA READY STATUS REGISTER 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0, HS, HC ARDY31 ⁽¹⁾	R-0, HS, HC ARDY30 ⁽¹⁾	R-0, HS, HC ARDY29 ⁽¹⁾	R-0, HS, HC ARDY28 ⁽¹⁾	R-0, HS, HC ARDY27 ⁽¹⁾	R-0, HS, HC ARDY26 ⁽¹⁾	R-0, HS, HC ARDY25 ⁽¹⁾	R-0, HS, HC ARDY24 ⁽¹⁾
23:16	R-0, HS, HC ARDY23 ⁽¹⁾	R-0, HS, HC ARDY22 ⁽¹⁾	R-0, HS, HC ARDY21 ⁽¹⁾	R-0, HS, HC ARDY20 ⁽¹⁾	R-0, HS, HC ARDY19 ⁽¹⁾	R-0, HS, HC ARDY18	R-0, HS, HC ARDY17	R-0, HS, HC ARDY16
15:8	R-0, HS, HC ARDY15	R-0, HS, HC ARDY14	R-0, HS, HC ARDY13	R-0, HS, HC ARDY12	R-0, HS, HC ARDY11	R-0, HS, HC ARDY10	R-0, HS, HC ARDY9	R-0, HS, HC ARDY8
7:0	R-0, HS, HC ARDY7	R-0, HS, HC ARDY6	R-0, HS, HC ARDY5	R-0, HS, HC ARDY4	R-0, HS, HC ARDY3	R-0, HS, HC ARDY2	R-0, HS, HC ARDY1	R-0, HS, HC ARDY0

Legend: HS = Hardware Set HC = Hardware Cleared
R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-0 **ARDY31:ARDY0:** Conversion Data Ready for Corresponding Analog Input Ready bits

1 = This bit is set when converted data is ready in the data register

0 = This bit is cleared when the associated data register is read

Note 1: This bit is not available on 64-pin devices.

REGISTER 28-13: ADCDSTAT2: ADC DATA READY STATUS REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —
23:16	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —
15:8	U-0 —	U-0 —	U-0 —	R-0, HS, HC ARDY44	R-0, HS, HC ARDY43	R-0, HS, HC ARDY42 ⁽²⁾	R-0, HS, HC ARDY41 ⁽²⁾	R-0, HS, HC ARDY40 ⁽²⁾
7:0	R-0, HS, HC ARDY39 ⁽²⁾	R-0, HS, HC ARDY38 ⁽²⁾	R-0, HS, HC ARDY37 ⁽²⁾	R-0, HS, HC ARDY36 ⁽²⁾	R-0, HS, HC ARDY35 ⁽²⁾	R-0, HS, HC ARDY34 ⁽¹⁾	R-0, HS, HC ARDY33 ⁽¹⁾	R-0, HS, HC ARDY32 ⁽¹⁾

Legend: HS = Hardware Set HC = Hardware Cleared
R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-13 **Unimplemented:** Read as '0'

bit 12-0 **ARDY44:ARDY32:** Conversion Data Ready for Corresponding Analog Input Ready bits

1 = This bit is set when converted data is ready in the data register

0 = This bit is cleared when the associated data register is read

Note 1: This bit is not available on 64-pin devices.

2: This bit is not available on 64-pin and 100-pin devices.

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

**REGISTER 28-14: ADCCMPENx: ADC DIGITAL COMPARATOR 'x' ENABLE REGISTER
(‘x’ = 1 THROUGH 6)**

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0 CMPE31 ⁽¹⁾	R/W-0 CMPE30 ⁽¹⁾	R/W-0 CMPE29 ⁽¹⁾	R/W-0 CMPE28 ⁽¹⁾	R/W-0 CMPE27 ⁽¹⁾	R/W-0 CMPE26 ⁽¹⁾	R/W-0 CMPE25 ⁽¹⁾	R/W-0 CMPE24 ⁽¹⁾
23:16	R/W-0 CMPE23 ⁽¹⁾	R/W-0 CMPE22 ⁽¹⁾	R/W-0 CMPE21 ⁽¹⁾	R/W-0 CMPE20 ⁽¹⁾	R/W-0 CMPE19 ⁽¹⁾	R/W-0 CMPE18	R/W-0 CMPE17	R/W-0 CMPE16
15:8	R/W-0 CMPE15	R/W-0 CMPE14	R/W-0 CMPE13	R/W-0 CMPE12	R/W-0 CMPE11	R/W-0 CMPE10	R/W-0 CMPE9	R/W-0 CMPE8
7:0	R/W-0 CMPE7	R/W-0 CMPE6	R/W-0 CMPE5	R/W-0 CMPE4	R/W-0 CMPE3	R/W-0 CMPE2	R/W-0 CMPE1	R/W-0 CMPE0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-0 **CMPE31:CMPE0**: ADC Digital Comparator 'x' Enable bits^(2,3)

These bits enable conversion results corresponding to the Analog Input to be processed by the Digital Comparator. CMPE0 enables AN0, CMPE1 enables AN1, and so on.

Note 1: This bit is not available on 64-pin devices.

2: CMPE_x = AN_x, where 'x' = 0-31 (Digital Comparator inputs are limited to AN0 through AN31).

3: Changing the bits in this register while the Digital Comparator is enabled (ENDCMP = 1) can result in unpredictable behavior.

REGISTER 28-21: ADCCMPCONx: ADC DIGITAL COMPARATOR 'x' CONTROL REGISTER ('x' = 2 THROUGH 6) (CONTINUED)

- bit 1 **IELOHI:** Low/High Digital Comparator 'x' Event bit
 1 = Generate a Digital Comparator 'x' Event when the DCMPL0<15:0> bits $\leq$ DATA<31:0> bits
 0 = Do not generate an event
- bit 0 **IELOLO:** Low/Low Digital Comparator 'x' Event bit
 1 = Generate a Digital Comparator 'x' Event when the DATA<31:0> bits < DCMPL0<15:0> bits
 0 = Do not generate an event

REGISTER 29-10: CifLTCON0: CAN FILTER CONTROL REGISTER 0 (CONTINUED)

bit 15	FLTEN1: Filter 1 Enable bit 1 = Filter is enabled 0 = Filter is disabled
bit 14-13	MSEL1<1:0>: Filter 1 Mask Select bits 11 = Acceptance Mask 3 selected 10 = Acceptance Mask 2 selected 01 = Acceptance Mask 1 selected 00 = Acceptance Mask 0 selected
bit 12-8	FSEL1<4:0>: FIFO Selection bits 11111 = Message matching filter is stored in FIFO buffer 31 11110 = Message matching filter is stored in FIFO buffer 30 • • • 00001 = Message matching filter is stored in FIFO buffer 1 00000 = Message matching filter is stored in FIFO buffer 0
bit 7	FLTEN0: Filter 0 Enable bit 1 = Filter is enabled 0 = Filter is disabled
bit 6-5	MSEL0<1:0>: Filter 0 Mask Select bits 11 = Acceptance Mask 3 selected 10 = Acceptance Mask 2 selected 01 = Acceptance Mask 1 selected 00 = Acceptance Mask 0 selected
bit 4-0	FSEL0<4:0>: FIFO Selection bits 11111 = Message matching filter is stored in FIFO buffer 31 11110 = Message matching filter is stored in FIFO buffer 30 • • • 00001 = Message matching filter is stored in FIFO buffer 1 00000 = Message matching filter is stored in FIFO buffer 0

Note: The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

REGISTER 30-29: EMAC1SUPP: ETHERNET CONTROLLER MAC PHY SUPPORT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	R/W-0	U-0	U-0	R/W-0
	—	—	—	—	RESETRMII ⁽¹⁾	—	—	SPEEDRMII ⁽¹⁾
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-12 **Unimplemented:** Read as '0'

bit 11 **RESETRMII:** Reset RMII Logic bit⁽¹⁾

1 = Reset the MAC RMII module

0 = Normal operation.

bit 10-9 **Unimplemented:** Read as '0'

bit 8 **SPEEDRMII:** RMII Speed bit⁽¹⁾

This bit configures the Reduced MII logic for the current operating speed.

1 = RMII is running at 100 Mbps

0 = RMII is running at 10 Mbps

bit 7-0 **Unimplemented:** Read as '0'

Note 1: This bit is only used for the RMII module.

Note: Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware.

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

REGISTER 30-31: EMAC1MCFG: ETHERNET CONTROLLER MAC MII MANAGEMENT CONFIGURATION REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	RESETMGMT	—	—	—	—	—	—	—
7:0	U-0	U-0	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	CLKSEL<3:0> ⁽¹⁾				NOPRE	SCANINC

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **RESETMGMT:** Test Reset MII Management bit
1 = Reset the MII Management module
0 = Normal Operation

bit 14-6 **Unimplemented:** Read as '0'

bit 5-2 **CLKSEL<3:0>:** MII Management Clock Select 1 bits⁽¹⁾

These bits are used by the clock divide logic in creating the MII Management Clock (MDC), which the IEEE 802.3 Specification defines to be no faster than 2.5 MHz. Some PHYs support clock rates up to 12.5 MHz.

bit 1 **NOPRE:** Suppress Preamble bit
1 = The MII Management will perform read/write cycles without the 32-bit preamble field. Some PHYs support suppressed preamble
0 = Normal read/write cycles are performed

bit 0 **SCANINC:** Scan Increment bit
1 = The MII Management module will perform read cycles across a range of PHYs. The read cycles will start from address 1 through the value set in EMAC1MADR<PHYADDR>
0 = Continuous reads of the same PHY

Note 1: Table 30-7 provides a description of the clock divider encoding.

Note: Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware.

TABLE 30-7: MIIM CLOCK SELECTION

MIIM Clock Select	EMAC1MCFG<5:2>
TPBCLK5 divided by 4	000x
TPBCLK5 divided by 6	0010
TPBCLK5 divided by 8	0011
TPBCLK5 divided by 10	0100
TPBCLK5 divided by 14	0101
TPBCLK5 divided by 20	0110
TPBCLK5 divided by 28	0111
TPBCLK5 divided by 40	1000
TPBCLK5 divided by 48	1001
TPBCLK5 divided by 50	1010
Undefined	Any other combination

TABLE 34-3: DEVICE ID, REVISION, AND CONFIGURATION SUMMARY

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets ⁽¹⁾
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0000	CFGCON	31:16	—	—	—	—	—	—	DMAPRI	CPUPRI	—	—	—	—	—	—	ICACLK	OCACLK	0000
		15:0	—	—	IOLOCK	PMDLOCK	PGLOCK	—	—	USBSSSEN	IOANCPEN	—	ECCCON<1:0>		JTAGEN	TROEN	—	TDOEN	000B
0020	DEVID	31:16	VER<3:0>					DEVID<27:16>											XXXX
		15:0	DEVID<15:0>																XXXX
0030	SYSKEY	31:16	SYSKEY<31:0>																0000
		15:0																	0000
00C0	CFGEBIA ⁽²⁾	31:16	EBIPINEN	—	—	—	—	—	—	—	EBIA23EN	EBIA22EN	EBIA21EN	EBIA20EN	EBIA19EN	EBIA18EN	EBIA17EN	EBIA16EN	0000
		15:0	EBIA15EN	EBIA14EN	EBIA13EN	EBIA12EN	EBIA11EN	EBIA10EN	EBIA9EN	EBIA8EN	EBIA7EN	EBIA6EN	EBIA5EN	EBIA4EN	EBIA3EN	EBIA2EN	EBIA1EN	EBIA0EN	0000
00D0	CFGEBIC ⁽²⁾	31:16	EBI RDYINV3	EBI RDYINV2	EBI RDYINV1	—	EBI RDYEN3	EBI RDYEN2	EBI RDYEN1	—	—	—	—	—	—	—	EBI RDYLV1	EBIRPEN	0000
		15:0	—	—	EBIWEEN	EBIOEEN	—	—	EBIBSEN1	EBIBSEN0	EBICSEN3	EBICSEN2	EBICSEN1	EBICSEN0	—	—	EBIDEN1	EBIDEN0	0000
00E0	CFGPG	31:16	ICD1PG<1:0>		—	—	—	—	CRYPTPG<1:0>		FCPG<1:0>		SQ1PG<1:0>		—	—	ETHPG<1:0>		0000
		15:0	CAN2PG<1:0>		CAN1PG<1:0>		—	—	USBPG<1:0>		—		—		DMPAG<1:0>		—	—	CPUPG<1:0>

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: Reset values are dependent on the device variant.

Note 2: This register is not available on 64-pin devices.

TABLE 34-4: DEVICE SERIAL NUMBER SUMMARY

Virtual Address (BFC5_#)	Register Name	Bit Range	Bits																All Resets ⁽¹⁾
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
4020	DEVSN0	31:16	Device Serial Number <31:16>																XXXX
		15:0	Device Serial Number <15:0>																XXXX
4024	DEVSN1	31:16	Device Serial Number <31:16>																XXXX
		15:0	Device Serial Number <15:0>																XXXX

Legend: x = unknown value on Reset.

Note 1: Reset values are dependent on the device variant.

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TABLE 37-23: I/O TIMING REQUIREMENTS

AC CHARACTERISTICS		Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended					
Param. No.	Symbol	Characteristics ⁽²⁾	Min.	Typ. ⁽¹⁾	Max.	Units	Conditions
DO31	TioR	Port Output Rise Time I/O Pins: 4x Source Driver Pins - RA3, RA9, RA10, RA14, RA15 RB0-RB2, RB4, RB6-RB7, RB11, RB13 RC12-RC15 RD0, RD6-RD7, RD11, RD14 RE8, RE9 RF2, RF3, RF8 RG15 RH0, RH1, RH4-RH6, RH8-RH13 RJ0-RJ2, RJ8, RJ9, RJ11	—	—	9.5	ns	CLOAD = 50 pF
			—	—	6	ns	CLOAD = 20 pF
		Port Output Rise Time I/O Pins: 8x Source Driver Pins - RA0-RA2, RA4, RA5 RB3, RB5, RB8-RB10, RB12, RB14, RB15 RC1-RC4 RD1-RD5, RD9, RD10, RD12, RD13, RD15 RE4-RE7 RF0, RF4, RF5, RF12, RF13 RG0, RG1, RG6-RG9 RH2, RH3, RH7, RH14, RH15 RJ3-RJ7, RJ10, RJ12-RJ15 RK0-RK7	—	—	8	ns	CLOAD = 50 pF
			—	—	6	ns	CLOAD = 20 pF
		Port Output Rise Time I/O Pins: 12x Source Driver Pins - RA6, RA7 RE0-RE3 RF1 RG12-RG14	—	—	3.5	ns	CLOAD = 50 pF
			—	—	2	ns	CLOAD = 20 pF

Note 1: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

2: This parameter is characterized, but not tested in manufacturing.