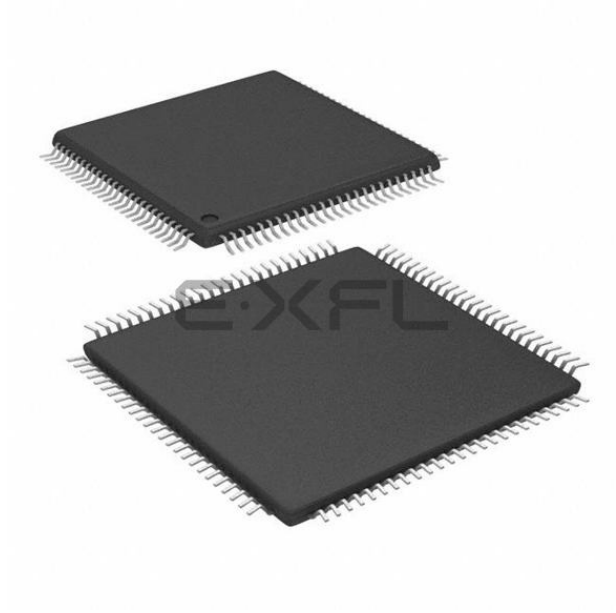
Microchip Technology - PIC32MZ1024EFM100T-I/PT Datasheet



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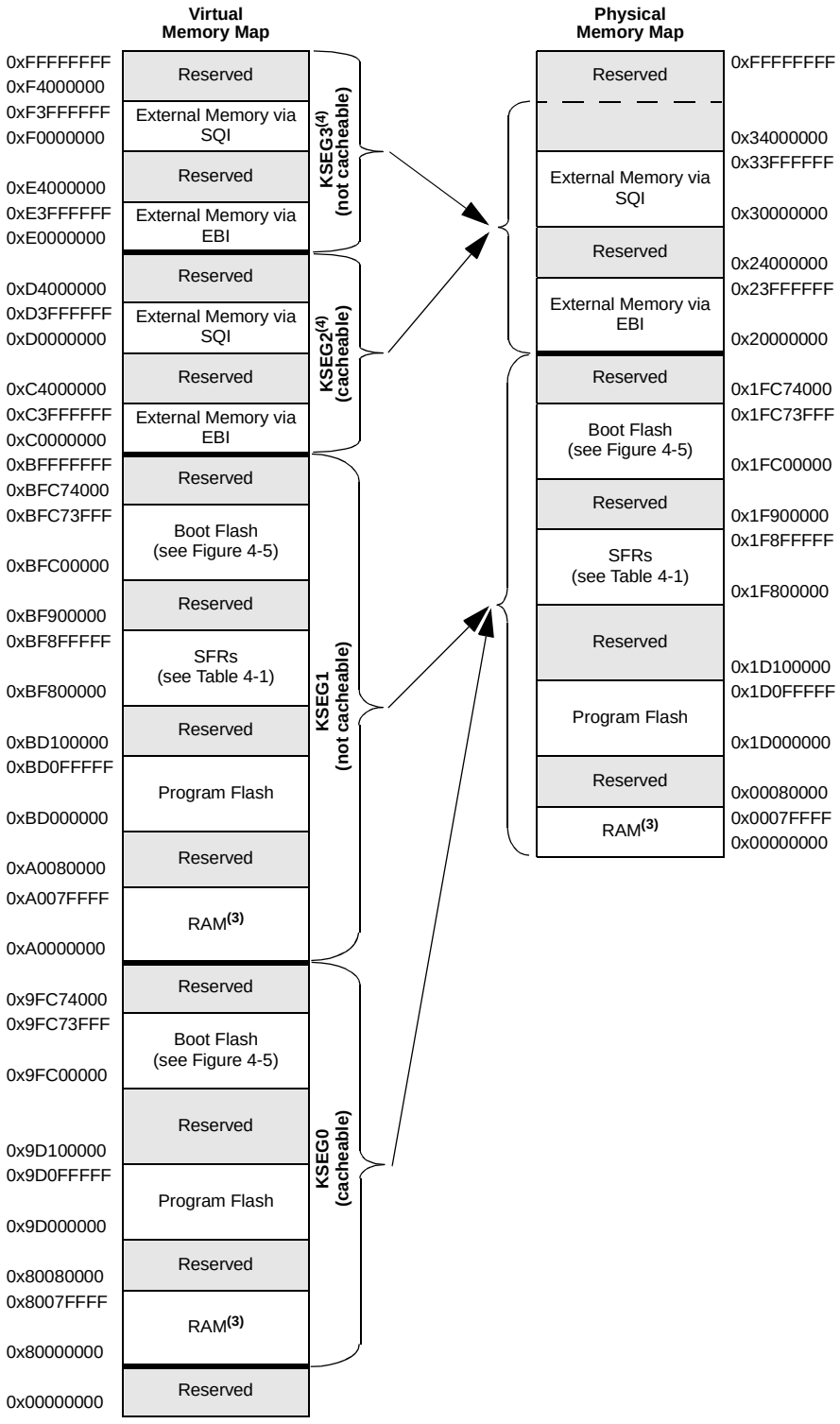
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® M-Class
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, PMP, SPI, SQI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	78
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	2.1V ~ 3.6V
Data Converters	A/D 40x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mz1024efm100t-i-pt

FIGURE 4-3: MEMORY MAP FOR DEVICES WITH 1024 KB OF PROGRAM MEMORY AND 512 KB OF RAM(1,2)



Note 1: Memory areas are not shown to scale.
2: The Cache, MMU, and TLB are initialized by compiler start-up code.
3: RAM memory is divided into two equal banks: RAM Bank 1 and RAM Bank 2 on a half boundary.
4: The MMU must be enabled and the TLB must be set up to access this segment.

REGISTER 5-1: NVMCON: FLASH PROGRAMMING CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0, HC	R/W-0	R-0, HS, HC	R-0, HS, HC	U-0	U-0	U-0	U-0
	WR(1)	WREN(1)	WRERR(1)	LVDERR(1)	—	—	—	—
7:0	R/W-0	R/W-x	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	PFSWAP	BFSWAP	—	—	NVMOP<3:0>			

Legend:	HC = Hardware Set	HC = Hardware Cleared	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **WR:** Write Control bit(1)

This bit cannot be cleared and can be set only when WREN = 1 and the unlock sequence has been performed.
1 = Initiate a Flash operation
0 = Flash operation is complete or inactive

bit 14 **WREN:** Write Enable bit(1)
1 = Enable writes to the WR bit and disables writes to the NVMOP<3:0> bits
0 = Disable writes to WR bit and enables writes to the NVMOP<3:0> bits

bit 13 **WRERR:** Write Error bit(1)

This bit can be cleared only by setting the NVMOP<3:0> bits = 0000 and initiating a Flash operation.
1 = Program or erase sequence did not complete successfully
0 = Program or erase sequence completed normally

bit 12 **LVDERR:** Low-Voltage Detect Error bit(1)

This bit can be cleared only by setting the NVMOP<3:0> bits = 0000 and initiating a Flash operation.
1 = Low-voltage detected (possible data corruption, if WRERR is set)
0 = Voltage level is acceptable for programming

bit 11-8 **Unimplemented:** Read as '0'

bit 7 **PFSWAP:** Program Flash Bank Swap Control bit

This bit is only writable when WREN = 0 and the unlock sequence has been performed.
1 = Program Flash Bank 2 is mapped to the lower mapped region and program Flash Bank 1 is mapped to the upper mapped region
0 = Program Flash Bank 1 is mapped to the lower mapped region and program Flash Bank 2 is mapped to the upper mapped region

Note 1: These bits are only reset by a Power-on Reset (POR) and are not affected by other reset sources.

2: This operation results in a "no operation" (NOP) when the Dynamic Flash ECC Configuration bits = 00 (FECCCON<1:0> (DVCFG0<9:8>)), which enables ECC at all times. For all other FECCCON<1:0> bit settings, this command will execute, but will not write the ECC bits for the word and can cause DED errors if dynamic Flash ECC is enabled (FECCCON<1:0> = 01). Refer to **Section 52. "Flash Program Memory with Support for Live Update"** (DS60001193) for information regarding ECC and Flash programming.

TABLE 7-3: INTERRUPT REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0674	OFF077(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0678	OFF078(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
067C	OFF079(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0680	OFF080(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0684	OFF081(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0688	OFF082(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
068C	OFF083(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0690	OFF084(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0694	OFF085(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0698	OFF086(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
069C	OFF087(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
06A0	OFF088(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
06A4	OFF089(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
06A8	OFF090(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
06AC	OFF091(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 "CLR, SET, and INV Registers"** for more information.
2: This bit or register is not available on 64-pin devices.
3: This bit or register is not available on devices without a CAN module.
4: This bit or register is not available on 100-pin devices.
5: Bits 31 and 30 are not available on 64-pin and 100-pin devices; bits 29 through 14 are not available on 64-pin devices.
6: Bits 31, 30, 29, and bits 5 through 0 are not available on 64-pin and 100-pin devices; bit 31 is not available on 124-pin devices; bit 22 is not available on 64-pin devices.
7: This bit or register is not available on devices without a Crypto module.
8: This bit or register is not available on 124-pin devices.

TABLE 10-3: DMA CHANNEL 0 THROUGH CHANNEL 7 REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
1170	DCH1SSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSSIZ<15:0>																0000
1180	DCH1DSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDSIZ<15:0>																0000
1190	DCH1SPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSPTR<15:0>																0000
11A0	DCH1DPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDPTR<15:0>																0000
11B0	DCH1CSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCSIZ<15:0>																0000
11C0	DCH1CPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCPTR<15:0>																0000
11D0	DCH1DAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHPDAT<15:0>																0000
11E0	DCH2CON	31:16	CHPIGN<7:0>								—	—	—	—	—	—	—	—	0000
		15:0	CHBUSY	—	CHPIGNEN	—	CHPATLEN	—	—	CHCHNS	CHEN	CHAED	CHCHN	CHAEN	—	CHEDET	CHPRI<1:0>		0000
11F0	DCH2ECON	31:16	—	—	—	—	—	—	—	—	CHAIRQ<7:0>								00FF
		15:0	CHSIRQ<7:0>								CFORCE	CABORT	PATEN	SIRQEN	AIRQEN	—	—	—	FF00
1200	DCH2INT	31:16	—	—	—	—	—	—	—	—	CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE	CHERIE	0000
		15:0	—	—	—	—	—	—	—	—	CHSDIF	CHSHIF	CHDDIF	CHDHIF	CHBCIF	CHCCIF	CHTAIF	CHERIF	0000
1210	DCH2SSA	31:16	CHSSA<31:0>																0000
		15:0																	0000
1220	DCH2DSA	31:16	CHDSA<31:0>																0000
		15:0																	0000
1230	DCH2SSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSSIZ<15:0>																0000
1240	DCH2DSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDSIZ<15:0>																0000
1250	DCH2SPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSPTR<15:0>																0000
1260	DCH2DPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDPTR<15:0>																0000
1270	DCH2CSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCSIZ<15:0>																0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 "CLR, SET, and INV Registers"** for more information.

REGISTER 10-10: DCHxSSA: DMA CHANNEL x SOURCE START ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHSSA<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHSSA<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHSSA<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHSSA<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **CHSSA<31:0>** Channel Source Start Address bits
Channel source start address.
Note: This must be the physical address of the source.

REGISTER 10-11: DCHxDSA: DMA CHANNEL x DESTINATION START ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHDSA<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHDSA<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHDSA<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHDSA<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **CHDSA<31:0>:** Channel Destination Start Address bits
Channel destination start address.
Note: This must be the physical address of the destination.

REGISTER 11-9: USBIENCSR1: USB INDEXED ENDPOINT CONTROL STATUS REGISTER 1 (ENDPOINT 1-7) (CONTINUED)

bit 18 **OVERRUN:** Data Overrun Status bit (*Device mode*)

1 = An OUT packet cannot be loaded into the RX FIFO.
0 = Written by software to clear this bit

This bit is only valid when the endpoint is operating in ISO mode. In Bulk mode, it always returns zero.

ERROR: No Data Packet Received Status bit (*Host mode*)

1 = Three attempts have been made to receive a packet and no data packet has been received. An interrupt is generated.

0 = Written by the software to clear this bit.

This bit is only valid when the RX endpoint is operating in Bulk or Interrupt mode. In ISO mode, it always returns zero.

bit 17 **FIFOFULL:** FIFO Full Status bit

1 = No more packets can be loaded into the RX FIFO
0 = The RX FIFO has at least one free space

bit 16 **RXPKTRDY:** Data Packet Reception Status bit

1 = A data packet has been received. An interrupt is generated.
0 = Written by software to clear this bit when the packet has been unloaded from the RX FIFO.

bit 15-11 **MULT<4:0>:** Multiplier Control bits

For Isochronous/Interrupt endpoints or of packet splitting on Bulk endpoints, multiplies TXMAXP by MULT+1 for the payload size.

For Bulk endpoints, MULT can be up to 32 and defines the number of “USB” packets of the specified payload into which a single data packet placed in the FIFO should be split, prior to transfer. The data packet is required to be an exact multiple of the payload specified by TXMAXP.

For Isochronous/Interrupts endpoints operating in Hi-Speed mode, MULT may be either 2 or 3 and specifies the maximum number of such transactions that can take place in a single microframe.

bit 10-0 **RXMAXP<10:0>:** Maximum RX Payload Per Transaction Control bits

This field sets the maximum payload (in bytes) transmitted in a single transaction. The value is subject to the constraints placed by the USB Specification on packet sizes for Bulk, Interrupt and Isochronous transfers in Full-Speed and Hi-Speed operations.

RXMAXP must be set to an even number of bytes for proper interrupt generation in DMA Mode 1.

REGISTER 11-13: USBOTG: USB OTG CONTROL/STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	RXDPB	RXFIFOSZ<3:0>			
23:16	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	TXDPB	TXFIFOSZ<3:0>			
15:8	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
	—	—	—	—	—	—	TXEDMA	RXEDMA
7:0	R-1	R-0	R-0	R-0	R-0	R-0	R/W-0, HC	R/W-0
	BDEV	FSDEV	LSDEV	VBUS<1:0>		HOSTMODE	HOSTREQ	SESSION

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-29 **Unimplemented:** Read as '0'

bit 28 **RXDPB:** RX Endpoint Double-packet Buffering Control bit
1 = Double-packet buffer is supported. This doubles the size set in RXFIFOSZ.
0 = Double-packet buffer is not supported

bit 27-24 **RXFIFOSZ<3:0>:** RX Endpoint FIFO Packet Size bits

The maximum packet size to allowed for (before any splitting within the FIFO of Bulk/High-Bandwidth packets prior to transmission)

1111 = Reserved
•
•
•
1010 = Reserved
1001 = 4096 bytes
1000 = 2048 bytes
0111 = 1024 bytes
0110 = 512 bytes
0101 = 256 bytes
0100 = 128 bytes
0011 = 64 bytes
0010 = 32 bytes
0001 = 16 bytes
0000 = 8 bytes

bit 23-21 **Unimplemented:** Read as '0'

bit 20 **TXDPB:** TX Endpoint Double-packet Buffering Control bit
1 = Double-packet buffer is supported. This doubles the size set in TXFIFOSZ.
0 = Double-packet buffer is not supported

12.4.3 CONTROLLING PPS

PPS features are controlled through two sets of SFRs: one to map peripheral inputs, and one to map outputs. Because they are separately controlled, a particular peripheral's input and output (if the peripheral has both) can be placed on any selectable function pin without constraint.

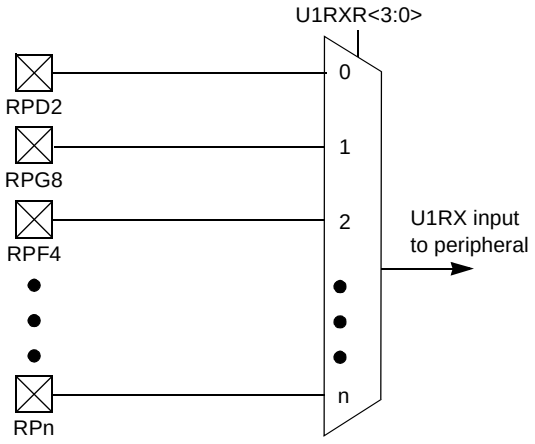
The association of a peripheral to a peripheral-selectable pin is handled in two different ways, depending on whether an input or output is being mapped.

12.4.4 INPUT MAPPING

The inputs of the PPS options are mapped on the basis of the peripheral. That is, a control register associated with a peripheral dictates the pin it will be mapped to. The [*pin name*]R registers, where [*pin name*] refers to the peripheral pins listed in Table 12-2, are used to configure peripheral input mapping (see Register 12-1). Each register contains sets of 4 bit fields. Programming these bit fields with an appropriate value maps the RPn pin with the corresponding value to that peripheral. For any given device, the valid range of values for any bit field is shown in Table 12-2.

For example, Figure 12-2 illustrates the remappable pin selection for the U1RX input.

FIGURE 12-2: REMAPPABLE INPUT EXAMPLE FOR U1RX



Note: For input only, PPS functionality does not have priority over TRISx settings. Therefore, when configuring RPn pin for input, the corresponding bit in the TRISx register must also be configured for input (set to '1').

15.1 Deadman Timer Control Registers

TABLE 15-1: DEADMAN TIMER REGISTER MAP

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0A00	DMTCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	x000
0A10	DMTPRECLR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	STEP1<7:0>								—	—	—	—	—	—	—	—	0000
0A20	DMTCLR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	STEP2<7:0>								0000
0A30	DMTSTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	BAD1	BAD2	DMTEVENT	—	—	—	—	WINOPN	0000
0A40	DMTCNT	31:16	COUNTER<31:0>																0000
		15:0																	0000
0A60	DMTPSCNT	31:16	PSCNT<31:0>																0000
		15:0																	00xx
0A70	DMTPSINTV	31:16	PSINTV<31:0>																0000
		15:0																	000x

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

REGISTER 23-1: PMCON: PARALLEL PORT CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	R/W-0, HC	U-0	U-0	U-0	U-0	U-0	R/W-0	U-0
	RDSTART	—	—	—	—	—	DUALBUF	—
15:8	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ON	—	SIDL	ADRMUX<1:0>		PMPTTL	PTWREN	PTRDEN
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
	CSF<1:0>(1)		ALP(1)	CS2P(1)	CS1P(1)	—	WRSP	RDSP

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-24 **Unimplemented:** Read as '0'

bit 23 **RDSTART:** Start Read on PMP Bus bit
This bit is cleared by hardware at the end of the read cycle.
1 = Start a read cycle on the PMP bus
0 = No effect

bit 22-18 **Unimplemented:** Read as '0'

bit 17 **DUALBUF:** Dual Read/Write Buffers enable bit
This bit is valid in Master mode only.
1 = PMP uses separate registers for reads and writes (PMRADDR, PMDATAIN, PMWADDR, PMDATAOUT)
0 = PMP uses legacy registers (PMADDR, PMDATA)

bit 16 **Unimplemented:** Read as '0'

bit 15 **ON:** Parallel Master Port Enable bit
1 = PMP is enabled
0 = PMP is disabled, no off-chip access performed

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit
1 = Discontinue module operation when device enters Idle mode
0 = Continue module operation in Idle mode

bit 12-11 **ADRMUX<1:0>:** Address/Data Multiplexing Selection bits
11 = Lower 8 bits of address are multiplexed on PMD<15:0> pins; upper 8 bits are not used
10 = All 16 bits of address are multiplexed on PMD<15:0> pins
01 = Lower 8 bits of address are multiplexed on PMD<7:0> pins, upper bits are on PMA<15:8>
00 = Address and data appear on separate pins

bit 10 **PMPTTL:** PMP Module TTL Input Buffer Select bit
1 = PMP module uses TTL input buffers
0 = PMP module uses Schmitt Trigger input buffer

bit 9 **PTWREN:** Write Enable Strobe Port Enable bit
1 = PMWR/PMENB port is enabled
0 = PMWR/PMENB port is disabled

bit 8 **PTRDEN:** Read/Write Strobe Port Enable bit
1 = PMRD/PMWR port is enabled
0 = PMRD/PMWR port is disabled

Note 1: These bits have no effect when their corresponding pins are used as address lines.

26.1 Crypto Engine Control Registers

TABLE 26-2: CRYPTO ENGINE REGISTER MAP

Virtual Address (BF8E_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
5000	CEVER	31:16	REVISION<7:0>								VERSION<7:0>								0000
		15:0	ID<15:0>																0000
5004	CECON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	SWAPOEN	SWRST	SWAPEN	—	—	BDPCHST	BDPPLEN	DMAEN	0000
5008	CEBDADDR	31:16	BDPADDR<31:0>																0000
		15:0																	0000
500C	CEBDPADDR	31:16	BASEADDR<31:0>																0000
		15:0																	0000
5010	CESTAT	31:16	ERRMODE<2:0>			ERROP<2:0>			ERRPHASE<1:0>		—	—	BDSTATE<3:0>				START	ACTIVE	0000
		15:0	BDCTRL<15:0>																0000
5014	CEINTSRC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	AREIF	PKTIF	CBDIF	PENDIF	0000
5018	CEINTEN	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	AREIE	PKTIE	CBDIE	PENDIE	0000
501C	CEPOLLCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	BDPPLCON<15:0>																0000
5020	CEHDLEN	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	HDRLEN<7:0>								0000
5024	CETRLLEN	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	TRLRLEN<7:0>								0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

REGISTER 26-3: CEBDADDR: CRYPTO ENGINE BUFFER DESCRIPTOR REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	BDPADDR<31:24>							
23:16	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	BDPADDR<23:16>							
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	BDPADDR<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	BDPADDR<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **BDPADDR<31:0>:** Current Buffer Descriptor Process Address Status bits

These bits contain the current descriptor address that is being processed by the Buffer Descriptor Processor (BDP).

REGISTER 26-4: CEBDPADDR: CRYPTO ENGINE BUFFER DESCRIPTOR PROCESSOR REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BASEADDR<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BASEADDR<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BASEADDR<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BASEADDR<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **BASEADDR<31:0>:** Buffer Descriptor Base Address bits

These bits contain the physical address of the first Buffer Descriptor in the Buffer Descriptor chain. When enabled, the Crypto DMA begins fetching Buffer Descriptors from this address.

TABLE 26-4: CRYPTO ENGINE SECURITY ASSOCIATION STRUCTURE (CONTINUED)

Name		Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
SA_ENCIV1	31:24	ENCIV<31:24>							
	23:16	ENCIV<23:16>							
	15:8	ENCIV<15:8>							
	7:0	ENCIV<7:0>							
SA_ENCIV2	31:24	ENCIV<31:24>							
	23:16	ENCIV<23:16>							
	15:8	ENCIV<15:8>							
	7:0	ENCIV<7:0>							
SA_ENCIV3	31:24	ENCIV<31:24>							
	23:16	ENCIV<23:16>							
	15:8	ENCIV<15:8>							
	7:0	ENCIV<7:0>							
SA_ENCIV4	31:24	ENCIV<31:24>							
	23:16	ENCIV<23:16>							
	15:8	ENCIV<15:8>							
	7:0	ENCIV<7:0>							

REGISTER 28-1: ADCCON1: ADC CONTROL REGISTER 1 (CONTINUED)

bit 3 **STRGLVL:** Scan Trigger High Level/Positive Edge Sensitivity bit
1 = Scan trigger is high level sensitive. Once STRIG mode is selected (TRGSRCx<4:0> in the ADCTRGx register), the scan trigger will continue for all selected analog inputs, until the STRIG option is removed.
0 = Scan trigger is positive edge sensitive. Once STRIG mode is selected (TRGSRCx<4:0> in the ADCTRGx register), only a single scan trigger will be generated, which will complete the scan of all selected analog inputs.

bit 2-0 **Unimplemented:** Read as '0'

REGISTER 29-2: CiCFG: CAN BAUD RATE CONFIGURATION REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	WAKFIL	—	—	—	SEG2PH<2:0>(1,4)		
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SEG2PHTS(1)	SAM(2)	SEG1PH<2:0>			PRSEG<2:0>		
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SJW<1:0>(3)		BRP<5:0>					

Legend:	HC = Hardware Clear	S = Settable bit	
R = Readable bit	W = Writable bit	P = Programmable bit	r = Reserved bit
U = Unimplemented bit	-n = Bit Value at POR: (‘0’, ‘1’, x = Unknown)		

bit 31-23 **Unimplemented:** Read as ‘0’

bit 22 **WAKFIL:** CAN Bus Line Filter Enable bit
1 = Use CAN bus line filter for wake-up
0 = CAN bus line filter is not used for wake-up

bit 21-19 **Unimplemented:** Read as ‘0’

bit 18-16 **SEG2PH<2:0>:** Phase Buffer Segment 2 bits(1,4)
111 = Length is 8 x TQ
•
•
•
000 = Length is 1 x TQ

bit 15 **SEG2PHTS:** Phase Segment 2 Time Select bit(1)
1 = Freely programmable
0 = Maximum of SEG1PH or Information Processing Time, whichever is greater

bit 14 **SAM:** Sample of the CAN Bus Line bit(2)
1 = Bus line is sampled three times at the sample point
0 = Bus line is sampled once at the sample point

bit 13-11 **SEG1PH<2:0>:** Phase Buffer Segment 1 bits(4)
111 = Length is 8 x TQ
•
•
•
000 = Length is 1 x TQ

Note 1: SEG2PH ≤ SEG1PH. If SEG2PHTS is clear, SEG2PH will be set automatically.
2: 3 Time bit sampling is not allowed for BRP < 2.
3: SJW ≤ SEG2PH.
4: The Time Quanta per bit must be greater than 7 (that is, TQBIT > 7).

Note: This register can only be modified when the CAN module is in Configuration mode (OPMOD<2:0> (CiCON<23:21>) = 100).

NOTES:

REGISTER 34-3: DEVCFG0/ADEVCFG0: DEVICE CONFIGURATION WORD 0

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	r-x	R/P	r-1	r-1	r-1	r-1	r-1	r-1
	—	EJTAGBEN	—	—	—	—	—	—
23:16	r-1	r-1	R/P	R/P	R/P	R/P	R/P	R/P
	—	—	POSCBOOST	POSCGAIN<1:0>		SOSCBOOST	SOSCGAIN<1:0>	
15:8	R/P	R/P	R/P	R/P	r-y	R/P	R/P	R/P
	SMCLR	DBGPER<2:0>			—	FSLEEP	FECCCON<1:0>	
7:0	r-1	R/P	R/P	R/P	R/P	R/P	R/P	R/P
	—	BOOTISA	TRCEN	ICESEL<1:0>		JTAGEN(1)	DEBUG<1:0>	

Legend:	r = Reserved bit	y = Value set from Configuration bits on POR	
R = Readable bit	P = Programmable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **Reserved:** The reset value of this bit is the same as DEVSIGN0<31>.

bit 30 **EJTAGBEN:** EJTAG Boot Enable bit
- 1 = Normal EJTAG functionality
- 0 = Reduced EJTAG functionality

bit 29-22 **Reserved:** Write as '1'

bit 21 **POSCBOOST:** Primary Oscillator Boost Kick Start Enable bit
- 1 = Boost the kick start of the oscillator
- 0 = Normal start of the oscillator

bit 20-19 **POSCGAIN<1:0>:** Primary Oscillator Gain Control bits
- 11 = Gain Level 3 (highest)
- 10 = Gain Level 2
- 01 = Gain Level 1
- 00 = Gain Level 0 (lowest)

bit 18 **SOSCBOOST:** Secondary Oscillator Boost Kick Start Enable bit
- 1 = Boost the kick start of the oscillator
- 0 = Normal start of the oscillator

bit 17-16 **SOSCGAIN<1:0>:** Secondary Oscillator Gain Control bits
- 11 = Gain Level 3 (highest)
- 10 = Gain Level 2
- 01 = Gain Level 1
- 00 = Gain Level 0 (lowest)

bit 15 **SMCLR:** Soft Master Clear Enable bit
- 1 = $\overline{\text{MCLR}}$ pin generates a normal system Reset
- 0 = $\overline{\text{MCLR}}$ pin generates a POR Reset

bit 14-12 **DBGPER<2:0>:** Debug Mode CPU Access Permission bits
- 1xx = Allow CPU access to Permission Group 2 permission regions
- x1x = Allow CPU access to Permission Group 1 permission regions
- xx1 = Allow CPU access to Permission Group 0 permission regions
- 0xx = Deny CPU access to Permission Group 2 permission regions
- x0x = Deny CPU access to Permission Group 1 permission regions
- xx0 = Deny CPU access to Permission Group 0 permission regions

When the CPU is in Debug mode and the CPU1PG<1:0> bits (CFGPG<1:0>) are set to a denied permission group as defined by DBGPER<2:0>, the transaction request is assigned Group 3 permissions.

bit 11 **Reserved:** This bit is controlled by debugger/emulator development tools and should not be modified by the user.

Note 1: This bit sets the value of the JTAGEN bit in the CFGCON register.

REGISTER 34-9: CFGEBIC: EXTERNAL BUS INTERFACE CONTROL PIN CONFIGURATION REGISTER (CONTINUED)

bit 12 **EBIOEEN:** $\overline{\text{EBIOE}}$ Pin Enable bit
1 = $\overline{\text{EBIOE}}$ pin is enabled for use by the EBI module
0 = $\overline{\text{EBIOE}}$ pin is available for general use

bit 11-10 **Unimplemented:** Read as '0'

bit 9 **EBIBSEN1:** $\overline{\text{EBIBS1}}$ Pin Enable bit
1 = $\overline{\text{EBIBS1}}$ pin is enabled for use by the EBI module
0 = $\overline{\text{EBIBS1}}$ pin is available for general use

bit 8 **EBIBSEN1:** $\overline{\text{EBIBS0}}$ Pin Enable bit
1 = $\overline{\text{EBIBS0}}$ pin is enabled for use by the EBI module
0 = $\overline{\text{EBIBS0}}$ pin is available for general use

bit 7 **EBICSEN3:** $\overline{\text{EBICS3}}$ Pin Enable bit
1 = $\overline{\text{EBICS3}}$ pin is enabled for use by the EBI module
0 = $\overline{\text{EBICS3}}$ pin is available for general use

bit 6 **EBICSEN2:** $\overline{\text{EBICS2}}$ Pin Enable bit
1 = $\overline{\text{EBICS2}}$ pin is enabled for use by the EBI module
0 = $\overline{\text{EBICS2}}$ pin is available for general use

bit 5 **EBICSEN1:** $\overline{\text{EBICS1}}$ Pin Enable bit
1 = $\overline{\text{EBICS1}}$ pin is enabled for use by the EBI module
0 = $\overline{\text{EBICS1}}$ pin is available for general use

bit 4 **EBICSEN0:** $\overline{\text{EBICS0}}$ Pin Enable bit
1 = $\overline{\text{EBICS0}}$ pin is enabled for use by the EBI module
0 = $\overline{\text{EBICS0}}$ pin is available for general use

bit 3-2 **Unimplemented:** Read as '0'

bit 1 **EBIDEN1:** EBI Data Upper Byte Pin Enable bit
1 = EBID<15:8> pins are enabled for use by the EBI module
0 = EBID<15:8> pins have reverted to general use

bit 0 **EBIDEN0:** EBI Data Lower Byte Pin Enable bit
1 = EBID<7:0> pins are enabled for use by the EBI module
0 = EBID<7:0> pins have reverted to general use

Note: When EBIMD = 1, the bits in this register are ignored and the pins are available for general use.

FIGURE 37-14: SQI SERIAL INPUT TIMING CHARACTERISTICS

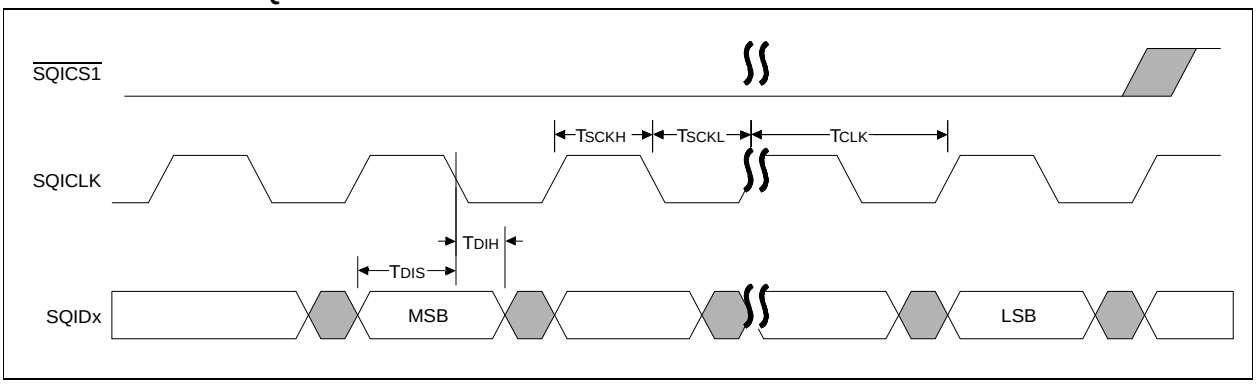
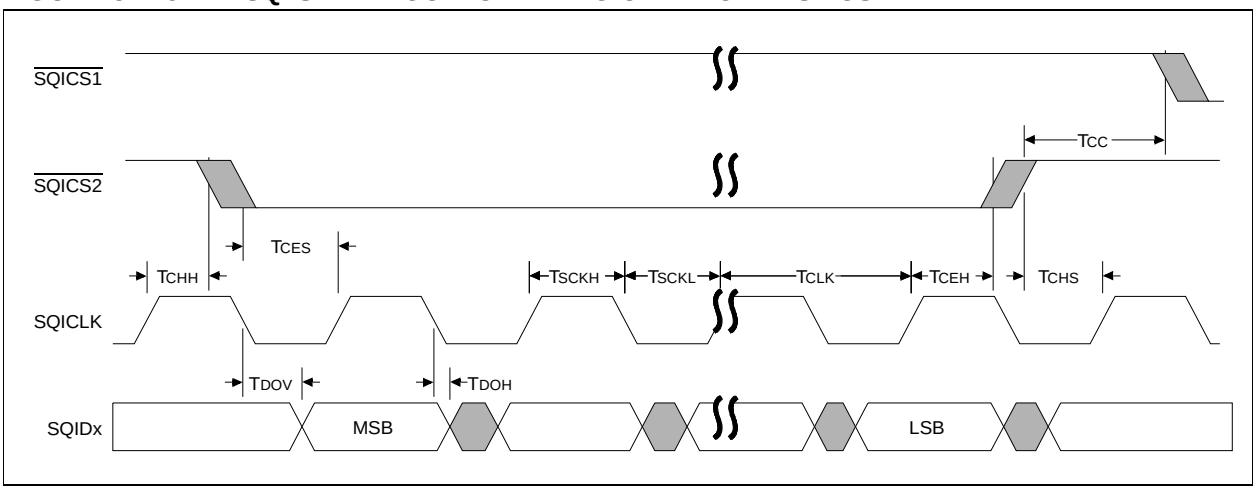


FIGURE 37-15: SQI SERIAL OUTPUT TIMING CHARACTERISTICS



Revision D (July 2016)

This revision includes the following major changes, which are referenced by their respective chapter in Table C-3.

In addition, minor updates to text and formatting were incorporated throughout the document.

TABLE C-3: MAJOR SECTION UPDATES

Section Name	Update Description
32-bit MCUs (up to 2 MB Live-Update Flash and 512 KB SRAM) with FPU, Audio and Graphics Interfaces, HS USB, Ethernet, and Advanced Analog	Updated the Operating Conditions and Core MHz values. The XFBGA package was renamed to TFBGA.
20.0 "Serial Quad Interface (SQI)"	The CLKDIV<9:0> bits in the SQI1CLKCON register were updated (see Register 20-5). The THRES<4:0> bits in the SQI1THR register were updated (see Register 20-21).
37.0 "Electrical Characteristics"	The Program Flash Memory Wait States were updated (see Table 37-13). The minimum value for System Time Requirements parameter OS51 (when the USB module is enabled) was updated (see Table 37-18).
39.0 "252 MHz Electrical Characteristics"	This chapter was added.
Appendix A: "Migrating from PIC32MX5XX/6XX/7XX to PIC32MZ EF"	The new ADC module reference was updated (see **A.2 "Analog-to-Digital Converter (ADC)"**). ADC Calibration was added to **B.2 "Analog-to-Digital Converter (ADC)"**
Appendix B: "Migrating from PIC32MZ EC to PIC32MZ EF"	The Device Configuration and Control Differences (Table B-8) were updated to include the Boot Flash Sequence. **B.10 "Serial Quad Interface (SQI)"** was updated.
Product Identification System	The Speed category was added.