Microchip Technology - PIC32MZ1024EFM144-E/PH Datasheet

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What is "Embedded - Microcontrollers"?

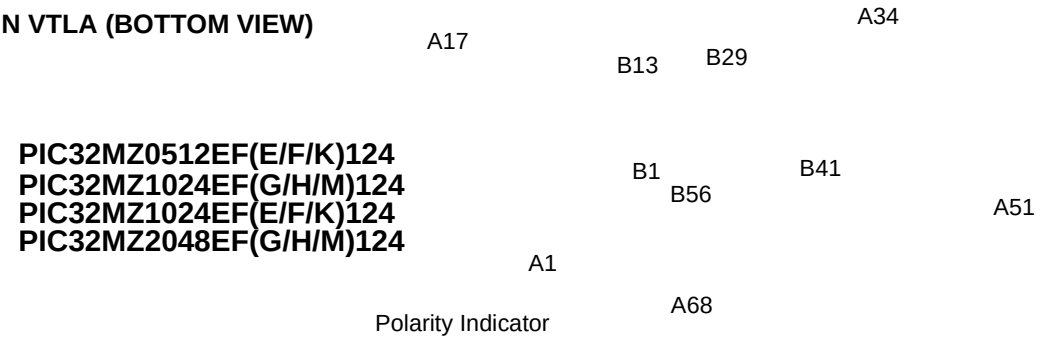
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® M-Class
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, PMP, SPI, SQI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	120
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	2.1V ~ 3.6V
Data Converters	A/D 48x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-TQFP
Supplier Device Package	144-TQFP (16x16)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mz1024efm144-e-ph

TABLE 4: PIN NAMES FOR 124-PIN DEVICES

124-PIN VTLA (BOTTOM VIEW)



Package Pin #	Full Pin Name	Package Pin #	Full Pin Name
A1	No Connect	A35	VBUS
A2	AN23/RG15	A36	VUSB3V3
A3	EBID5/AN17/RPE5/PMD5/RE5	A37	D-
A4	EBID7/AN15/PMD7/RE7	A38	RPF3/USBID/RF3
A5	AN35/ETXD0/RJ8	A39	EBIRDY2/RPF8/SCL3/RF8
A6	EBIA12/AN21/RPC2/PMA12/RC2	A40	ERXD3/RH9
A7	$\overline{\text{EBIOE}}$/AN19/RPC4/PMRD/RC4	A41	$\overline{\text{EBICS0}}$/SCL2/RA2
A8	EBIA4/AN13/C1INC/RPG7/SDA4/PMA4/RG7	A42	EBIA14/PMCS1/PMA14/RA4
A9	VSS	A43	VSS
A10	$\overline{\text{MCLR}}$	A44	EBIA8/RPF5/SCL5/PMA8/RF5
A11	TMS/EBIA16/AN24/RA0	A45	RPA15/SDA1/RA15
A12	AN26/RPE9/RE9	A46	RPD10/SCK4/RD10
A13	AN4/C1INB/RB4	A47	ECRS/RH12
A14	AN3/C2INA/RPB3/RB3	A48	RPD0/RTCC/INT0/RD0
A15	VDD	A49	SOSCO/RPC14/T1CK/RC14
A16	AN2/C2INB/RPB2/RB2	A50	VDD
A17	PGEC1/AN1/RPB1/RB1	A51	VSS
A18	PGED1/AN0/RPB0/RB0	A52	RPD1/SCK1/RD1
A19	PGED2/AN47/RPB7/RB7	A53	EBID15/RPD3/PMD15/RD3
A20	VREF+/CVREF+/AN28/RA10	A54	EBID13/PMD13/RD13
A21	AVSS	A55	EMDIO/RJ1
A22	AN39/ETXD3/RH1	A56	$\overline{\text{SQICS0}}$/RPD4/RD4
A23	EBIA7/AN49/RPB9/PMA7/RB9	A57	ETXEN/RPD6/RD6
A24	AN6/RB11	A58	VDD
A25	VDD	A59	EBID11/RPF0/PMD11/RF0
A26	TDI/EBIA18/AN30/RPF13/SCK5/RF13	A60	EBID9/RPG1/PMD9/RG1
A27	EBIA11/AN7/PMA11/RB12	A61	TRCLK/SQICLK/RA6
A28	EBIA1/AN9/RPB14/SCK3/PMA1/RB14	A62	RJ4
A29	VSS	A63	VSS
A30	AN40/ERXERR/RH4	A64	EBID1/PMD1/RE1
A31	AN42/ERXD2/RH6	A65	TRD1/SQID1/RG12
A32	AN33/RPD15/SCK6/RD15	A66	EBID2/SQID2/PMD2/RE2
A33	OSC2/CLKO/RC15	A67	EBID4/AN18/PMD4/RE4
A34	No Connect	A68	No Connect

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and **Section 12.4 "Peripheral Pin Select (PPS)"** for restrictions.

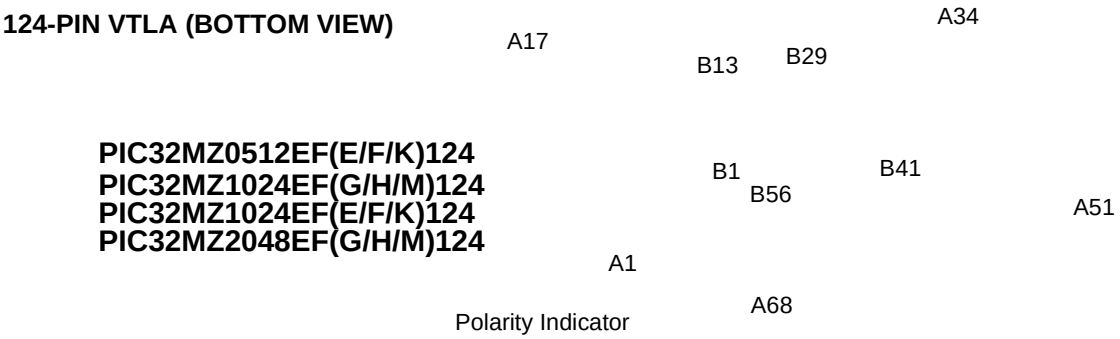
2: Every I/O port pin (RAx-RJx) can be used as a change notification pin (CNAx-CNJx). See **Section 12.0 "I/O Ports"** for more information.

3: Shaded pins are 5V tolerant.

4: The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

TABLE 4: PIN NAMES FOR 124-PIN DEVICES (CONTINUED)

124-PIN VTLA (BOTTOM VIEW)



Package Pin #	Full Pin Name	Package Pin #	Full Pin Name
B1	EBIA5/AN34/PMA5/RA5	B29	VSS
B2	EBID6/AN16/PMD6/RE6	B30	D+
B3	EBIA6/AN22/RPC1/PMA6/RC1	B31	RPF2/SDA3/RF2
B4	AN36/ETXD1/RJ9	B32	ERXD0/RH8
B5	$\overline{\text{EBIWE}}$/AN20/RPC3/PMWR/RC3	B33	ECOL/RH10
B6	AN14/C1IND/RPG6/SCK2/RG6	B34	EBIRDY1/SDA2/RA3
B7	EBIA3/AN12/C2IND/RPG8/SCL4/PMA3/RG8	B35	VDD
B8	VDD	B36	EBIA9/RPF4/SDA5/PMA9/RF4
B9	EBIA2/AN11/C2INC/RPG9/PMA2/RG9	B37	RPA14/SCL1/RA14
B10	AN25/RPE8/RE8	B38	EBIA15/RPD9/PMCS2/PMA15/RD9
B11	AN45/C1INA/RPB5/RB5	B39	EMDC/RPD11/RD11
B12	AN37/ERXCLK/EREFCLK/RJ11	B40	ERXDV/ECRSDV/RH13
B13	VSS	B41	SOSCI/RPC13/RC13
B14	PGEC2/AN46/RPB6/RB6	B42	EBID14/RPD2/PMD14/RD2
B15	VREF-/CVREF-/AN27/RA9	B43	EBID12/RPD12/PMD12/RD12
B16	AVDD	B44	ETXERR/RJ0
B17	AN38/ETXD2/RH0	B45	EBIRDY3/RJ2
B18	EBIA10/AN48/RPB8/PMA10/RB8	B46	$\overline{\text{SQICS1}}$/RPD5/RD5
B19	EBIA13/CVREFOUT/AN5/RPB10/PMA13/RB10	B47	ETXCLK/RPD7/RD7
B20	VSS	B48	VSS
B21	TCK/EBIA19/AN29/RA1	B49	EBID10/RPF1/PMD10/RF1
B22	TDO/EBIA17/AN31/RPF12/RF12	B50	EBID8/RPG0/PMD8/RG0
B23	AN8/RB13	B51	TRD3/SQID3/RA7
B24	EBIA0/AN10/RPB15/OCFB/PMA0/RB15	B52	EBID0/PMD0/RE0
B25	VDD	B53	VDD
B26	AN41/ERXD1/RH5	B54	TRD2/SQID2/RG14
B27	AN32/AETXD0/RPD14/RD14	B55	TRD0/SQID0/RG13
B28	OSC1/CLKI/RC12	B56	EBID3/RPE3/PMD3/RE3

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and **Section 12.4 "Peripheral Pin Select (PPS)"** for restrictions.

2: Every I/O port pin (RAx-RJx) can be used as a change notification pin (CNAx-CNJx). See **Section 12.0 "I/O Ports"** for more information.

3: Shaded pins are 5V tolerant.

4: The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

TABLE 1-12: PMP PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number				Pin Type	Buffer Type	Description
	64-pin QFN/ TQFP	100-pin TQFP	124-pin VTLA	144-pin TQFP/ LQFP			
PMA0	30	44	B24	30	I/O	TTL/ST	Parallel Master Port Address bit 0 Input (Buffered Slave modes) and Output (Master modes)
PMA1	29	43	A28	51	I/O	TTL/ST	Parallel Master Port Address bit 1 Input (Buffered Slave modes) and Output (Master modes)
PMA2	10	16	B9	21	O	—	Parallel Master Port Address (Demultiplexed Master modes)
PMA3	6	12	B7	52	O	—	
PMA4	5	11	A8	68	O	—	
PMA5	4	2	B1	2	O	—	
PMA6	16	6	B3	6	O	—	
PMA7	22	33	A23	48	O	—	
PMA8	42	65	A44	91	O	—	
PMA9	41	64	B36	90	O	—	
PMA10	21	32	B18	47	O	—	
PMA11	27	41	A27	29	O	—	
PMA12	24	7	A6	11	O	—	
PMA13	23	34	B19	28	O	—	
PMA14	45	61	A42	87	O	—	
PMA15	43	68	B38	97	O	—	
PMCS1	45	61	A42	87	O	—	Parallel Master Port Chip Select 1 Strobe
PMCS2	43	68	B38	97	O	—	Parallel Master Port Chip Select 2 Strobe
PMD0	58	91	B52	135	I/O	TTL/ST	Parallel Master Port Data (Demultiplexed Master mode) or Address/Data (Multiplexed Master modes)
PMD1	61	94	A64	138	I/O	TTL/ST	
PMD2	62	98	A66	142	I/O	TTL/ST	
PMD3	63	99	B56	143	I/O	TTL/ST	
PMD4	64	100	A67	144	I/O	TTL/ST	
PMD5	1	3	A3	3	I/O	TTL/ST	
PMD6	2	4	B2	4	I/O	TTL/ST	
PMD7	3	5	A4	5	I/O	TTL/ST	
PMD8	—	88	B50	128	I/O	TTL/ST	
PMD9	—	87	A60	127	I/O	TTL/ST	
PMD10	—	86	B49	125	I/O	TTL/ST	
PMD11	—	85	A59	124	I/O	TTL/ST	
PMD12	—	79	B43	112	I/O	TTL/ST	
PMD13	—	80	A54	113	I/O	TTL/ST	
PMD14	—	77	B42	110	I/O	TTL/ST	
PMD15	—	78	A53	111	I/O	TTL/ST	
PMALL	30	44	B24	30	O	—	Parallel Master Port Address Latch Enable Low Byte (Multiplexed Master modes)
PMALH	29	43	A28	51	O	—	Parallel Master Port Address Latch Enable High Byte (Multiplexed Master modes)
PMRD	53	9	A7	13	O	—	Parallel Master Port Read Strobe
PMWR	52	8	B5	12	O	—	Parallel Master Port Write Strobe

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

4.2 System Bus Arbitration

Note: The System Bus interconnect implements one or more instantiations of the SonicsSX® interconnect from Sonics, Inc. This document contains materials that are (c) 2003-2015 Sonics, Inc., and that constitute proprietary information of Sonics, Inc. SonicsSX is a registered trademark of Sonics, Inc. All such materials and trademarks are used under license from Sonics, Inc.

As shown in the PIC32MZ EF Family Block Diagram (see Figure 1-1), there are multiple initiator modules (I1 through I14) in the system that can access various target modules (T1 through T13). Table 4-4 illustrates which initiator can access which target. The System Bus supports simultaneous access to targets by initiators, so long as the initiators are accessing different targets. The System Bus will perform arbitration, if multiple initiators attempt to access the same target.

REGISTER 10-18: DCHxDAT: DMA CHANNEL x PATTERN DATA REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHPDAT<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHPDAT<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **CHPDAT<15:0>:** Channel Data Register bits

Pattern Terminate mode:
Data to be matched must be stored in this register to allow terminate on match.

All other modes:
Unused.

REGISTER 11-29: USBLPMR2: USB LINK POWER MANAGEMENT CONTROL REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	LPMFADDR<6:0>						
7:0	U-0	U-0	R-0	R-0, HS	R-0, HS	R-0, HS	R-0, HS	R-0, HS
	—	—	LPMERRIF	LPMRESIF	LPMNCIF	LPMACKIF	LPMNYIF	LPMSTIF

Legend:	HS = Hardware Set		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-15 **Unimplemented:** Read as '0'

bit 14-8 **LPMFADDR<6:0>:** LPM Payload Function Address bits
These bits contain the address of the LPM payload function.

bit 7-6 **Unimplemented:** Read as '0'

bit 5 **LPMERRIF:** LPM Error Interrupt Flag bit (*Device mode*)
1 = An LPM transaction was received that had a LINKSTATE field that is not supported. The response will be a STALL.
0 = No error condition

bit 4 **LPMRESIF:** LPM Resume Interrupt Flag bit
1 = The USB module has resumed (for any reason)
0 = No Resume condition

bit 3 **LPMNCIF:** LPM NC Interrupt Flag bit
When in *Device mode*:
1 = The USB module received a LPM transaction and responded with a NYET due to data pending in the RX FIFOs.
0 = No NC interrupt condition

When in *Host mode*:
1 = A LPM transaction is transmitted and the device responded with an ACK
0 = No NC interrupt condition

bit 2 **LPMACKIF:** LPM ACK Interrupt Flag bit
When in *Device mode*:
1 = A LPM transaction was received and the USB Module responded with an ACK
0 = No ACK interrupt condition

When in *Host mode*:
1 = The LPM transaction is transmitted and the device responds with an ACK
0 = No ACK interrupt condition

bit 1 **LPMNYIF:** LPM NYET Interrupt Flag bit
When in *Device mode*:
1 = A LPM transaction is received and the USB Module responded with a NYET
0 = No NYET interrupt flag

When in *Host mode*:
1 = A LPM transaction is transmitted and the device responded with an NYET
0 = No NYET interrupt flag

TABLE 12-2: INPUT PIN SELECTION (CONTINUED)

Peripheral Pin	[*pin name*]R SFR	[*pin name*]R bits	[*pin name*]R Value to RPn Pin Selection
INT1	INT1R	INT1R<3:0>	0000 = RPD1 0001 = RPG9 0010 = RPB14 0011 = RPD0 0100 = Reserved 0101 = RPB6 0110 = RPD5 0111 = RPB2 1000 = RPF3 1001 = RPF13(1) 1010 = No Connect 1011 = RPF2(1) 1100 = RPC2(1) 1101 = RPE8(1) 1110 = Reserved 1111 = Reserved
T4CK	T4CKR	T4CKR<3:0>	
T9CK	T9CKR	T9CKR<3:0>	
IC1	IC1R	IC1R<3:0>	
IC6	IC6R	IC6R<3:0>	
$\overline{\text{U3CTS}}$	U3CTSR	U3CTSR<3:0>	
U4RX	U4RXR	U4RXR<3:0>	
U6RX	U6RXR	U6RXR<3:0>	
$\overline{\text{SS2}}$	SS2R	SS2R<3:0>	
SDI6(1)	SDI6R(1)	SDI6R<3:0>(1)	
OCFA	OCFAR	OCFAR<3:0>	
REFCLKI3	REFCLKI3R	REFCLKI3R<3:0>	

Note 1: This selection is not available on 64-pin devices.

2: This selection is not available on 64-pin or 100-pin devices.

3: This selection is not available on devices without a CAN module.

TABLE 12-11: PORTE REGISTER MAP FOR 100-PIN, 124-PIN, AND 144-PIN DEVICES ONLY

Virtual Address (BF86_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0400	ANSELE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	ANSE9	ANSE8	ANSE7	ANSE6	ANSE5	ANSE4	—	—	—	—	03F0
0410	TRISE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	TRISE9	TRISE8	TRISE7	TRISE6	TRISE5	TRISE4	TRISE3	TRISE2	TRISE1	TRISE0	03FF
0420	PORTE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	RE9	RE8	RE7	RE6	RE5	RE4	RE3	RE2	RE1	RE0	xxxx
0430	LATE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	LATE9	LATE8	LATE7	LATE6	LATE5	LATE4	LATE3	LATE2	LATE1	LATE0	xxxx
0440	ODCE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	ODCE9	ODCE8	ODCE7	ODCE6	ODCE5	ODCE4	ODCE3	ODCE2	ODCE1	ODCE0	0000
0450	CNPUE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CNPUE9	CNPUE8	CNPUE7	CNPUE6	CNPUE5	CNPUE4	CNPUE3	CNPUE2	CNPUE1	CNPUE0	0000
0460	CNPDE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CNPDE9	CNPDE8	CNPDE7	CNPDE6	CNPDE5	CNPDE4	CNPDE3	CNPDE2	CNPDE1	CNPDE0	0000
0470	CNCONE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	EDGE DETECT	—	—	—	—	—	—	—	—	—	—	—	0000
0480	CNENE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CNENE9	CNENE8	CNENE7	CNENE6	CNENE5	CNENE4	CNENE3	CNENE2	CNENE1	CNENE0	0000
0490	CNSTATE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CN STATE9	CN STATE8	CN STATE7	CN STATE6	CN STATE5	CN STATE4	CN STATE3	CN STATE2	CN STATE1	CN STATE0	0000
04A0	CNNEE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CNNEE9	CNNEE8	CNNEE7	CNNEE6	CNNEE5	CNNEE4	CNNEE3	CNNEE2	CNNEE1	CNNEE0	0000
04B0	CNFE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CNFE9	CNFE8	CNFE7	CNFE6	CNFE5	CNFE4	CNFE3	CNFE2	CNFE1	CNFE0	0000
04C0	SRCON0E	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	SR0E3	SR0E2	SR0E1	SR0E0	0000
04D0	SRCON1E	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	SR1E3	SR1E2	SR1E1	SR1E0	0000

Legend: x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 "CLR, SET, and INV Registers"** for more information.

REGISTER 17-1: ICxCON: INPUT CAPTURE x CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0
	ON	—	SIDL	—	—	—	FEDGE	C32
7:0	R/W-0	R/W-0	R/W-0	R-0	R-0	R/W-0	R/W-0	R/W-0
	ICTMR(1)	ICI<1:0>		ICOV	ICBNE	ICM<2:0>		

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit
-n = Bit Value at POR: (‘0’, ‘1’, x = unknown)	P = Programmable bit	r = Reserved bit

bit 31-16 **Unimplemented:** Read as ‘0’

bit 15 **ON:** Input Capture Module Enable bit
- 1 = Module is enabled
- 0 = Disable and reset module, disable clocks, disable interrupt generation and allow SFR modifications

bit 14 **Unimplemented:** Read as ‘0’

bit 13 **SIDL:** Stop in Idle Control bit
- 1 = Halt in CPU Idle mode
- 0 = Continue to operate in CPU Idle mode

bit 12-10 **Unimplemented:** Read as ‘0’

bit 9 **FEDGE:** First Capture Edge Select bit (only used in mode 6, ICM<2:0> = 110)
- 1 = Capture rising edge first
- 0 = Capture falling edge first

bit 8 **C32:** 32-bit Capture Select bit
- 1 = 32-bit timer resource capture
- 0 = 16-bit timer resource capture

bit 7 **ICTMR:** Timer Select bit (Does not affect timer selection when C32 (ICxCON<8>) is ‘1’)(1)
- 0 = Timery is the counter source for capture
- 1 = Timerx is the counter source for capture

bit 6-5 **ICI<1:0>:** Interrupt Control bits
- 11 = Interrupt on every fourth capture event
- 10 = Interrupt on every third capture event
- 01 = Interrupt on every second capture event
- 00 = Interrupt on every capture event

bit 4 **ICOV:** Input Capture Overflow Status Flag bit (read-only)
- 1 = Input capture overflow is occurred
- 0 = No input capture overflow is occurred

bit 3 **ICBNE:** Input Capture Buffer Not Empty Status bit (read-only)
- 1 = Input capture buffer is not empty; at least one more capture value can be read
- 0 = Input capture buffer is empty

bit 2-0 **ICM<2:0>:** Input Capture Mode Select bits
- 111 = Interrupt-Only mode (only supported while in Sleep mode or Idle mode)
- 110 = Simple Capture Event mode – every edge, specified edge first and every edge thereafter
- 101 = Prescaled Capture Event mode – every sixteenth rising edge
- 100 = Prescaled Capture Event mode – every fourth rising edge
- 011 = Simple Capture Event mode – every rising edge
- 010 = Simple Capture Event mode – every falling edge
- 001 = Edge Detect mode – every edge (rising and falling)
- 000 = Input Capture module is disabled

Note 1: Refer to Table 17-1 for Timerx and Timery selections.

REGISTER 20-24: SQI1MEMSTAT: SQI MEMORY STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	STATPOS	STATTYPE<1:0>		STATBYTES<1:0>	
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	STATDATA<7:0>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	STATCMD<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-21 **Unimplemented:** Read as '0'

bit 20 **STATPOS:** Status Bit Position in Flash bit
Indicates the BUSY bit position in the Flash Status register. This bit is added to support all Flash types (with BUSY bit at 0 and at 7).
1 = BUSY bit position is bit 7 in status register
0 = BUSY bit position is bit 0 in status register

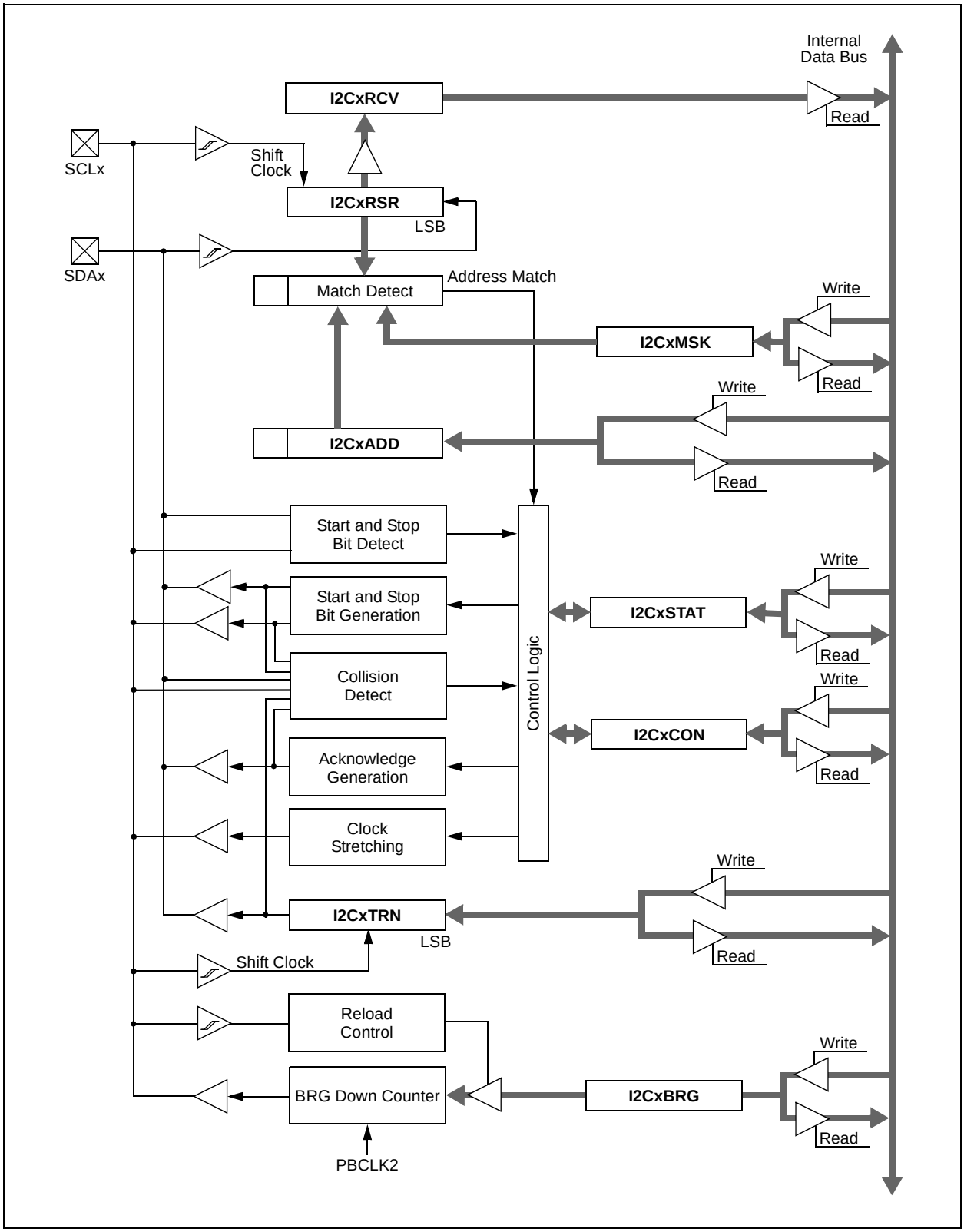
bit 19-18 **STATTYPE<1:0>:** Status Command/Read Lane Mode bits
11 = Reserved
10 = Status command and read are executed in Quad Lane mode
01 = Status command and read are executed in Dual Lane mode
00 = Status command and read are executed in Single Lane mode

bit 17-16 **STATBYTES<1:0>:** Number of Status Bytes bits
11 = Reserved
10 = Status command/read is 2 bytes long
01 = Status command/read is 1 byte long
00 = Reserved

bit 15-8 **STATDATA<7:0>:** Status Data bits
These bits contain the status value of the Flash device

bit 7-0 **STATCMD<7:0>:** Status Command bits
The status check command is written into these bits

FIGURE 21-1: I²C BLOCK DIAGRAM



REGISTER 22-2: UxSTA: UARTx STATUS AND CONTROL REGISTER (CONTINUED)

bit 7-6 **URXISEL<1:0>:** Receive Interrupt Mode Selection bit
11 = Reserved
10 = Interrupt flag bit is asserted while receive buffer is 3/4 or more full
01 = Interrupt flag bit is asserted while receive buffer is 1/2 or more full
00 = Interrupt flag bit is asserted while receive buffer is not empty (i.e., has at least 1 data character)

bit 5 **ADDEN:** Address Character Detect bit (bit 8 of received data = 1)
1 = Address Detect mode is enabled. If 9-bit mode is not selected, this control bit has no effect
0 = Address Detect mode is disabled

bit 4 **RIDLE:** Receiver Idle bit (read-only)
1 = Receiver is Idle
0 = Data is being received

bit 3 **PERR:** Parity Error Status bit (read-only)
1 = Parity error has been detected for the current character
0 = Parity error has not been detected

bit 2 **FERR:** Framing Error Status bit (read-only)
1 = Framing error has been detected for the current character
0 = Framing error has not been detected

bit 1 **OERR:** Receive Buffer Overrun Error Status bit.
This bit is set in hardware and can only be cleared (= 0) in software. Clearing a previously set OERR bit resets the receiver buffer and RSR to empty state.
1 = Receive buffer has overflowed
0 = Receive buffer has not overflowed

bit 0 **URXDA:** Receive Buffer Data Available bit (read-only)
1 = Receive buffer has data, at least one more character can be read
0 = Receive buffer is empty

REGISTER 23-4: PMDOUT: PARALLEL PORT OUTPUT DATA REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DATAOUT<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DATAOUT<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **DATAOUT<15:0>:** Port Data Output bits

This register is used for Read operations in the Enhanced Parallel Slave mode and Write operations for Dual Buffer Master mode.

In Dual Buffer Master mode, the DUALBUF bit (PMPCON<17>) = 1, a write to the MSB triggers the transaction on the PMP port. When MODE16 = 1, MSB = DATAOUT<15:8>. When MODE16 = 0, MSB = DATAOUT<7:0>.

Note: In Master mode, a read will return the last value written to the register. In Slave mode, a read will return indeterminate results.

REGISTER 23-5: PMDIN: PARALLEL PORT INPUT DATA REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DATAIN<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DATAIN<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **DATAIN<15:0>:** Port Data Input bits

This register is used for both Parallel Master Port mode and Enhanced Parallel Slave mode.

In Parallel Master mode, a write to the MSB triggers the write transaction on the PMP port. Similarly, a read to the MSB triggers the read transaction on the PMP port.

When MODE16 = 1, MSB = DATAIN<15:8>. When MODE16 = 0, MSB = DATAIN<7:0>.

Note: This register is not used in Dual Buffer Master mode (i.e., DUALBUF bit (PMPCON<17>) = 1).

REGISTER 25-2: RTCALRM: REAL-TIME CLOCK ALARM CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0
	ALRMEN(1,2)	CHIME(2)	PIV(2)	ALRMSYNC	AMASK<3:0>(2)			
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ARPT<7:0>(2)							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ALRMEN:** Alarm Enable bit(1,2)
- 1 = Alarm is enabled
- 0 = Alarm is disabled

bit 14 **CHIME:** Chime Enable bit(2)
- 1 = Chime is enabled – ARPT<7:0> is allowed to rollover from 0x00 to 0xFF
- 0 = Chime is disabled – ARPT<7:0> stops once it reaches 0x00

bit 13 **PIV:** Alarm Pulse Initial Value bit(2)

When ALRMEN = 0, PIV is writable and determines the initial value of the Alarm Pulse.
When ALRMEN = 1, PIV is read-only and returns the state of the Alarm Pulse.

bit 12 **ALRMSYNC:** Alarm Sync bit
- 1 = ARPT<7:0> and ALRMEN may change as a result of a half second rollover during a read. The ARPT must be read repeatedly until the same value is read twice. This must be done since multiple bits may be changing.
- 0 = ARPT<7:0> and ALRMEN can be read without concerns of rollover because the prescaler is more than 32 real-time clocks away from a half-second rollover

bit 11-8 **AMASK<3:0>:** Alarm Mask Configuration bits(2)
- 0000 = Every half-second
- 0001 = Every second
- 0010 = Every 10 seconds
- 0011 = Every minute
- 0100 = Every 10 minutes
- 0101 = Every hour
- 0110 = Once a day
- 0111 = Once a week
- 1000 = Once a month
- 1001 = Once a year (except when configured for February 29, once every four years)
- 1010 = Reserved
- 1011 = Reserved
- 11xx = Reserved

Note 1: Hardware clears the ALRMEN bit anytime the alarm event occurs, when ARPT<7:0> = 00 and CHIME = 0.

2: This field should not be written when the RTCC ON bit = '1' (RTCCON<15>) and ALRMSYNC = 1.

Note: This register is reset only on a Power-on Reset (POR).

REGISTER 28-27: ADCxTIME: DEDICATED ADCx TIMING REGISTER 'x' ('x' = 0 THROUGH 4)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-1
	—	—	—	ADCEIS<2:0>			SELRES<1:0>	
23:16	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	ADCDIV<6:0>						
15:8	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
	—	—	—	—	—	—	SAMC<9:8>	
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SAMC<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-29 **Unimplemented:** Read as '0'

bit 28-26 **ADCEIS<2:0>:** ADCx Early Interrupt Select bits

111 = The data ready interrupt is generated 8 ADC clocks prior to the end of conversion
110 = The data ready interrupt is generated 7 ADC clocks prior to the end of conversion
•
•
•
001 = The data ready interrupt is generated 2 ADC clocks prior to the end of conversion
000 = The data ready interrupt is generated 1 ADC clock prior to the end of conversion

Note: All options are available when the selected resolution, specified by the SELRES<1:0> bits (ADCxTIME<25:24>), is 12-bit or 10-bit. For a selected resolution of 8-bit, options from '000' to '101' are valid. For a selected resolution of 6-bit, options from '000' to '011' are valid.

bit 25-24 **SELRES<1:0>:** ADCx Resolution Select bits

11 = 12 bits
10 = 10 bits
01 = 8 bits
00 = 6 bits

Note: Changing the resolution of the ADC does not shift the result in the corresponding ADCDATAx register. The result will still occupy 12 bits, with the corresponding lower unused bits set to '0'. For example, a resolution of 6 bits will result in ADCDATAx<5:0> being set to '0', and ADCDATAx<11:6> holding the result.

bit 23 **Unimplemented:** Read as '0'

bit 22-16 **ADCDIV<6:0>:** ADCx Clock Divisor bits

These bits divide the ADC control clock with period TQ to generate the clock for ADCx (TADx).

1111111 = 254 * TQ = TADx
•
•
•
0000011 = 6 * TQ = TADx
0000010 = 4 * TQ = TADx
0000001 = 2 * TQ = TADx
0000000 = Reserved

bit 15-10 **Unimplemented:** Read as '0'

bit 9-0 **SAMC<9:0>:** ADCx Sample Time bits

Where TADx = period of the ADC conversion clock for the dedicated ADC controlled by the ADCDIV<6:0> bits.

1111111111 = 1025 TADx
•
•
•
0000000001 = 3 TADx
0000000000 = 2 TADx

TABLE 29-2: CAN2 REGISTER SUMMARY FOR PIC32MZXXXXECF AND PIC32MZXXXXECH DEVICES (CONTINUED)

Virtual Address (BF88_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
1100	C2FLTCON4	31:16	FLTEN19	MSEL19<1:0>		FSEL19<4:0>					FLTEN18	MSEL18<1:0>		FSEL18<4:0>					0000
		15:0	FLTEN17	MSEL17<1:0>		FSEL17<4:0>					FLTEN16	MSEL16<1:0>		FSEL16<4:0:					0000
1110	C2FLTCON5	31:16	FLTEN23	MSEL23<1:0>		FSEL23<4:0>					FLTEN22	MSEL22<1:0>		FSEL22<4:0>					0000
		15:0	FLTEN21	MSEL21<1:0>		FSEL21<4:0>					FLTEN20	MSEL20<1:0>		FSEL20<4:0>					0000
1120	C2FLTCON6	31:16	FLTEN27	MSEL27<1:0>		FSEL27<4:0>					FLTEN26	MSEL26<1:0>		FSEL26<4:0>					0000
		15:0	FLTEN25	MSEL25<1:0>		FSEL25<4:0>					FLTEN24	MSEL24<1:0>		FSEL24<4:0>					0000
1130	C2FLTCON7	31:16	FLTEN31	MSEL31<1:0>		FSEL31<4:0>					FLTEN30	MSEL30<1:0>		FSEL30<4:0>					0000
		15:0	FLTEN29	MSEL29<1:0>		FSEL29<4:0>					FLTEN28	MSEL28<1:0>		FSEL28<4:0>					0000
1140-1330	C2RXFn (n = 0-31)	31:16	SID<10:0>											-—	EXID	—	EID<17:16>		xxxx
		15:0	EID<15:0>																xxxx
1340	C2FIFOBA	31:16	C2FIFOBA<31:0>																0000
		15:0																	0000
1350	C2FIFOCONn (n = 0)	31:16	—	—	—	—	—	—	—	—	—	—	—	FSIZE<4:0>					0000
		15:0	—	FRESET	UINC	DONLY	—	—	—	—	TXEN	TXABAT	TXLARB	TXERR	TXREQ	RTREN	TXPRI<1:0>		0000
1360	C2FIFOINTn (n = 0)	31:16	—	—	—	—	—	TXNFULLIE	TXHALFIE	TXEMPTYIE	—	—	—	—	RXOVFLIE	RXFULLIE	RXHALFIE	RXN EMPTYIE	0000
		15:0	—	—	—	—	—	TXNFULLIF	TXHALFIF	TXEMPTYIF	—	—	—	—	RXOVFLIF	RXFULLIF	RXHALFIF	RXN EMPTYIF	0000
1370	C2FIFOUAn (n = 0)	31:16	C2FIFOUA<31:0>																0000
		15:0																	0000
1380	C2FIFOCIn (n = 0)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	C2FIFOCI<4:0>					0000
1390-1B40	C2FIFOCONn C2FIFOINTn C2FIFOUAn C2FIFOCIn (n = 1-31)	31:16	—	—	—	—	—	—	—	—	—	—	—	FSIZE<4:0>					0000
		15:0	—	FRESET	UINC	DONLY	—	—	—	—	TXEN	TXABAT	TXLARB	TXERR	TXREQ	RTREN	TXPRI<1:0>		0000
		31:16	—	—	—	—	—	TXNFULLIE	TXHALFIE	TXEMPTYIE	—	—	—	—	RXOVFLIE	RXFULLIE	RXHALFIE	RXN EMPTYIE	0000
		15:0	—	—	—	—	—	TXNFULLIF	TXHALFIF	TXEMPTYIF	—	—	—	—	RXOVFLIF	RXFULLIF	RXHALFIF	RXN EMPTYIF	0000
		31:16	C2FIFOUA<31:0>																0000
		15:0																	0000
		31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	C2FIFOCI<4:0>					0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 "CLR, SET, and INV Registers"** for more information.

NOTES:

TABLE 37-10: DC CHARACTERISTICS: I/O PIN INPUT INJECTION CURRENT SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Symbol**	**Characteristics**	**Min.**	**Typical(1)**	**Max.**	**Units**	**Conditions**
DI60a	IICL	**Input Low Injection Current**	0	—	-5(2,5)	mA	This parameter applies to all pins, with the exception of RB10. Maximum IICH current for this exception is 0 mA.
DI60b	IICH	**Input High Injection Current**	0	—	+5(3,4,5)	mA	This parameter applies to all pins, with the exception of all 5V tolerant pins, OSCI, OSCO, SOSCI, SOSCO, D+, D- and RB10. Maximum IICH current for these exceptions is 0 mA.
DI60c	∑IICT	**Total Input Injection Current (sum of all I/O and control pins)**	-20(6)	—	+20(6)	mA	Absolute instantaneous sum of all ± input injection currents from all I/O pins (| IICL + | IICH |) ≤ ∑IICT

Note 1: Data in “Typical” column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: VIL source < (VSS - 0.3). Characterized but not tested.

3: VIH source > (VDD + 0.3) for non-5V tolerant pins only.

4: Digital 5V tolerant pins do not have an internal high side diode to VDD, and therefore, cannot tolerate any “positive” input injection current.

5: Injection currents > | 0 | can affect the ADC results by approximately 4 to 6 counts (i.e., VIH Source > (VDD + 0.3) or VIL source < (VSS - 0.3)).

6: Any number and/or combination of I/O pins not excluded under IICL or IICH conditions are permitted provided the “absolute instantaneous” sum of the input injection currents from all pins do not exceed the specified limit. If **Note 2**, IICL = (((Vss - 0.3) - VIL source) / Rs). If **Note 3**, IICH = ((IICH source - (VDD + 0.3)) / RS). RS = Resistance between input source voltage and device pin. If (VSS - 0.3) ≤ VSOURCE ≤ (VDD + 0.3), injection current = 0.

TABLE 37-23: I/O TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Symbol**	**Characteristics(2)**	**Min.**	**Typ.(1)**	**Max.**	**Units**	**Conditions**
DO31	TIOR	**Port Output Rise Time** I/O Pins: 4x Source Driver Pins - RA3, RA9, RA10, RA14, RA15 RB0-RB2, RB4, RB6-RB7, RB11, RB13 RC12-RC15 RD0, RD6-RD7, RD11, RD14 RE8, RE9 RF2, RF3, RF8 RG15 RH0, RH1, RH4-RH6, RH8-RH13 RJ0-RJ2, RJ8, RJ9, RJ11	—	—	9.5	ns	CLOAD = 50 pF
			—	—	6	ns	CLOAD = 20 pF
		Port Output Rise Time I/O Pins: 8x Source Driver Pins - RA0-RA2, RA4, RA5 RB3, RB5, RB8-RB10, RB12, RB14, RB15 RC1-RC4 RD1-RD5, RD9, RD10, RD12, RD13, RD15 RE4-RE7 RF0, RF4, RF5, RF12, RF13 RG0, RG1, RG6-RG9 RH2, RH3, RH7, RH14, RH15 RJ3-RJ7, RJ10, RJ12-RJ15 RK0-RK7	—	—	8	ns	CLOAD = 50 pF
			—	—	6	ns	CLOAD = 20 pF
		Port Output Rise Time I/O Pins: 12x Source Driver Pins - RA6, RA7 RE0-RE3 RF1 RG12-RG14	—	—	3.5	ns	CLOAD = 50 pF
			—	—	2	ns	CLOAD = 20 pF

Note 1: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

2: This parameter is characterized, but not tested in manufacturing.

TABLE A-9: FLASH PROGRAMMING DIFFERENCES (CONTINUED)

PIC32MX5XX/6XX/7XX Feature	PIC32MZ EF Feature
Flash Programming	
	The op codes for programming the Flash memory have been changed to accommodate the new quad-word programming and dual-panel features. The row size has changed to 2 KB (512 IW) from 128 IW. The page size has changed to 16 KB (4K IW) from 4 KB (1K IW). Note that the NVMOP register is now protected, and requires the WREN bit be set to enable modification.
NVMOP<3:0> (NVMCON<3:0>) 1111 = Reserved • • • **0111 = Reserved** **0110 = No operation** **0101 = Program Flash (PFM) erase operation** 0100 = Page erase operation 0011 = Row program operation **0010 = No operation** 0001 = Word program operation 0000 = No operation	NVMOP<3:0> (NVMCON<3:0>) 1111 = Reserved • • • 1000 = Reserved **0111 = Program erase operation** **0110 = Upper program Flash memory erase operation** **0101 = Lower program Flash memory erase operation** 0100 = Page erase operation 0011 = Row program operation **0010 = Quad Word (128-bit) program operation** 0001 = Word program operation 0000 = No operation
PIC32MX devices feature a single NVMDATA register for word programming. NVMDATA	On PIC32MZ EF devices, to support quad word programming, the NVMDATA register has been expanded to four words. NVMDATA**x**, where 'x' = 0 through 3
Flash Endurance and Retention	
PIC32MX devices support Flash endurance and retention of up to 20K E/W cycles and 20 years.	On PIC32MZ EF devices, ECC must be enabled to support the same endurance and retention as PIC32MX devices.
Configuration Words	
On PIC32MX devices, Configuration Words can be programmed with **Word or Row program** operation.	On PIC32MZ EF devices, all Configuration Words must be programmed with **Quad Word or Row Program** operations.
Configuration Words Reserved Bit	
On PIC32MX devices, the **DEVCFG0<15>** bit is Reserved and must be programmed to '0'.	On PIC32MZ EF devices, this bit is **DEVSIGN0<31>**.