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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	MIPS32® M-Class
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, PMP, SPI, SQI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	120
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	2.1V ~ 3.6V
Data Converters	A/D 48x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mz1024efm144-i-pl

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

TABLE 1-6: PORTA THROUGH PORTK PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number				Pin Type	Buffer Type	Description
	64-pin QFN/ TQFP	100-pin TQFP	124-pin VTLA	144-pin TQFP/ LQFP			
PORTG							
RG0	—	88	B50	128	I/O	ST	PORTG is a bidirectional I/O port
RG1	—	87	A60	127	I/O	ST	
RG6	4	10	B6	14	I/O	ST	
RG7	5	11	A8	15	I/O	ST	
RG8	6	12	B7	16	I/O	ST	
RG9	10	16	B9	21	I/O	ST	
RG12	—	96	A65	140	I/O	ST	
RG13	—	97	B55	141	I/O	ST	
RG14	—	95	B54	139	I/O	ST	
RG15	—	1	A2	1	I/O	ST	
PORTH							
RH0	—	—	B17	43	I/O	ST	PORTH is a bidirectional I/O port
RH1	—	—	A22	44	I/O	ST	
RH2	—	—	—	45	I/O	ST	
RH3	—	—	—	46	I/O	ST	
RH4	—	—	A30	65	I/O	ST	
RH5	—	—	B26	66	I/O	ST	
RH6	—	—	A31	67	I/O	ST	
RH7	—	—	—	68	I/O	ST	
RH8	—	—	B32	81	I/O	ST	
RH9	—	—	A40	82	I/O	ST	
RH10	—	—	B33	83	I/O	ST	
RH11	—	—	—	84	I/O	ST	
RH12	—	—	A47	100	I/O	ST	
RH13	—	—	B40	101	I/O	ST	
RH14	—	—	—	102	I/O	ST	
RH15	—	—	—	103	I/O	ST	
PORTJ							
RJ0	—	—	B44	114	I/O	ST	PORTJ is a bidirectional I/O port
RJ1	—	—	A55	115	I/O	ST	
RJ2	—	—	B45	116	I/O	ST	
RJ3	—	—	—	117	I/O	ST	
RJ4	—	—	A62	131	I/O	ST	
RJ5	—	—	—	132	I/O	ST	
RJ6	—	—	—	133	I/O	ST	
RJ7	—	—	—	134	I/O	ST	
RJ8	—	—	A5	7	I/O	ST	
RJ9	—	—	B4	8	I/O	ST	
RJ10	—	—	—	10	I/O	ST	
RJ11	—	—	B12	27	I/O	ST	
RJ12	—	—	—	9	I/O	ST	
RJ13	—	—	—	28	I/O	ST	
RJ14	—	—	—	29	I/O	ST	
RJ15	—	—	—	30	I/O	ST	

Legend: CMOS = CMOS-compatible input or output
ST = Schmitt Trigger input with CMOS levels
TTL = Transistor-transistor Logic input buffer

Analog = Analog input
O = Output
PPS = Peripheral Pin Select

P = Power
I = Input

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

REGISTER 3-10: FCSR: FLOATING POINT CONTROL AND STATUS REGISTER; CP1 REGISTER 31

bit 16	V: Invalid Operation bit
bit 15	Z: Divide-by-Zero bit
bit 14	O: Overflow bit
bit 13	U: Underflow bit
bit 12	I: Inexact bit
bit 11-7	ENABLES<4:0>: FPU Exception Enable bits These bits control whether or not a trap is taken when an IEEE exception condition occurs for any of the five conditions. The trap occurs when both an enable bit and its corresponding cause bit are set either during an FPU arithmetic operation or by moving a value to the FCSR or one of its alternative representations.
bit 11	V: Invalid Operation bit
bit 10	Z: Divide-by-Zero bit
bit 9	O: Overflow bit
bit 8	U: Underflow bit
bit 7	I: Inexact bit
bit 6-2	FLAGS<4:0>: FPU Flags bits These bits show any exception conditions that have occurred for completed instructions since the flag was last reset by software.
bit 6	V: Invalid Operation bit
bit 5	Z: Divide-by-Zero bit
bit 4	O: Overflow bit
bit 3	U: Underflow bit
bit 2	I: Inexact bit
bit 1-0	RM<1:0>: Rounding Mode control bits 11 = Round towards Minus Infinity ($-\infty$) 10 = Round towards Plus Infinity ($+\infty$) 01 = Round toward Zero (0) 00 = Round to Nearest

TABLE 4-12: SYSTEM BUS TARGET 4 REGISTER MAP

Virtual Address (BF8F_#)	Register Name	Bit Range	Bits															All Resets	
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1		16/0
9020	SBT4ELOG1	31:16	MULTI	—	—	—	CODE<3:0>				—	—	—	—	—	—	—	—	0000
		15:0	INITID<7:0>							REGION<3:0>				—	CMD<2:0>				0000
9024	SBT4ELOG2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	GROUP<1:0>			0000
9028	SBT4ECON	31:16	—	—	—	—	—	—	—	ERRP	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
9030	SBT4ECLRS	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
9038	SBT4ECLRM	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
9040	SBT4REG0	31:16	BASE<21:6>															xxxx	
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
9050	SBT4RD0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
9058	SBT4WR0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
9080	SBT4REG2	31:16	BASE<21:6>															xxxx	
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
9090	SBT4RD2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
9098	SBT4WR2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note: For reset values listed as 'xxxx', please refer to Table 4-6 for the actual reset values.

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

REGISTER 5-8: NVMBWP: FLASH BOOT (PAGE) WRITE-PROTECT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-1	U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
	LBWPULOCK	—	—	LBWP4 ⁽¹⁾	LBWP3 ⁽¹⁾	LBWP2 ⁽¹⁾	LBWP1 ⁽¹⁾	LBWP0 ⁽¹⁾
7:0	R/W-1	r-1	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
	UBWPULOCK	—	—	UBWP4 ⁽¹⁾	UBWP3 ⁽¹⁾	UBWP2 ⁽¹⁾	UBWP1 ⁽¹⁾	UBWP0 ⁽¹⁾

Legend:

R = Readable bit

W = Writable bit

r = Reserved

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **LBWPULOCK:** Lower Boot Alias Write-protect Unlock bit

1 = LBWPx bits are not locked and can be modified

0 = LBWPx bits are locked and cannot be modified

This bit is only clearable and cannot be set except by any reset.

bit 14-13 **Unimplemented:** Read as '0'

bit 12 **LBWP4:** Lower Boot Alias Page 4 Write-protect bit⁽¹⁾

1 = Write protection for physical address 0x01FC10000 through 0x1FC13FFF enabled

0 = Write protection for physical address 0x01FC10000 through 0x1FC13FFF disabled

bit 11 **LBWP3:** Lower Boot Alias Page 3 Write-protect bit⁽¹⁾

1 = Write protection for physical address 0x01FC0C000 through 0x1FC0FFFF enabled

0 = Write protection for physical address 0x01FC0C000 through 0x1FC0FFFF disabled

bit 10 **LBWP2:** Lower Boot Alias Page 2 Write-protect bit⁽¹⁾

1 = Write protection for physical address 0x01FC08000 through 0x1FC0BFFF enabled

0 = Write protection for physical address 0x01FC08000 through 0x1FC0BFFF disabled

bit 9 **LBWP1:** Lower Boot Alias Page 1 Write-protect bit⁽¹⁾

1 = Write protection for physical address 0x01FC04000 through 0x1FC07FFF enabled

0 = Write protection for physical address 0x01FC04000 through 0x1FC07FFF disabled

bit 8 **LBWP0:** Lower Boot Alias Page 0 Write-protect bit⁽¹⁾

1 = Write protection for physical address 0x01FC00000 through 0x1FC03FFF enabled

0 = Write protection for physical address 0x01FC00000 through 0x1FC03FFF disabled

bit 7 **UBWPULOCK:** Upper Boot Alias Write-protect Unlock bit

1 = UBWPx bits are not locked and can be modified

0 = UBWPx bits are locked and cannot be modified

This bit is only user-clearable and cannot be set except by any reset.

bit 6 **Reserved:** This bit is reserved for use by development tools

bit 5 **Unimplemented:** Read as '0'

Note 1: These bits are only available when the NVMKEY unlock sequence is performed and the associated Lock bit (LBWPULOCK or UBWPULOCK) is set.

Note: The bits in this register are only writable when the NVMKEY unlock sequence is followed.

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

REGISTER 10-9: DCHxINT: DMA CHANNEL x INTERRUPT CONTROL REGISTER (CONTINUED)

- bit 5 **CHDDIF:** Channel Destination Done Interrupt Flag bit
1 = Channel Destination Pointer has reached end of destination (CHDPTR = CHDSIZ)
0 = No interrupt is pending
- bit 4 **CHDHIF:** Channel Destination Half Full Interrupt Flag bit
1 = Channel Destination Pointer has reached midpoint of destination (CHDPTR = CHDSIZ/2)
0 = No interrupt is pending
- bit 3 **CHBCIF:** Channel Block Transfer Complete Interrupt Flag bit
1 = A block transfer has been completed (the larger of CHSSIZ/CHDSIZ bytes has been transferred), or a pattern match event occurs
0 = No interrupt is pending
- bit 2 **CHCCIF:** Channel Cell Transfer Complete Interrupt Flag bit
1 = A cell transfer has been completed (CHCSIZ bytes have been transferred)
0 = No interrupt is pending
- bit 1 **CHTAIF:** Channel Transfer Abort Interrupt Flag bit
1 = An interrupt matching CHAIRQ has been detected and the DMA transfer has been aborted
0 = No interrupt is pending
- bit 0 **CHERIF:** Channel Address Error Interrupt Flag bit
1 = A channel address error has been detected
 Either the source or the destination address is invalid.
0 = No interrupt is pending

TABLE 11-1: USB REGISTER MAP 1 (CONTINUED)

Virtual Address (BF8E #)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
3028	USB FIFO2	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
302C	USB FIFO3	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
3030	USB FIFO4	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
3034	USB FIFO5	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
3038	USB FIFO6	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
303C	USB FIFO7	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
3060	USBOTG	31:16	—	—	—	RXDPB	RXFIFOSZ<3:0>			—	—	—	TXDPB	TXFIFOSZ<3:0>				0000	
		15:0	—	—	—	—	—	—	TXEDMA	RXEDMA	BDEV	FSDEV	LSDEV	VBUS<1:0>		HOSTMODE	HOSTREQ	SESSION	0080
3064	USB FIFOA	31:16	—	—	—	RXFIFOAD<12:0>												0000	
		15:0	—	—	—	TXFIFOAD<12:0>												0000	
306C	USB HWVER	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	RC	VERMAJOR<4:0>					VERMINOR<9:0>									0800	
3078	USB INFO	31:16	VPLEN<7:0>								WTCON<3:0>				WTID<3:0>				3C5C
		15:0	DMACHANS<3:0>				RAMBITS<3:0>				RXENDPTS<3:0>				TXENDPTS<3:0>				8C77
307C	USB EOFRST	31:16	—	—	—	—	—	—	NRSTX	NRST	LSEOF<7:0>							0072	
		15:0	FSEOF<7:0>								HSEOF<7:0>							7780	
3080	USB E0TXA	31:16	—	TXHUBPRT<6:0>							MULTTRAN	TXHUBADD<6:0>						0000	
		15:0	—	—	—	—	—	—	—	—	—	TXFADDR<6:0>						0000	
3084	USB E0RXA	31:16	—	RXHUBPRT<6:0>							MULTTRAN	RXHUBADD<6:0>						0000	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
3088	USB E1TXA	31:16	—	TXHUBPRT<6:0>							MULTTRAN	TXHUBADD<6:0>						0000	
		15:0	—	—	—	—	—	—	—	—	—	TXFADDR<6:0>						0000	
308C	USB E1RXA	31:16	—	RXHUBPRT<6:0>							MULTTRAN	RXHUBADD<6:0>						0000	
		15:0	—	—	—	—	—	—	—	—	—	RXFADDR<6:0>						0000	
3090	USB E2TXA	31:16	—	TXHUBPRT<6:0>							MULTTRAN	TXHUBADD<6:0>						0000	
		15:0	—	—	—	—	—	—	—	—	—	TXFADDR<6:0>						0000	
3094	USB E2RXA	31:16	—	RXHUBPRT<6:0>							MULTTRAN	RXHUBADD<6:0>						0000	
		15:0	—	—	—	—	—	—	—	—	—	RXFADDR<6:0>						0000	
3098	USB E3TXA	31:16	—	TXHUBPRT<6:0>							MULTTRAN	TXHUBADD<6:0>						0000	
		15:0	—	—	—	—	—	—	—	—	—	TXFADDR<6:0>						0000	

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

- Note
- 1: Device mode.
 - 2: Host mode.
 - 3: Definition for Endpoint 0 (ENDPOINT<3:0> (USBCSR<19:16>) = 0).
 - 4: Definition for Endpoints 1-7 (ENDPOINT<3:0> (USBCSR<19:16>) = 1 through 7).

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

REGISTER 11-12: USBFIFOx: USB FIFO DATA REGISTER 'x' ('x' = 0-7)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DATA<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DATA<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DATA<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DATA<7:0>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-0 **DATA<31:0>**: USB Transmit/Receive FIFO Data bits

Writes to this register loads data into the TxFIFO for the corresponding endpoint. Reading from this register unloads data from the RxFIFO for the corresponding endpoint.

Transfers may be 8-bit, 16-bit or 32-bit as required, and any combination of access is allowed provided the data accessed is contiguous. However, all transfers associated with one packet must be of the same width so that data is consistently byte-, word- or double-word aligned. The last transfer may contain fewer bytes than the previous transfers in order to complete an odd-byte or odd-word transfer.

TABLE 12-9: PORTD REGISTER MAP FOR 100-PIN DEVICES ONLY

Virtual Address (BF86_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0300	ANSELD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ANS15	ANS14	—	—	—	—	—	—	—	—	—	—	—	—	—	—	C000
0310	TRISD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRISD15	TRISD14	TRISD13	TRISD12	TRISD11	TRISD10	TRISD9	—	—	—	TRISD5	TRISD4	TRISD3	TRISD2	TRISD1	TRISD0	FE3F
0320	PORTD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RD15	RD14	RD13	RD12	RD11	RD10	RD9	—	—	—	RD5	RD4	RD3	RD2	RD1	RD0	xxxx
0330	LATD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	LATD15	LATD14	LATD13	LATD12	LATD11	LATD10	LATD9	—	—	—	LATD5	LATD4	LATD3	LATD2	LATD1	LATD0	xxxx
0340	ODCD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ODCD15	ODCD14	ODCD13	ODCD12	ODCD11	ODCD10	ODCD9	—	—	—	ODCD5	ODCD4	ODCD3	ODCD2	ODCD1	ODCD0	0000
0350	CNPUD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPUD15	CNPUD14	CNPUD13	CNPUD12	CNPUD11	CNPUD10	CNPUD9	—	—	—	CNPUD5	CNPUD4	CNPUD3	CNPUD2	CNPUD1	CNPUD0	0000
0360	CNPDD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPDD15	CNPDD14	CNPDD13	CNPDD12	CNPDD11	CNPDD10	CNPDD9	—	—	—	CNPDD5	CNPDD4	CNPDD3	CNPDD2	CNPDD1	CNPDD0	0000
0370	CNCOND	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	EDGE DETECT	—	—	—	—	—	—	—	—	—	—	—	0000
0380	CNEND	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNEND15	CNEND14	CNEND13	CNEND12	CNEND11	CNEND10	CNEND9	—	—	—	CNEND5	CNEND4	CNEND3	CNEND2	CNEND1	CNEND0	0000
0390	CNSTATD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CN STATD15	CN STATD14	CN STATD13	CN STATD12	CN STATD11	CN STATD10	CN STATD9	—	—	—	CN STATD5	CN STATD4	CN STATD3	CN STATD2	CN STATD1	CN STATD0	0000
03A0	CNNED	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNNED15	CNNED14	CNNED13	CNNED12	CNNED11	CNNED10	CNNED9	—	—	—	CNNED5	CNNED4	CNNED3	CNNED2	CNNED1	CNNED0	0000
03B0	CNFD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNFD15	CNFD14	CNFD13	CNFD12	CNFD11	CNFD10	CNFD9	—	—	—	CNFD5	CNFD4	CNFD3	CNFD2	CNFD1	CNFD0	0000

Legend: x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 “CLR, SET, and INV Registers”** for more information.

REGISTER 14-1: TxCON: TYPE B TIMER CONTROL REGISTER ('x' = 2-9) (CONTINUED)

- bit 2 **Unimplemented:** Read as '0'
- bit 1 **TCS:** Timer Clock Source Select bit⁽¹⁾
 1 = External clock from TxCK pin
 0 = Internal peripheral clock
- bit 0 **Unimplemented:** Read as '0'

- Note 1:** While operating in 32-bit mode, this bit has no effect for odd numbered timers (Timer1, Timer3, Timer5, Timer7, and Timer9). All timer functions are set through the even numbered timers.
- 2:** While operating in 32-bit mode, this bit must be cleared on odd numbered timers to enable the 32-bit timer in Idle mode.
- 3:** This bit is available only on even numbered timers (Timer2, Timer4, Timer6, and Timer8).

REGISTER 19-1: SPIxCON: SPI CONTROL REGISTER (CONTINUED)

- bit 17 **SPIFE**: Frame Sync Pulse Edge Select bit (Framed SPI mode only)
 1 = Frame synchronization pulse coincides with the first bit clock
 0 = Frame synchronization pulse precedes the first bit clock
- bit 16 **ENHBUF**: Enhanced Buffer Enable bit⁽¹⁾
 1 = Enhanced Buffer mode is enabled
 0 = Enhanced Buffer mode is disabled
- bit 15 **ON**: SPI/I²S Module On bit
 1 = SPI/I²S module is enabled
 0 = SPI/I²S module is disabled
- bit 14 **Unimplemented**: Read as '0'
- bit 13 **SIDL**: Stop in Idle Mode bit
 1 = Discontinue operation when CPU enters in Idle mode
 0 = Continue operation in Idle mode
- bit 12 **DISSDO**: Disable SDOx pin bit⁽⁴⁾
 1 = SDOx pin is not used by the module. Pin is controlled by associated PORT register
 0 = SDOx pin is controlled by the module
- bit 11-10 **MODE<32,16>**: 32/16-Bit Communication Select bits
 When AUDEN = 1:
- | MODE32 | MODE16 | Communication |
|--------|--------|---|
| 1 | 1 | 24-bit Data, 32-bit FIFO, 32-bit Channel/64-bit Frame |
| 1 | 0 | 32-bit Data, 32-bit FIFO, 32-bit Channel/64-bit Frame |
| 0 | 1 | 16-bit Data, 16-bit FIFO, 32-bit Channel/64-bit Frame |
| 0 | 0 | 16-bit Data, 16-bit FIFO, 16-bit Channel/32-bit Frame |
- When AUDEN = 0:
- | MODE32 | MODE16 | Communication |
|--------|--------|---------------|
| 1 | x | 32-bit |
| 0 | 1 | 16-bit |
| 0 | 0 | 8-bit |
- bit 9 **SMP**: SPI Data Input Sample Phase bit
 Master mode (MSTEN = 1):
 1 = Input data sampled at end of data output time
 0 = Input data sampled at middle of data output time
 Slave mode (MSTEN = 0):
 SMP value is ignored when SPI is used in Slave mode. The module always uses SMP = 0.
- bit 8 **CKE**: SPI Clock Edge Select bit⁽²⁾
 1 = Serial output data changes on transition from active clock state to Idle clock state (see CKP bit)
 0 = Serial output data changes on transition from Idle clock state to active clock state (see CKP bit)
- bit 7 **SSEN**: Slave Select Enable (Slave mode) bit
 1 = \overline{SSx} pin is used for Slave mode
 0 = \overline{SSx} pin is not used for Slave mode, pin is controlled by the port function.
- bit 6 **CKP**: Clock Polarity Select bit⁽³⁾
 1 = Idle state for clock is a high level; active state is a low level
 0 = Idle state for clock is a low level; active state is a high level

- Note 1:** This bit can only be written when the ON bit = 0. Refer to **Section 37.0 “Electrical Characteristics”** for maximum clock frequency requirements.
- 2:** This bit is not used in the Framed SPI mode. The user should program this bit to '0' for the Framed SPI mode (FRMEN = 1).
- 3:** When AUDEN = 1, the SPI/I²S module functions as if the CKP bit is equal to '1', regardless of the actual value of the CKP bit.
- 4:** This bit present for legacy compatibility and is superseded by PPS functionality on these devices (see **Section 12.4 “Peripheral Pin Select (PPS)”** for more information).

26.0 CRYPTO ENGINE

Note: This data sheet summarizes the features of the PIC32MZ EF family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 49. “Crypto Engine (CE) and Random Number Generator (RNG)”** (DS60001246) in the “PIC32 Family Reference Manual”, which is available from the Microchip web site (www.microchip.com/PIC32).

The Crypto Engine is intended to accelerate applications that need cryptographic functions. By executing these functions in the hardware module, software overhead is reduced and actions, such as encryption, decryption, and authentication can execute much more quickly.

The Crypto Engine uses an internal descriptor-based DMA for efficient programming of the security association data and packet pointers (allowing scatter/gather data fetching). An intelligent state machine schedules the Crypto Engines based on the protocol selection and packet boundaries. The hardware engines can perform the encryption and authentication in sequence or in parallel.

The following are key features of the Crypto Engine:

- Bulk ciphers and hash engines
- Integrated DMA to off-load processing:
 - Buffer descriptor-based
 - Secure association per buffer descriptor
- Some functions can execute in parallel

Bulk ciphers that are handled by the Crypto Engine include:

- AES:
 - 128-bit, 192-bit, and 256-bit key sizes
 - CBC, ECB, CTR, CFB, and OFB modes
- DES/TDES:
 - CBC, ECB, CFB, and OFB modes

Authentication engines that are available through the Crypto Engine include:

- SHA-1
- SHA-256
- MD-5
- AES-GCM
- HMAC operation (for all authentication engines)

The rate of data that can be processed by the Crypto Engine depends on these factors:

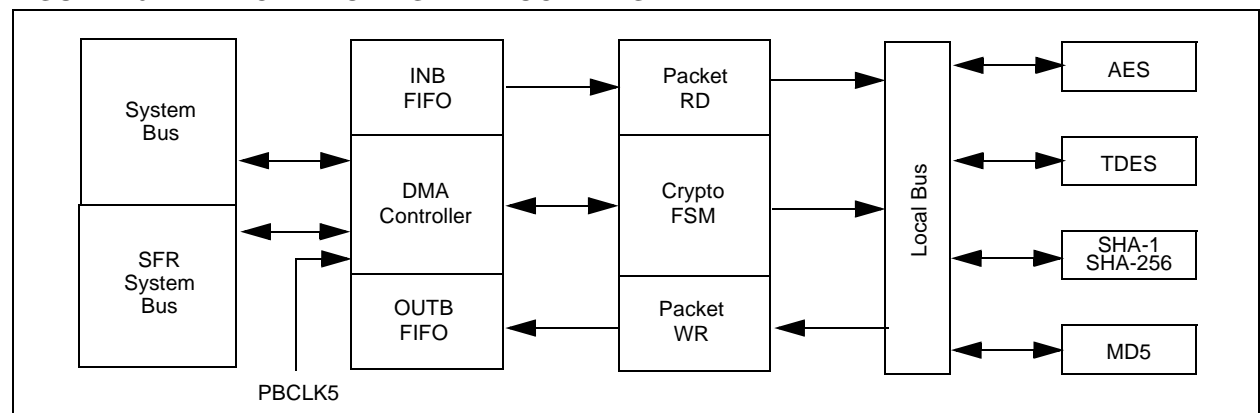
- Which engine is in use
- Whether the engines are used in parallel or in series
- The demands on source and destination memories by other parts of the system (i.e., CPU, DMA, etc.)
- The speed of PBCLK5, which drives the Crypto Engine

Table 26-1 shows typical performance for various engines.

TABLE 26-1: CRYPTO ENGINE PERFORMANCE

Engine/ Algorithm	Performance Factor (Mbps/MHz)	Maximum Mbps (PBCLK5 = 100 MHz)
DES	14.4	1440
TDES	6.6	660
AES-128	9.0	900
AES-192	7.9	790
AES-256	7.2	720
MD5	15.6	1560
SHA-1	13.2	1320
SHA-256	9.3	930

FIGURE 26-1: CRYPTO ENGINE BLOCK DIAGRAM



PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

REGISTER 26-7: CEINTEN: CRYPTO ENGINE INTERRUPT ENABLE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	AREIE	PKTIE	BDPIE	PENDIE ⁽¹⁾

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-4 **Unimplemented:** Read as '0'

bit 3 **AREIE:** Access Response Error Interrupt Enable bit

1 = Access response error interrupts are enabled

0 = Access response error interrupts are not enabled

bit 2 **PKTIE:** DMA Packet Completion Interrupt Enable bit

1 = DMA packet completion interrupts are enabled

0 = DMA packet completion interrupts are not enabled

bit 1 **BDPIE:** DMA Buffer Descriptor Processor Interrupt Enable bit

1 = BDP interrupts are enabled

0 = BDP interrupts are not enabled

bit 0 **PENDIE:** Master Interrupt Enable bit⁽¹⁾

1 = Crypto Engine interrupts are enabled

0 = Crypto Engine interrupts are not enabled

Note 1: The PENDIE bit is a global enable bit and must be enabled together with the other interrupts desired.

REGISTER 29-2: CiCFG: CAN BAUD RATE CONFIGURATION REGISTER (CONTINUED)

bit 10-8 **PRSEG<2:0>**: Propagation Time Segment bits⁽⁴⁾

111 = Length is 8 x T_Q

•
•
•

000 = Length is 1 x T_Q

bit 7-6 **SJW<1:0>**: Synchronization Jump Width bits⁽³⁾

11 = Length is 4 x T_Q

10 = Length is 3 x T_Q

01 = Length is 2 x T_Q

00 = Length is 1 x T_Q

bit 5-0 **BRP<5:0>**: Baud Rate Prescaler bits

111111 = T_Q = (2 x 64)/TPBCLK5

111110 = T_Q = (2 x 63)/TPBCLK5

•
•
•

000001 = T_Q = (2 x 2)/TPBCLK5

000000 = T_Q = (2 x 1)/TPBCLK5

Note 1: SEG2PH ≤ SEG1PH. If SEG2PHTS is clear, SEG2PH will be set automatically.

2: 3 Time bit sampling is not allowed for BRP < 2.

3: SJW ≤ SEG2PH.

4: The Time Quanta per bit must be greater than 7 (that is, T_{QBIT} > 7).

Note: This register can only be modified when the CAN module is in Configuration mode (OPMOD<2:0> (CiCON<23:21>) = 100).

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

REGISTER 29-5: CiTREC: CAN TRANSMIT/RECEIVE ERROR COUNT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	R-0	R-0	R-0	R-0	R-0	R-0
	—	—	TXBO	TXBP	RXBP	TXWARN	RXWARN	EWARN
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	TERRCNT<7:0>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	RERRCNT<7:0>							

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 31-22 **Unimplemented:** Read as '0'
- bit 21 **TXBO:** Transmitter in Error State Bus OFF (TERRCNT ≥ 256)
- bit 20 **TXBP:** Transmitter in Error State Bus Passive (TERRCNT ≥ 128)
- bit 19 **RXBP:** Receiver in Error State Bus Passive (RERRCNT ≥ 128)
- bit 18 **TXWARN:** Transmitter in Error State Warning (128 > TERRCNT ≥ 96)
- bit 17 **RXWARN:** Receiver in Error State Warning (128 > RERRCNT ≥ 96)
- bit 16 **EWARN:** Transmitter or Receiver is in Error State Warning
- bit 15-8 **TERRCNT<7:0>:** Transmit Error Counter
- bit 7-0 **RERRCNT<7:0>:** Receive Error Counter

REGISTER 29-6: CiFSTAT: CAN FIFO STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	FIFOIP31	FIFOIP30	FIFOIP29	FIFOIP28	FIFOIP27	FIFOIP26	FIFOIP25	FIFOIP24
23:16	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	FIFOIP23	FIFOIP22	FIFOIP21	FIFOIP20	FIFOIP19	FIFOIP18	FIFOIP17	FIFOIP16
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	FIFOIP15	FIFOIP14	FIFOIP13	FIFOIP12	FIFOIP11	FIFOIP10	FIFOIP9	FIFOIP8
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	FIFOIP7	FIFOIP6	FIFOIP5	FIFOIP4	FIFOIP3	FIFOIP2	FIFOIP1	FIFOIP0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 31-0 **FIFOIP<31:0>:** FIFOx Interrupt Pending bits
- 1 = One or more enabled FIFO interrupts are pending
- 0 = No FIFO interrupts are pending

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

REGISTER 29-12: CiFLTCON2: CAN FILTER CONTROL REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN11	MSEL11<1:0>		FSEL11<4:0>				
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN10	MSEL10<1:0>		FSEL10<4:0>				
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN9	MSEL9<1:0>		FSEL9<4:0>				
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN8	MSEL8<1:0>		FSEL8<4:0>				

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 31 **FLTEN11:** Filter 11 Enable bit
 1 = Filter is enabled
 0 = Filter is disabled
- bit 30-29 **MSEL11<1:0>:** Filter 11 Mask Select bits
 11 = Acceptance Mask 3 selected
 10 = Acceptance Mask 2 selected
 01 = Acceptance Mask 1 selected
 00 = Acceptance Mask 0 selected
- bit 28-24 **FSEL11<4:0>:** FIFO Selection bits
 11111 = Message matching filter is stored in FIFO buffer 31
 11110 = Message matching filter is stored in FIFO buffer 30
 •
 •
 •
 00001 = Message matching filter is stored in FIFO buffer 1
 00000 = Message matching filter is stored in FIFO buffer 0
- bit 23 **FLTEN10:** Filter 10 Enable bit
 1 = Filter is enabled
 0 = Filter is disabled
- bit 22-21 **MSEL10<1:0>:** Filter 10 Mask Select bits
 11 = Acceptance Mask 3 selected
 10 = Acceptance Mask 2 selected
 01 = Acceptance Mask 1 selected
 00 = Acceptance Mask 0 selected
- bit 20-16 **FSEL10<4:0>:** FIFO Selection bits
 11111 = Message matching filter is stored in FIFO buffer 31
 11110 = Message matching filter is stored in FIFO buffer 30
 •
 •
 •
 00001 = Message matching filter is stored in FIFO buffer 1
 00000 = Message matching filter is stored in FIFO buffer 0

Note: The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

REGISTER 29-12: CiFLTCON2: CAN FILTER CONTROL REGISTER 2 (CONTINUED)

- bit 15 **FLTEN9**: Filter 9 Enable bit
 1 = Filter is enabled
 0 = Filter is disabled
- bit 14-13 **MSEL9<1:0>**: Filter 9 Mask Select bits
 11 = Acceptance Mask 3 selected
 10 = Acceptance Mask 2 selected
 01 = Acceptance Mask 1 selected
 00 = Acceptance Mask 0 selected
- bit 12-8 **FSEL9<4:0>**: FIFO Selection bits
 11111 = Message matching filter is stored in FIFO buffer 31
 11110 = Message matching filter is stored in FIFO buffer 30
 •
 •
 •
 00001 = Message matching filter is stored in FIFO buffer 1
 00000 = Message matching filter is stored in FIFO buffer 0
- bit 7 **FLTEN8**: Filter 8 Enable bit
 1 = Filter is enabled
 0 = Filter is disabled
- bit 6-5 **MSEL8<1:0>**: Filter 8 Mask Select bits
 11 = Acceptance Mask 3 selected
 10 = Acceptance Mask 2 selected
 01 = Acceptance Mask 1 selected
 00 = Acceptance Mask 0 selected
- bit 4-0 **FSEL8<4:0>**: FIFO Selection bits
 11111 = Message matching filter is stored in FIFO buffer 31
 11110 = Message matching filter is stored in FIFO buffer 30
 •
 •
 •
 00001 = Message matching filter is stored in FIFO buffer 1
 00000 = Message matching filter is stored in FIFO buffer 0

Note: The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

TABLE 37-35: I2Cx BUS DATA TIMING REQUIREMENTS (MASTER MODE) (CONTINUED)

AC CHARACTERISTICS				Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended			
Param. No.	Symbol	Characteristics		Min. ⁽¹⁾	Max.	Units	Conditions
IM21	TR:SCL	SDAx and SCLx Rise Time	100 kHz mode	—	1000	ns	Cb is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1 Cb	300	ns	
			1 MHz mode (Note 2)	—	300	ns	
IM25	TSU:DAT	Data Input Setup Time	100 kHz mode	250	—	ns	—
			400 kHz mode	100	—	ns	
			1 MHz mode (Note 2)	100	—	ns	
IM26	THD:DAT	Data Input Hold Time	100 kHz mode	0	—	μs	—
			400 kHz mode	0	0.9	μs	
			1 MHz mode (Note 2)	0	0.3	μs	
IM30	TSU:STA	Start Condition Setup Time	100 kHz mode	TPBCLK2 * (BRG + 2)	—	μs	Only relevant for Repeated Start condition
			400 kHz mode	TPBCLK2 * (BRG + 2)	—	μs	
			1 MHz mode (Note 2)	TPBCLK2 * (BRG + 2)	—	μs	
IM31	THD:STA	Start Condition Hold Time	100 kHz mode	TPBCLK2 * (BRG + 2)	—	μs	After this period, the first clock pulse is generated
			400 kHz mode	TPBCLK2 * (BRG + 2)	—	μs	
			1 MHz mode (Note 2)	TPBCLK2 * (BRG + 2)	—	μs	
IM33	TSU:STO	Stop Condition Setup Time	100 kHz mode	TPBCLK2 * (BRG + 2)	—	μs	—
			400 kHz mode	TPBCLK2 * (BRG + 2)	—	μs	
			1 MHz mode (Note 2)	TPBCLK2 * (BRG + 2)	—	μs	
IM34	THD:STO	Stop Condition Hold Time	100 kHz mode	TPBCLK2 * (BRG + 2)	—	ns	—
			400 kHz mode	TPBCLK2 * (BRG + 2)	—	ns	
			1 MHz mode (Note 2)	TPBCLK2 * (BRG + 2)	—	ns	
IM40	TAA:SCL	Output Valid from Clock	100 kHz mode	—	3500	ns	—
			400 kHz mode	—	1000	ns	—
			1 MHz mode (Note 2)	—	350	ns	—
IM45	TBF:SDA	Bus Free Time	100 kHz mode	4.7	—	μs	The amount of time the bus must be free before a new transmission can start
			400 kHz mode	1.3	—	μs	
			1 MHz mode (Note 2)	0.5	—	μs	
IM50	Cb	Bus Capacitive Loading	—	—	—	pF	See parameter DO58
IM51	TPGD	Pulse Gobbler Delay	52	312	—	ns	See Note 3

Note 1: BRG is the value of the I²C Baud Rate Generator.

2: Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

3: The typical value for this parameter is 104 ns.

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

TABLE 37-38: ADC MODULE SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	Symbol	Characteristics	Min.	Typ.	Max.	Units	Conditions
Device Supply							
AD01	AVDD	Module VDD Supply	Greater of VDD – 0.3 or 2.1	—	Lesser of VDD + 0.3 or 3.6	V	—
AD02	AVSS	Module VSS Supply	VSS	—	VSS + 0.3	V	—
Reference Inputs							
AD05	VREFH	Reference Voltage High	VREFL + 1.8	—	AVDD	V	(Note 1)
AD06	VREFL	Reference Voltage Low	AVSS	—	VREFH – 1.8	V	(Note 1)
AD07	VREF	Absolute Reference Voltage (VREFH – VREFL)	1.8	—	AVDD	V	(Note 2)
AD08	IREF	Current Drain	—	102	—	μA	Per ADCx ('x' = 0-4, 7)
Analog Input							
AD12	VINH-VINL	Full-Scale Input Span	VREFL	—	VREFH	V	—
AD13	VINL	Absolute VINL Input Voltage	AVSS	—	VREFL	V	—
AD14	VINH	Absolute VINH Input Voltage	AVSS	—	VREFH	V	—
ADC Accuracy – Measurements with External VREF+/VREF-							
AD20c	Nr	Resolution	6	—	12	bits	Selectable 6, 8, 10, 12 Resolution Ranges
AD21c	INL	Integral Nonlinearity	—	±3	—	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.3V
AD22c	DNL	Differential Nonlinearity	—	±1	—	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.3V
AD23c	GERR	Gain Error	—	±8	—	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.3V
AD24c	EOFF	Offset Error	—	±2	—	LSb	VINL = AVSS = 0V, AVDD = 3.3V
Dynamic Performance							
AD31b	SINAD	Signal to Noise and Distortion	—	67	—	dB	Single-ended (Notes 2,3)
AD34b	ENOB	Effective Number of bits	—	10.5	—	bits	(Notes 2,3)

Note 1: These parameters are not characterized or tested in manufacturing.

2: These parameters are characterized, but not tested in manufacturing.

3: Characterized with a 1 kHz sine wave.

4: The ADC module is functional at VBORMIN < VDD < VDDMIN, but with degraded performance. Unless otherwise stated, module functionality is guaranteed, but not characterized.

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

A.9 Other Peripherals and Features

Most of the remaining peripherals on PIC32MZ EF devices act identical to their counterparts on PIC32MX-5XX/6XX/7XX devices. The main differences have to do with handling the increased peripheral bus clock speed and additional clock sources.

Table A-10 lists the differences (indicated by **Bold** type) that will affect software and hardware migration.

TABLE A-10: PERIPHERAL DIFFERENCES

PIC32MX5XX/6XX/7XX Feature	PIC32MZ EF Feature
I²C	
On PIC32MX devices, all pins are 5V-tolerant.	On PIC32MZ EF devices, the I2C4 port uses non-5V tolerant pins, and will have different VOL/VOH specifications.
I2CxBRG<11:0>	The Baud Rate Generator register has been expanded from 12 bits to 16 bits. I2CxBRG< 15:0 >
Watchdog Timer	
Clearing the Watchdog Timer on PIC32MX5XX/6XX/7XX devices required writing a '1' to the WDTCLR bit.	On PIC32MZ EF devices, the WDTCLR bit has been replaced with the 16-bit WDTCLRKEY, which must be written with a specific value (0x5743) to clear the Watchdog Timer. In addition, the WDTSPGM (DEVCFG1<21>) bit is used to control operation of the Watchdog Timer during Flash programming.
WDTCLR (WDTCON<0>)	WDTCLRKEY<15:0> (WDTCON< 31:16 >)
RTCC	
On PIC32MX devices, the output of the RTCC pin was selected between the Seconds Clock or the Alarm Pulse. RTCSECSEL (RTCCON<7>) 1 = RTCC Seconds Clock is selected for the RTCC pin 0 = RTCC Alarm Pulse is selected for the RTCC pin	On PIC32MZ EF devices, the RTCC Clock is added as an option. RTCSECSEL has been renamed RTCOUTSEL and expanded to two bits. RTCOUTSEL<1:0> (RTCCON< 8:7 >) 11 = Reserved 10 = RTCC Clock is presented on the RTCC pin 01 = Seconds Clock is presented on the RTCC pin 00 = Alarm Pulse is presented on the RTCC pin when the alarm interrupt is triggered
On PIC32MX devices, the Secondary Oscillator (SOSC) serves as the input clock for the RTCC module.	On PIC32MZ EF devices, an additional clock source, LPRC, is available as a choice for the input clock. RTCCLKSEL<1:0> (RTCCON< 10:9 >) 11 = Reserved 10 = Reserved 01 = RTCC uses the external 32.768 kHz Sosc 00 = RTCC uses the internal 32 kHz oscillator (LPRC)

Revision C (March 2016)

In this revision, the Preliminary status was removed from the document footer.

The revision also includes the following major changes, which are referenced by their respective chapter in Table C-2. In addition, minor updates to text and formatting were incorporated throughout the document.

TABLE C-2: MAJOR SECTION UPDATES

Section Name	Update Description
2.0 “Guidelines for Getting Started with 32-bit Microcontrollers”	2.9.1.3 “EMI/EMC/EFT (IEC 61000-4-4 and IEC 61000-4-2) Suppression Considerations” and Figure 2-5 were updated.
4.0 “Memory Organization”	The names of the Boot Flash Words were updated from BFXSEQ0 to BFXSEQ3 (see 4.1.1 “Boot Flash Sequence and Configuration Spaces”). The ABFXSEQx registers were removed from the Boot Flash Sequence and Configuration tables (see Table 4-2 and Table 4-3).
7.0 “CPU Exceptions and Interrupt Controller”	The Cache Error exception type was removed from the MIPS32 M-Class Microprocessor Core Exception Types (see Table 7-1).
8.0 “Oscillator Configuration”	The PLLDIV<2:0> bit value settings were updated in the SPLLCON register (see Register 8-3).
12.0 “I/O Ports”	The SIDL bit was removed from the CNCONx registers (see Table 12-4 through Table 12-21 and Register 12-3).
20.0 “Serial Quad Interface (SQI)”	The following bits were removed from the SQI1XCON1 register (see Table 20-1 and Register 20-1): DDRDATA, DDRDUMMY, DDRMODE, DDRADDR, and DDRCMD. The DDRMODE bit was removed from the SQI1CON register (see Table 20-1 and Register 20-4).
28.0 “12-bit High-Speed Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC)”	A note was added to the SELRES<1:0> bits in the ADCCON1 and ADCxTIME registers (see Register 28-1 and Register 28-27). The ADCID<2:0> bit values were updated in the ADCFSTAT register (see Register 28-22).
34.0 “Special Features”	The bit value definitions for the POSCGAIN<1:0> and SOSCGAIN<1:0> bits were updated (see Register 34-3). The Device ADC Calibration Word (DEVADCx) register was added (see Table 34-5 and Register 34-13).