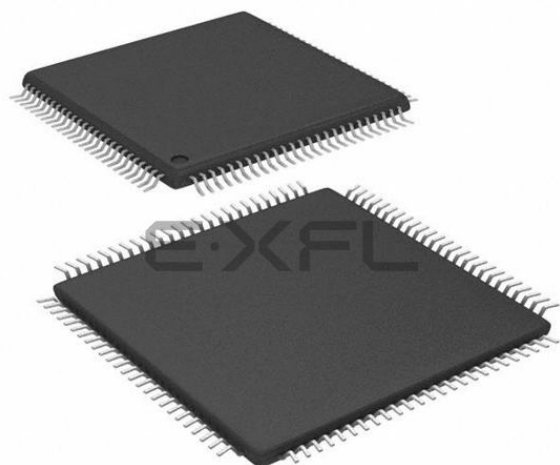




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Details

Product Status	Active
Core Processor	MIPS32® M-Class
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	EBI/EMI, Ethernet, I ² C, PMP, SPI, SQI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	78
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	2.1V ~ 3.6V
Data Converters	A/D 40x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mz2048efg100t-i-pt

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

REGISTER 4-9: SBTxRDy: SYSTEM BUS TARGET 'x' REGION 'y' READ PERMISSIONS
REGISTER ('x' = 0-13; 'y' = 0-8)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	R/W-0	R/W-1	R/W-1	R/W-1
	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

bit 31-4 **Unimplemented:** Read as '0'

bit 3 **Group3:** Group3 Read Permissions bits

1 = Privilege Group 3 has read permission

0 = Privilege Group 3 does not have read permission

bit 2 **Group2:** Group2 Read Permissions bits

1 = Privilege Group 2 has read permission

0 = Privilege Group 2 does not have read permission

bit 1 **Group1:** Group1 Read Permissions bits

1 = Privilege Group 1 has read permission

0 = Privilege Group 1 does not have read permission

bit 0 **Group0:** Group0 Read Permissions bits

1 = Privilege Group 0 has read permission

0 = Privilege Group 0 does not have read permission

Note 1: Refer to Table 4-6 for the list of available targets and their descriptions.

2: For some target regions, certain bits in this register are read-only with preset values. See Table 4-6 for more information.

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

REGISTER 5-5: NVMDATAx: FLASH DATA REGISTER (x = 0-3)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMDATA<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMDATA<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMDATA<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMDATA<7:0>							

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-0 **NVMDATA<31:0>**: Flash Data bits

Word Program: Writes NVMDATA0 to the target Flash address defined in NVMADDR

Quad Word Program: Writes NVMDATA3:NVMDATA2:NVMDATA1:NVMDATA0 to the target Flash address defined in NVMADDR. NVMDATA0 contains the Least Significant Instruction Word.

Note: The bits in this register are only reset by a Power-on Reset (POR) and are not affected by other reset sources.

REGISTER 5-6: NVMSRCADDR: SOURCE DATA ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMSRCADDR<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMSRCADDR<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMSRCADDR<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMSRCADDR<7:0>							

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-0 **NVMSRCADDR<31:0>**: Source Data Address bits

The system physical address of the data to be programmed into the Flash when the NVMOP<3:0> bits (NVMCON<3:0>) are set to perform row programming.

Note: The bits in this register are only reset by a Power-on Reset (POR) and are not affected by other reset sources.

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

REGISTER 6-3: RNMICON: NON-MASKABLE INTERRUPT (NMI) CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
	—	—	—	—	—	—	DMTO	WDTO
23:16	R/W-0	U-0	U-0	U-0	R/W-0	U-0	R/W-0	R/W-0
	SWNMI	—	—	—	GNMI	—	CF	WDTs
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NMICNT<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NMICNT<7:0>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-26 **Unimplemented:** Read as '0'

bit 25 **DMTO:** Deadman Timer Time-out Flag bit

1 = DMT time-out has occurred and caused a NMI

0 = DMT time-out has not occurred

Setting this bit will cause a DMT NMI event, and NMICNT will begin counting.

bit 24 **WDTO:** Watchdog Timer Time-Out Flag bit

1 = WDT time-out has occurred and caused a NMI

0 = WDT time-out has not occurred

Setting this bit will cause a WDT NMI event, and NMICNT will begin counting.

bit 23 **SWNMI:** Software NMI Trigger.

1 = An NMI will be generated

0 = An NMI will not be generated

bit 22-20 **Unimplemented:** Read as '0'

bit 19 **GNMI:** General NMI bit

1 = A general NMI event has been detected or a user-initiated NMI event has occurred

0 = A general NMI event has not been detected

Setting GNMI to a '1' causes a user-initiated NMI event. This bit is also set by writing 0x4E to the NMIKEY<7:0> (INTCON<31:24>) bits.

bit 18 **Unimplemented:** Read as '0'

bit 17 **CF:** Clock Fail Detect bit

1 = FSCM has detected clock failure and caused an NMI

0 = FSCM has not detected clock failure

Setting this bit will cause a CF NMI event, but will not cause a clock switch to the BFRC.

bit 16 **WDTs:** Watchdog Timer Time-out in Sleep Mode Flag bit

1 = WDT time-out has occurred during Sleep mode and caused a wake-up from sleep

0 = WDT time-out has not occurred during Sleep mode

Setting this bit will cause a WDT NMI.

bit 15-0 **NMICNT<15:0>:** NMI Reset Counter Value bits

1111111111111111-00000000000000001 = Number of SYSCLK cycles before a device Reset occurs⁽¹⁾

0000000000000000 = No delay between NMI assertion and device Reset event

Note 1: When a Watchdog Timer NMI event (when not in Sleep mode) or a Deadman Timer NMI event is triggered the NMICNT will start decrementing. When NMICNT reaches zero, the device is Reset. This NMI reset counter is only applicable to these two specific NMI events.

Note: The system unlock sequence must be performed before the SWRST bit can be written. Refer to **Section 42. "Oscillators with Enhanced PLL"** in the *"PIC32 Family Reference Manual"* for details.

TABLE 7-2: INTERRUPT IRQ, VECTOR, AND BIT LOCATION (CONTINUED)

Interrupt Source ⁽¹⁾	XC32 Vector Name	IRQ #	Vector #	Interrupt Bit Location				Persistent Interrupt
				Flag	Enable	Priority	Sub-priority	
ADC Digital Comparator 5	_ADC_DC5_VECTOR	50	OFF050<17:1>	IFS1<18>	IEC1<18>	IPC12<20:18>	IPC12<17:16>	Yes
ADC Digital Comparator 6	_ADC_DC6_VECTOR	51	OFF051<17:1>	IFS1<19>	IEC1<19>	IPC12<28:26>	IPC12<25:24>	Yes
ADC Digital Filter 1	_ADC_DF1_VECTOR	52	OFF052<17:1>	IFS1<20>	IEC1<20>	IPC13<4:2>	IPC13<1:0>	Yes
ADC Digital Filter 2	_ADC_DF2_VECTOR	53	OFF053<17:1>	IFS1<21>	IEC1<21>	IPC13<12:10>	IPC13<9:8>	Yes
ADC Digital Filter 3	_ADC_DF3_VECTOR	54	OFF054<17:1>	IFS1<22>	IEC1<22>	IPC13<20:18>	IPC13<17:16>	Yes
ADC Digital Filter 4	_ADC_DF4_VECTOR	55	OFF055<17:1>	IFS1<23>	IEC1<23>	IPC13<28:26>	IPC13<25:24>	Yes
ADC Digital Filter 5	_ADC_DF5_VECTOR	56	OFF056<17:1>	IFS1<24>	IEC1<24>	IPC14<4:2>	IPC14<1:0>	Yes
ADC Digital Filter 6	_ADC_DF6_VECTOR	57	OFF057<17:1>	IFS1<25>	IEC1<25>	IPC14<12:10>	IPC14<9:8>	Yes
ADC Fault	_ADC_FAULT_VECTOR	58	OFF058<17:1>	IFS1<26>	IEC1<26>	IPC14<20:18>	IPC14<17:16>	No
ADC Data 0	_ADC_DATA0_VECTOR	59	OFF059<17:1>	IFS1<27>	IEC1<27>	IPC14<28:26>	IPC14<25:24>	Yes
ADC Data 1	_ADC_DATA1_VECTOR	60	OFF060<17:1>	IFS1<28>	IEC1<28>	IPC15<4:2>	IPC15<1:0>	Yes
ADC Data 2	_ADC_DATA2_VECTOR	61	OFF061<17:1>	IFS1<29>	IEC1<29>	IPC15<12:10>	IPC15<9:8>	Yes
ADC Data 3	_ADC_DATA3_VECTOR	62	OFF062<17:1>	IFS1<30>	IEC1<30>	IPC15<20:18>	IPC15<17:16>	Yes
ADC Data 4	_ADC_DATA4_VECTOR	63	OFF063<17:1>	IFS1<31>	IEC1<31>	IPC15<28:26>	IPC15<25:24>	Yes
ADC Data 5	_ADC_DATA5_VECTOR	64	OFF064<17:1>	IFS2<0>	IEC2<0>	IPC16<4:2>	IPC16<1:0>	Yes
ADC Data 6	_ADC_DATA6_VECTOR	65	OFF065<17:1>	IFS2<1>	IEC2<1>	IPC16<12:10>	IPC16<9:8>	Yes
ADC Data 7	_ADC_DATA7_VECTOR	66	OFF066<17:1>	IFS2<2>	IEC2<2>	IPC16<20:18>	IPC16<17:16>	Yes
ADC Data 8	_ADC_DATA8_VECTOR	67	OFF067<17:1>	IFS2<3>	IEC2<3>	IPC16<28:26>	IPC16<25:24>	Yes
ADC Data 9	_ADC_DATA9_VECTOR	68	OFF068<17:1>	IFS2<4>	IEC2<4>	IPC17<4:2>	IPC17<1:0>	Yes
ADC Data 10	_ADC_DATA10_VECTOR	69	OFF069<17:1>	IFS2<5>	IEC2<5>	IPC17<12:10>	IPC17<9:8>	Yes
ADC Data 11	_ADC_DATA11_VECTOR	70	OFF070<17:1>	IFS2<6>	IEC2<6>	IPC17<20:18>	IPC17<17:16>	Yes
ADC Data 12	_ADC_DATA12_VECTOR	71	OFF071<17:1>	IFS2<7>	IEC2<7>	IPC17<28:26>	IPC17<25:24>	Yes
ADC Data 13	_ADC_DATA13_VECTOR	72	OFF072<17:1>	IFS2<8>	IEC2<8>	IPC18<4:2>	IPC18<1:0>	Yes
ADC Data 14	_ADC_DATA14_VECTOR	73	OFF073<17:1>	IFS2<9>	IEC2<9>	IPC18<12:10>	IPC18<9:8>	Yes
ADC Data 15	_ADC_DATA15_VECTOR	74	OFF074<17:1>	IFS2<10>	IEC2<10>	IPC18<20:18>	IPC18<17:16>	Yes
ADC Data 16	_ADC_DATA16_VECTOR	75	OFF075<17:1>	IFS2<11>	IEC2<11>	IPC18<28:26>	IPC18<25:24>	Yes
ADC Data 17	_ADC_DATA17_VECTOR	76	OFF076<17:1>	IFS2<12>	IEC2<12>	IPC19<4:2>	IPC19<1:0>	Yes
ADC Data 18	_ADC_DATA18_VECTOR	77	OFF077<17:1>	IFS2<13>	IEC2<13>	IPC19<12:10>	IPC19<9:8>	Yes

Note 1: Not all interrupt sources are available on all devices. See **TABLE 1: “PIC32MZ EF Family Features”** for the list of available peripherals.

- 2:** This interrupt source is not available on 64-pin devices.
3: This interrupt source is not available on 100-pin devices.
4: This interrupt source is not available on 124-pin devices.

TABLE 7-3: INTERRUPT REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name ⁽¹⁾	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
00F0	IEC3 ⁽⁶⁾	31:16	CNKIE	CNJIE	CNHIE	CNGIE	CNFIE	CNEIE	CNDIE	CNCIE	CNBIE	CNAIE	I2C1MIE	I2C1SIE	I2C1BIE	U1TXIE	U1RXIE	U1EIE	0000
		15:0	SPI1TXIE	SPI1RXIE	SPI1EIE	—	CRPTIE ⁽⁷⁾	SBIE	CFDCIE	CPCIE	ADCD44IE	ADCD43IE	ADCD42IE	ADCD41IE	ADCD40IE	ADCD39IE	ADCD38IE	ADCD37IE	0000
0100	IEC4	31:16	U3TXIE	U3RXIE	U3EIE	SPI3TXIE	SPI3RXIE	SPI3EIE	ETHIE	CAN2IE ⁽³⁾	CAN1IE ⁽³⁾	I2C2MIE ⁽²⁾	I2C2SIE ⁽²⁾	I2C2BIE ⁽²⁾	U2TXIE	U2RXIE	U2EIE	SPI2TXIE	0000
		15:0	SPI2RXIE	SPI2EIE	DMA7IE	DMA6IE	DMA5IE	DMA4IE	DMA3IE	DMA2IE	DMA1IE	DMA0IE	USBDMAIE	USBIE	CMP2IE	CMP1IE	PMPEIE	PMPIE	0000
0110	IEC5	31:16	—	U6TXIE	U6RXIE	U6EIE	SPI6TXIE ⁽²⁾	SPI6RXIE ⁽²⁾	SPI6EIE ⁽²⁾	I2C5MIE	I2C5SIE	I2C5BIE	U5TXIE	U5RXIE	U5EIE	SPI5TXIE ⁽²⁾	SPI5RXIE ⁽²⁾	SPI5EIE ⁽²⁾	0000
		15:0	I2C4MIE	I2C4SIE	I2C4BIE	U4TXIE	U4RXIE	U4EIE	SQ11IE	PREIE	FCEIE	RTCCIE	SPI4TXIE	SPI4RXIE	SPI4EIE	I2C3MIE	I2C3SIE	I2C3BIE	0000
0120	IEC6	31:16	—	—	—	—	—	—	—	—	—	—	ADC7WIE	—	—	ADC4WIE	ADC3WIE	ADC2WIE	0000
		15:0	ADC1WIE	ADC0WIE	ADC7EIE	—	—	ADC4EIE	ADC3EIF	ADC2EIE	ADC1EIE	ADC0EIE	—	ADCGRPIE	—	ADCURDYIE	ADCARDYIE	ADCEOSIE	0000
0140	IPC0	31:16	—	—	—	—	INT0IP<2:0>		INT0IS<1:0>		—	—	—	—	CS1IP<2:0>		CS1IS<1:0>		0000
		15:0	—	—	—	—	CS0IP<2:0>		CS0IS<1:0>		—	—	—	—	CTIP<2:0>		CTIS<1:0>		0000
0150	IPC1	31:16	—	—	—	—	OC1IP<2:0>		OC1IS<1:0>		—	—	—	—	IC1IP<2:0>		IC1IS<1:0>		0000
		15:0	—	—	—	—	IC1EIP<2:0>		IC1EIS<1:0>		—	—	—	—	T1IP<2:0>		T1IS<1:0>		0000
0160	IPC2	31:16	—	—	—	—	IC2IP<2:0>		IC2IS<1:0>		—	—	—	—	IC2EIP<2:0>		IC2EIS<1:0>		0000
		15:0	—	—	—	—	T2IP<2:0>		T2IS<1:0>		—	—	—	—	INT1IP<2:0>		INT1IS<1:0>		0000
0170	IPC3	31:16	—	—	—	—	IC3EIP<2:0>		IC3EIS<1:0>		—	—	—	—	T3IP<2:0>		T3IS<1:0>		0000
		15:0	—	—	—	—	INT2IP<2:0>		INT2IS<1:0>		—	—	—	—	OC2IP<2:0>		OC2IS<1:0>		0000
0180	IPC4	31:16	—	—	—	—	T4IP<2:0>		T4IS<1:0>		—	—	—	—	INT3IP<2:0>		INT3IS<1:0>		0000
		15:0	—	—	—	—	OC3IP<2:0>		OC3IS<1:0>		—	—	—	—	IC3IP<2:0>		IC3IS<1:0>		0000
0190	IPC5	31:16	—	—	—	—	INT4IP<2:0>		INT4IS<1:0>		—	—	—	—	OC4IP<2:0>		OC4IS<1:0>		0000
		15:0	—	—	—	—	IC4IP<2:0>		IC4IS<1:0>		—	—	—	—	IC4EIP<2:0>		IC4EIS<1:0>		0000
01A0	IPC6	31:16	—	—	—	—	OC5IP<2:0>		OC5IS<1:0>		—	—	—	—	IC5IP<2:0>		IC5IS<1:0>		0000
		15:0	—	—	—	—	IC5EIP<2:0>		IC5EIS<1:0>		—	—	—	—	T5IP<2:0>		T5IS<1:0>		0000
01B0	IPC7	31:16	—	—	—	—	OC6IP<2:0>		OC6IS<1:0>		—	—	—	—	IC6IP<2:0>		IC6IS<1:0>		0000
		15:0	—	—	—	—	IC6EIP<2:0>		IC6EIS<1:0>		—	—	—	—	T6IP<2:0>		T6IS<1:0>		0000
01C0	IPC8	31:16	—	—	—	—	OC7IP<2:0>		OC7IS<1:0>		—	—	—	—	IC7IP<2:0>		IC7IS<1:0>		0000
		15:0	—	—	—	—	IC7EIP<2:0>		IC7EIS<1:0>		—	—	—	—	T7IP<2:0>		T7IS<1:0>		0000
01D0	IPC9	31:16	—	—	—	—	OC8IP<2:0>		OC8IS<1:0>		—	—	—	—	IC8IP<2:0>		IC8IS<1:0>		0000
		15:0	—	—	—	—	IC8EIP<2:0>		IC8EIS<1:0>		—	—	—	—	T8IP<2:0>		T8IS<1:0>		0000
01E0	IPC10	31:16	—	—	—	—	OC9IP<2:0>		OC9IS<1:0>		—	—	—	—	IC9IP<2:0>		IC9IS<1:0>		0000
		15:0	—	—	—	—	IC9EIP<2:0>		IC9EIS<1:0>		—	—	—	—	T9IP<2:0>		T9IS<1:0>		0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

- Note** 1: All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 “CLR, SET, and INV Registers”** for more information.
- 2: This bit or register is not available on 64-pin devices.
- 3: This bit or register is not available on devices without a CAN module.
- 4: This bit or register is not available on 100-pin devices.
- 5: Bits 31 and 30 are not available on 64-pin and 100-pin devices; bits 29 through 14 are not available on 64-pin devices.
- 6: Bits 31, 30, 29, and bits 5 through 0 are not available on 64-pin and 100-pin devices; bit 31 is not available on 124-pin devices; bit 22 is not available on 64-pin devices.
- 7: This bit or register is not available on devices without a Crypto module.
- 8: This bit or register is not available on 124-pin devices.

TABLE 7-3: INTERRUPT REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name ⁽¹⁾	Bit Range	Bits															All Resets	
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1		16/0
081C	OFF183	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0820	OFF184	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0824	OFF185 ⁽²⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0828	OFF186 ⁽²⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
082C	OFF187 ⁽²⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0830	OFF188	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0834	OFF189	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0838	OFF190	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0840	OFF192	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0844	OFF193	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0848	OFF194	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0850	OFF196	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0858	OFF198	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
085C	OFF199	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0860	OFF200	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

- Note** 1: All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 “CLR, SET, and INV Registers”** for more information.
- 2: This bit or register is not available on 64-pin devices.
- 3: This bit or register is not available on devices without a CAN module.
- 4: This bit or register is not available on 100-pin devices.
- 5: Bits 31 and 30 are not available on 64-pin and 100-pin devices; bits 29 through 14 are not available on 64-pin devices.
- 6: Bits 31, 30, 29, and bits 5 through 0 are not available on 64-pin and 100-pin devices; bit 31 is not available on 124-pin devices; bit 22 is not available on 64-pin devices.
- 7: This bit or register is not available on devices without a Crypto module.
- 8: This bit or register is not available on 124-pin devices.

REGISTER 7-2: PRISS: PRIORITY SHADOW SELECT REGISTER (CONTINUED)

bit 15-12 **PRI3SS<3:0>**: Interrupt with Priority Level 3 Shadow Set bits⁽¹⁾

1xxx = Reserved (by default, an interrupt with a priority level of 3 uses Shadow Set 0)

0111 = Interrupt with a priority level of 3 uses Shadow Set 7

0110 = Interrupt with a priority level of 3 uses Shadow Set 6

.
.
.

0001 = Interrupt with a priority level of 3 uses Shadow Set 1

0000 = Interrupt with a priority level of 3 uses Shadow Set 0

bit 11-8 **PRI2SS<3:0>**: Interrupt with Priority Level 2 Shadow Set bits⁽¹⁾

1xxx = Reserved (by default, an interrupt with a priority level of 2 uses Shadow Set 0)

0111 = Interrupt with a priority level of 2 uses Shadow Set 7

0110 = Interrupt with a priority level of 2 uses Shadow Set 6

.
.
.

0001 = Interrupt with a priority level of 2 uses Shadow Set 1

0000 = Interrupt with a priority level of 2 uses Shadow Set 0

bit 7-4 **PRI1SS<3:0>**: Interrupt with Priority Level 1 Shadow Set bits⁽¹⁾

1xxx = Reserved (by default, an interrupt with a priority level of 1 uses Shadow Set 0)

0111 = Interrupt with a priority level of 1 uses Shadow Set 7

0110 = Interrupt with a priority level of 1 uses Shadow Set 6

.
.
.

0001 = Interrupt with a priority level of 1 uses Shadow Set 1

0000 = Interrupt with a priority level of 1 uses Shadow Set 0

bit 3-1 **Unimplemented**: Read as '0'

bit 0 **SS0**: Single Vector Shadow Register Set bit

1 = Single vector is presented with a shadow set

0 = Single vector is not presented with a shadow set

Note 1: These bits are ignored if the MVEC bit (INTCON<12>) = 0.

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

REGISTER 8-8: CLKSTAT: OSCILLATOR CLOCK STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —
23:16	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —
15:8	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —
7:0	U-0 —	U-0 —	R-0 LPRCRDY	R-0 SOSCRDY	U-0 —	R-0 POSCRDY	R-0 DIVSPLLRDY	R-0 FRCRDY

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-6 **Unimplemented:** Read as '0'

bit 5 **LPRCRDY:** Low-Power RC (LPRC) Oscillator Ready Status bit

1 = LPRC is stable and ready

0 = LPRC is disabled or not operating

bit 4 **SOSCRDY:** Secondary Oscillator (Sosc) Ready Status bit

1 = Sosc is stable and ready

0 = Sosc is disabled or not operating

bit 3 **Unimplemented:** Read as '0'

bit 2 **POSCRDY:** Primary Oscillator (Posc) Ready Status bit

1 = Posc is stable and ready

0 = Posc is disabled or not operating

bit 1 **DIVSPLLRDY:** Divided System PLL Ready Status bit

1 = Divided System PLL is ready

0 = Divided System PLL is not ready

bit 0 **FRCRDY:** Fast RC (FRC) Oscillator Ready Status bit

1 = FRC is stable and ready

0 = FRC is disabled for not operating

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

REGISTER 11-10: USBIENCSR2: USB INDEXED ENDPOINT CONTROL STATUS REGISTER 2 (ENDPOINT 1-7)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	TXINTERV<7:0>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SPEED<1:0>		PROTOCOL<1:0>		TEP<3:0>			
15:8	U-0	U-0	R-0	R-0	R-0	R-0	R-0	R-0
	—	—	RXCNT<13:8>					
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	RXCNT<7:0>							

Legend:

R = Readable bit
-n = Value at POR

HC = Hardware Cleared
W = Writable bit
'1' = Bit is set

HS = Hardware Set
U = Unimplemented bit, read as '0'
'0' = Bit is cleared
x = Bit is unknown

bit 31-24 **TXINTERV<7:0>**: Endpoint TX Polling Interval/NAK Limit bits (*Host mode*)

For Interrupt and Isochronous transfers, this field defines the polling interval for the endpoint. For Bulk endpoints, this field sets the number of frames/microframes after which the endpoint should time out on receiving a stream of NAK responses.

The following table describes the valid values and interpretation for these bits:

Transfer Type	Speed	Valid Values (m)	Interpretation
Interrupt	Low/Full	0x01 to 0xFF	Polling interval is 'm' frames.
	High	0x01 to 0x10	Polling interval is $2^{(m-1)}$ frames.
Isochronous	Full or High	0x01 to 0x10	Polling interval is $2^{(m-1)}$ frames/microframes.
Bulk	Full or High	0x02 to 0x10	NAK limit is $2^{(m-1)}$ frames/microframes. A value of '0' or '1' disables the NAK time-out function.

bit 23-22 **SPEED<1:0>**: TX Endpoint Operating Speed Control bits (*Host mode*)

11 = Low-Speed
10 = Full-Speed
01 = Hi-Speed
00 = Reserved

bit 21-20 **PROTOCOL<1:0>**: TX Endpoint Protocol Control bits

11 = Interrupt
10 = Bulk
01 = Isochronous
00 = Control

bit 19-16 **TEP<3:0>**: TX Target Endpoint Number bits

This value is the endpoint number contained in the TX endpoint descriptor returned to the USB module during device enumeration.

bit 15-14 **Unimplemented**: Read as '0'

bit 13-0 **RXCNT<13:0>**: Receive Count bits

The number of received data bytes in the endpoint RX FIFO. The value returned changes as the contents of the FIFO change and is only valid while RXPKTRDY is set.

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REGISTER 11-16: USBINFO: USB INFORMATION REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0
	VPLEN<7:0>							
23:16	R/W-0	R/W-1	R/W-0	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0
	WTCON<3:0>				WTID<3:0>			
15:8	R-1	R-0	R-0	R-0	R-1	R-1	R-0	R-0
	DMACHANS<3:0>				RAMBITS<3:0>			
7:0	R-0	R-1	R-1	R-1	R-0	R-1	R-1	R-1
	RXENDPTS<3:0>				TXENDPTS<3:0>			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-24 **VPLEN<7:0>**: Vbus pulsing charge length bits

Sets the duration of the Vbus pulsing charge in units of 546.1 μ s. (The default setting corresponds to 32.77 ms.)

bit 23-20 **WTCON<3:0>**: Connect/Disconnect filter control bits

Sets the wait to be applied to allow for the connect/disconnect filter in units of 533.3 ns. The default setting corresponds to 2.667 μ s.

bit 19-6 **WTID<3:0>**: ID delay valid control bits

Sets the delay to be applied from IDPULLUP being asserted to IDDIG being considered valid in units of 4.369ms. The default setting corresponds to 52.43ms.

bit 15-12 **DMACHANS<3:0>**: DMA Channels bits

These read-only bits provide the number of DMA channels in the USB module. For the PIC32MZ EF family, this number is 8.

bit 11-8 **RAMBITS<3:0>**: RAM address bus width bits

These read-only bits provide the width of the RAM address bus. For the PIC32MZ EF family, this number is 12.

bit 7-4 **RXENDPTS<3:0>**: Included RX Endpoints bits

This read-only register gives the number of RX endpoints in the design. For the PIC32MZ EF family, this number is 7.

bit 3-0 **TXENDPTS<3:0>**: Included TX Endpoints bits

These read-only bits provide the number of TX endpoints in the design. For the PIC32MZ EF family, this number is 7.

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

REGISTER 11-28: USBLPMR1: USB LINK POWER MANAGEMENT CONTROL REGISTER 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	LPMERRIE	LPMRESIE	LPMACKIE	LPMNYIE	LPMSTIE	LPMTIOE
23:16	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0, HC	R/W-0, HC
	—	—	—	LPMNAK	LPMEN<1:0>		LPMRES	LPMXMT
15:8	R-0	R-0	R-0	R-0	U-0	U-0	U-0	R-0
	ENDPOINT<3:0>				—	—	—	RMTWAK
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	HIRD<3:0>				LNKSTATE<3:0>			

Legend:

R = Readable bit

-n = Value at POR

HC = Hardware Cleared

W = Writable bit

'1' = Bit is set

U = Unimplemented bit, read as '0'

'0' = Bit is cleared

x = Bit is unknown

bit 31-30 **Unimplemented:** Read as '0'

bit 29 **LPMERRIE:** LPM Error Interrupt Enable bit

1 = LPMERR interrupt is enabled

0 = LPMERR interrupt is disabled

bit 28 **LPMRESIE:** LPM Resume Interrupt Enable bit

1 = LPMRES interrupt is enabled

0 = LPMRES interrupt is disabled

bit 27 **LPMACKIE:** LPM Acknowledge Interrupt Enable bit

1 = Enable the LPMACK Interrupt

0 = Disable the LPMACK Interrupt

bit 26 **LPMNYIE:** LPM NYET Interrupt Enable bit

1 = Enable the LPMNYET Interrupt

0 = Disable the LPMNYET Interrupt

bit 25 **LPMSTIE:** LPM STALL Interrupt Enable bit

1 = Enable the LPMST Interrupt

0 = Disable the LPMST Interrupt

bit 24 **LPMTIOE:** LPM Time-out Interrupt Enable bit

1 = Enable the LPMTIO Interrupt

0 = Disable the LPMTIO Interrupt

bit 23-21 **Unimplemented:** Read as '0'

bit 20 **LPMNAK:** LPM-only Transaction Setting bit

1 = All endpoints will respond to all transactions other than a LPM transaction with a NAK

0 = Normal transaction operation

Setting this bit to '1' will only take effect after the USB module has been LPM suspended.

bit 19-18 **LPMEN<1:0>:** LPM Enable bits (*Device mode*)

11 = LPM Extended transactions are supported

10 = LPM and Extended transactions are not supported

01 = LPM mode is not supported but Extended transactions are supported

00 = LPM Extended transactions are supported

bit 17 **LPMRES:** LPM Resume bit

1 = Initiate resume (remote wake-up). Resume signaling is asserted for 50 μ s.

0 = No resume operation

This bit is self-clearing.

TABLE 12-16: PORTG REGISTER MAP FOR 64-PIN DEVICES ONLY

Virtual Address (BF86_#)	Register Name(s)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0600	ANSELG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	ANSG9	ANSG8	ANSG7	ANSG6	—	—	—	—	—	—	03C0
0610	TRISG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	TRISG9	TRISG8	TRISG7	TRISG6	—	—	—	—	—	—	03C0
0620	PORTG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	RG9	RG8	RG7	RG6	—	—	—	—	—	—	xxxx
0630	LATG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	LATG9	LATG8	LATG7	LATG6	—	—	—	—	—	—	xxxx
0640	ODCG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	ODCG9	ODCG8	ODCG7	ODCG6	—	—	—	—	—	—	0000
0650	CNPUG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CNPUG9	CNPUG8	CNPUG7	CNPUG6	—	—	—	—	—	—	0000
0660	CNPDG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CNPDG9	CNPDG8	CNPDG7	CNPDG6	—	—	—	—	—	—	0000
0670	CNCONG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	EDGE DETECT	—	—	—	—	—	—	—	—	—	—	—	0000
0680	CNENG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CNENG9	CNENG8	CNENG7	CNENG6	—	—	—	—	—	—	0000
0690	CNSTATG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CN STATG9	CN STATG8	CN STATG7	CN STATG6	—	—	—	—	—	—	0000
06A0	CNNEG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CNNEG9	CNNEG8	CNNEG7	CNNEG6	—	—	—	—	—	—	0000
06B0	CNFG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CNFG9	CNFG8	CNFG7	CNFG6	—	—	—	—	—	—	0000
06C0	SRCON0G	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	SR0G9	—	—	SR0G6	—	—	—	—	—	—	0000
06D0	SRCON1G	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	SR1G9	—	—	SR1G6	—	—	—	—	—	—	0000

Legend: x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 “CLR, SET, and INV Registers”** for more information.

TABLE 12-23: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
1538	RPA14R ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPA14R<3:0>				0000
153C	RPA15R ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPA15R<3:0>				0000
1540	RPB0R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPB0R<3:0>				0000
1544	RPB1R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPB1R<3:0>				0000
1548	RPB2R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPB2R<3:0>				0000
154C	RPB3R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPB3R<3:0>				0000
1554	RPB5R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPB5R<3:0>				0000
1558	RPB6R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPB6R<3:0>				0000
155C	RPB7R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPB7R<3:0>				0000
1560	RPB8R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPB8R<3:0>				0000
1564	RPB9R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPB9R<3:0>				0000
1568	RPB10R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPB10R<3:0>				0000
1578	RPB14R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPB14R<3:0>				0000
157C	RPB15R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPB15R<3:0>				0000
1584	RPC1R ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPC1R<3:0>				0000
1588	RPC2R ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPC2R<3:0>				0000
158C	RPC3R ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPC3R<3:0>				0000
1590	RPC4R ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPC4R<3:0>				0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

- Note** 1: This register is not available on 64-pin devices.
 2: This register is not available on 64-pin and 100-pin devices.

22.0 UNIVERSAL ASYNCHRONOUS RECEIVER TRANSMITTER (UART)

Note: This data sheet summarizes the features of the PIC32MZ EF family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 21. “Universal Asynchronous Receiver Transmitter (UART)”** (DS60001107) in the “PIC32 Family Reference Manual”, which is available from the Microchip web site (www.microchip.com/PIC32).

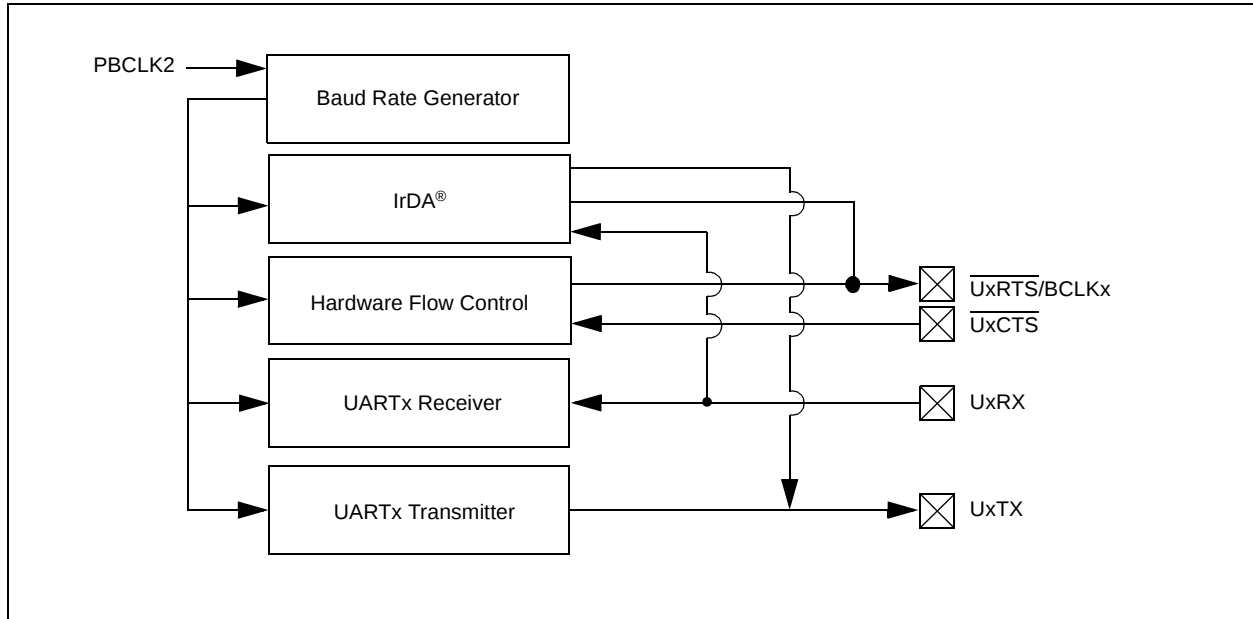
The UART module is one of the serial I/O modules available in the PIC32MZ EF family of devices. The UART is a full-duplex, asynchronous communication channel that communicates with peripheral devices and personal computers through protocols, such as RS-232, RS-485, LIN, and IrDA®. The module also supports the hardware flow control option, with $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$ pins, and also includes an IrDA encoder and decoder.

The primary features of the UART module are:

- Full-duplex, 8-bit or 9-bit data transmission
- Even, Odd or No Parity options (for 8-bit data)
- One or two Stop bits
- Hardware auto-baud feature
- Hardware flow control option
- Fully integrated Baud Rate Generator (BRG) with 16-bit prescaler
- Baud rates ranging from 76 bps to 25 Mbps at 100 MHz (PBCLK2)
- 8-level deep First-In-First-Out (FIFO) transmit data buffer
- 8-level deep FIFO receive data buffer
- Parity, framing and buffer overrun error detection
- Support for interrupt-only on address detect (9th bit = 1)
- Separate transmit and receive interrupts
- Loopback mode for diagnostic support
- LIN Protocol support
- IrDA encoder and decoder with 16x baud clock output for external IrDA encoder/decoder support

Figure 22-1 illustrates a simplified block diagram of the UART module.

FIGURE 22-1: UART SIMPLIFIED BLOCK DIAGRAM



REGISTER 28-20: ADCCMPCON1: ADC DIGITAL COMPARATOR 1 CONTROL REGISTER

- bit 3 **IEHIHI:** High/High Digital Comparator 0 Event bit
1 = Generate a Digital Comparator 0 Event when $DCMPHI<15:0> \leq DATA<31:0>$
0 = Do not generate an event
- bit 2 **IEHILO:** High/Low Digital Comparator 0 Event bit
1 = Generate a Digital Comparator 0 Event when $DATA<31:0> < DCMPHI<15:0>$
0 = Do not generate an event
- bit 1 **IELOHI:** Low/High Digital Comparator 0 Event bit
1 = Generate a Digital Comparator 0 Event when $DCMPLO<15:0> \leq DATA<31:0>$
0 = Do not generate an event
- bit 0 **IELOLO:** Low/Low Digital Comparator 0 Event bit
1 = Generate a Digital Comparator 0 Event when $DATA<31:0> < DCMPLO<15:0>$
0 = Do not generate an event

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REGISTER 29-2: CcCFG: CAN BAUD RATE CONFIGURATION REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	WAKFIL	—	—	—	SEG2PH<2:0> ^(1,4)		
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SEG2PHTS ⁽¹⁾	SAM ⁽²⁾	SEG1PH<2:0>			PRSEG<2:0>		
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SJW<1:0> ⁽³⁾		BRP<5:0>					

Legend: HC = Hardware Clear S = Settable bit
R = Readable bit W = Writable bit P = Programmable bit r = Reserved bit
U = Unimplemented bit -n = Bit Value at POR: ('0', '1', x = Unknown)

bit 31-23 **Unimplemented:** Read as '0'

bit 22 **WAKFIL:** CAN Bus Line Filter Enable bit
1 = Use CAN bus line filter for wake-up
0 = CAN bus line filter is not used for wake-up

bit 21-19 **Unimplemented:** Read as '0'

bit 18-16 **SEG2PH<2:0>:** Phase Buffer Segment 2 bits^(1,4)
111 = Length is 8 x Tq
•
•
•

000 = Length is 1 x Tq

bit 15 **SEG2PHTS:** Phase Segment 2 Time Select bit⁽¹⁾
1 = Freely programmable
0 = Maximum of SEG1PH or Information Processing Time, whichever is greater

bit 14 **SAM:** Sample of the CAN Bus Line bit⁽²⁾
1 = Bus line is sampled three times at the sample point
0 = Bus line is sampled once at the sample point

bit 13-11 **SEG1PH<2:0>:** Phase Buffer Segment 1 bits⁽⁴⁾
111 = Length is 8 x Tq
•
•
•

000 = Length is 1 x Tq

- Note 1:** $SEG2PH \leq SEG1PH$. If SEG2PHTS is clear, SEG2PH will be set automatically.
2: 3 Time bit sampling is not allowed for BRP < 2.
3: $SJW \leq SEG2PH$.
4: The Time Quanta per bit must be greater than 7 (that is, TQBIT > 7).

Note: This register can only be modified when the CAN module is in Configuration mode (OPMOD<2:0> (CiCON<23:21>) = 100).

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REGISTER 30-22: ETHALGNERR: ETHERNET CONTROLLER ALIGNMENT ERRORS STATISTICS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ALGNERRCNT<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ALGNERRCNT<7:0>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **ALGNERRCNT<15:0>:** Alignment Error Count bits

Increment count for frames with alignment errors. Note that an alignment error is a frame that has an FCS error and the frame length in bits is not an integral multiple of 8 bits (a.k.a., dribble nibble)

Note 1: This register is only used for RX operations.

2: This register is automatically cleared by hardware after a read operation, unless the byte enables for bytes 0/1 are '0'.

3: It is recommended to use the SET, CLR, or INV registers to set or clear any bit in this register. Setting or clearing any bits in this register should be only done for debug/test purposes.

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

TABLE 33-1: PERIPHERAL MODULE DISABLE BITS AND LOCATIONS⁽¹⁾ (CONTINUED)

Peripheral	PMDx bit Name	Register Name and Bit Location
UART3	U3MD	PMD5<2>
UART4	U4MD	PMD5<3>
UART5	U5MD	PMD5<4>
UART6	U6MD	PMD5<5>
SPI1	SPI1MD	PMD5<8>
SPI2	SPI2MD	PMD5<9>
SPI3	SPI3MD	PMD5<10>
SPI4	SPI4MD	PMD5<11>
SPI5	SPI5MD	PMD5<12>
SPI6	SPI6MD	PMD5<13>
I2C1	I2C1MD	PMD5<16>
I2C2	I2C2MD	PMD5<17>
I2C3	I2C3MD	PMD5<18>
I2C4	I2C4MD	PMD5<19>
I2C5	I2C5MD	PMD5<20>
USB ⁽²⁾	USBMD	PMD5<24>
CAN1	CAN1MD	PMD5<28>
CAN2	CAN2MD	PMD5<29>
RTCC	RTCCMD	PMD6<0>
Reference Clock Output 1	REFO1MD	PMD6<8>
Reference Clock Output 2	REFO2MD	PMD6<9>
Reference Clock Output 3	REFO3MD	PMD6<10>
Reference Clock Output 4	REFO4MD	PMD6<11>
PMP	PMPMD	PMD6<16>
EBI	EBIMD	PMD6<17>
SQI1	SQI1MD	PMD6<23>
Ethernet	ETHMD	PMD6<28>
DMA	DMAMD	PMD7<4>
Random Number Generator	RNGMD	PMD7<20>
Crypto	CRYPTMD	PMD7<22>

Note 1: Not all modules and associated PMDx bits are available on all devices. See **TABLE 1: “PIC32MZ EF Family Features”** for the lists of available peripherals.

2: Module must not be busy after clearing the associated ON bit and prior to setting the USBMD bit.

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TABLE 37-39: ANALOG-TO-DIGITAL CONVERSION TIMING REQUIREMENTS

AC CHARACTERISTICS ⁽²⁾			Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	Symbol	Characteristics	Min.	Typ. ⁽¹⁾	Max.	Units	Conditions
Clock Parameters							
AD50	TAD	ADC Clock Period	20	—	6250	ns	—
Throughput Rate							
AD51	FTP	Sample Rate for ADC0-ADC4 (Class 1 Inputs)	—	—	3.125	Msp	12-bit resolution Source Impedance ≤ 200Ω
			—	—	3.57	Msp	10-bit resolution Source Impedance ≤ 200Ω
			—	—	4.16	Msp	8-bit resolution Source Impedance ≤ 200Ω
			—	—	5	Msp	6-bit resolution Source Impedance ≤ 200Ω
		Sample Rate for ADC7 (Class 2 and Class 3 Inputs)	—	—	2.94	Msp	12-bit resolution Source Impedance ≤ 200Ω
			—	—	3.33	Msp	10-bit resolution Source Impedance ≤ 200Ω
			—	—	3.84	Msp	8-bit resolution Source Impedance ≤ 200Ω
			—	—	4.55	Msp	6-bit resolution Source Impedance ≤ 200Ω
Timing Parameters							
AD60	TSAMP	Sample Time for ADC0-ADC4 (Class 1 Inputs)	3	—	—	TAD	Source Impedance ≤ 200Ω, Max ADC clock Source Impedance ≤ 500Ω, Max ADC clock Source Impedance ≤ 1 KΩ, Max ADC clock Source Impedance ≤ 5 KΩ, Max ADC clock
			4				
			5				
			13				
		Sample Time for ADC7 (Class 2 and 3 Inputs)	4	—	—	TAD	Source Impedance ≤ 200Ω, Max ADC clock Source Impedance ≤ 500Ω, Max ADC clock Source Impedance ≤ 1 KΩ, Max ADC clock Source Impedance ≤ 5 KΩ, Max ADC clock
			5				
			6				
			14				
		Sample Time for ADC7 (Class 2 and 3 Inputs)	See Table 37-40	—	—	TAD	CVDEN (ADCCON1<11>) = 1
AD62	TCONV	Conversion Time (after sample time is complete)	—	—	13	TAD	12-bit resolution 10-bit resolution 8-bit resolution 6-bit resolution
			—				
			—				
			—				
AD65	TWAKE	Wake-up time from Low- Power Mode	—	500	—	TAD	Lesser of 500 TAD or 20 μs.
			—	20	—	μs	

Note 1: These parameters are characterized, but not tested in manufacturing.

2: The ADC module is functional at VBORMIN < VDD < VDDMIN, but with degraded performance. Unless otherwise stated, module functionality is guaranteed, but not characterized.

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TABLE 37-40: ADC SAMPLE TIMES WITH CVD ENABLED

AC CHARACTERISTICS ⁽²⁾			Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	Symbol	Characteristics	Min.	Typ. ⁽¹⁾	Max.	Units	Conditions
AD60a	TSAMP	Sample Time for ADC7 (Class 2 and Class 3 Inputs) with the CVDEN bit (ADCCON1<11>) = 1	8	—	—	TAD	Source Impedance ≤ 200Ω CVDCPL<2:0> (ADCCON2<28:26>) = 001
			9				CVDCPL<2:0> (ADCCON2<28:26>) = 010
			11				CVDCPL<2:0> (ADCCON2<28:26>) = 011
			12				CVDCPL<2:0> (ADCCON2<28:26>) = 100
			14				CVDCPL<2:0> (ADCCON2<28:26>) = 101
			16				CVDCPL<2:0> (ADCCON2<28:26>) = 110
			17				CVDCPL<2:0> (ADCCON2<28:26>) = 111
			10	—	—	TAD	Source Impedance ≤ 500Ω CVDCPL<2:0> (ADCCON2<28:26>) = 001
			12				CVDCPL<2:0> (ADCCON2<28:26>) = 010
			14				CVDCPL<2:0> (ADCCON2<28:26>) = 011
			16				CVDCPL<2:0> (ADCCON2<28:26>) = 100
			18				CVDCPL<2:0> (ADCCON2<28:26>) = 101
			19				CVDCPL<2:0> (ADCCON2<28:26>) = 110
			21				CVDCPL<2:0> (ADCCON2<28:26>) = 111
			13	—	—	TAD	Source Impedance ≤ 1 KΩ CVDCPL<2:0> (ADCCON2<28:26>) = 001
			16				CVDCPL<2:0> (ADCCON2<28:26>) = 010
			18				CVDCPL<2:0> (ADCCON2<28:26>) = 011
			21				CVDCPL<2:0> (ADCCON2<28:26>) = 100
			23				CVDCPL<2:0> (ADCCON2<28:26>) = 101
			26				CVDCPL<2:0> (ADCCON2<28:26>) = 110
			28				CVDCPL<2:0> (ADCCON2<28:26>) = 111
			41	—	—	TAD	Source Impedance ≤ 5 KΩ CVDCPL<2:0> (ADCCON2<28:26>) = 001
			48				CVDCPL<2:0> (ADCCON2<28:26>) = 010
			56				CVDCPL<2:0> (ADCCON2<28:26>) = 011
			63				CVDCPL<2:0> (ADCCON2<28:26>) = 100
			70				CVDCPL<2:0> (ADCCON2<28:26>) = 101
			78				CVDCPL<2:0> (ADCCON2<28:26>) = 110
			85				CVDCPL<2:0> (ADCCON2<28:26>) = 111

Note 1: These parameters are characterized, but not tested in manufacturing.

2: The ADC module is functional at VBORMIN < VDD < VDDMIN, but with degraded performance. Unless otherwise stated, module functionality is guaranteed, but not characterized.