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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

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Details

Product Status	Active
Core Processor	MIPS32® M-Class
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	EBI/EMI, Ethernet, I ² C, PMP, SPI, SQI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	120
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	2.1V ~ 3.6V
Data Converters	A/D 48x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mz2048efg144-e-pl

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

Device Pin Tables

TABLE 2: PIN NAMES FOR 64-PIN DEVICES

64-PIN QFN ⁽⁴⁾ AND TQFP (TOP VIEW)			
PIC32MZ0512EF(E/F/K)064 PIC32MZ1024EF(G/H/M)064 PIC32MZ1024EF(E/F/K)064 PIC32MZ2048EF(G/H/M)064			
		64	1
		QFN ⁽⁴⁾	TQFP
Pin #	Full Pin Name	Pin #	Full Pin Name
1	AN17/ETXEN/RPE5/PMD5/RE5	33	VBUS
2	AN16/ETXD0/PMD6/RE6	34	VUSB3V3
3	AN15/ETXD1/PMD7/RE7	35	VSS
4	AN14/C1IND/RPG6/SCK2/PMA5/RG6	36	D-
5	AN13/C1INC/RPG7/SDA4/PMA4/RG7	37	D+
6	AN12/C2IND/RPG8/SCL4/PMA3/RG8	38	RPF3/USBID/RF3
7	VSS	39	VDD
8	VDD	40	VSS
9	MCLR	41	RPF4/SDA5/PMA9/RF4
10	AN11/C2INC/RPG9/PMA2/RG9	42	RPF5/SCL5/PMA8/RF5
11	AN45/C1INA/RPB5/RB5	43	AERXD0/ETXD2/RPD9/SDA1/PMCS2/PMA15/RD9
12	AN4/C1INB/RB4	44	ECOL/RPD10/SCL1/SCK4/RD10
13	AN3/C2INA/RPB3/RB3	45	AERXCLK/AEREFCLK/ECRS/RPD11/PMCS1/PMA14/RD11
14	AN2/C2INB/RPB2/RB2	46	AERXD1/ETXD3/RPD0/RTCC/INT0/RD0
15	PGEC1/VREF-/CVREF-/AN1/RPB1/RB1	47	SOSCI/RPC13/RC13
16	PGED1/VREF+/CVREF+/AN0/RPB0/PMA6/RB0	48	SOSCO/RPC14/T1CK/RC14
17	PGEC2/AN46/RPB6/RB6	49	EMDIO/AEMDIO/RPD1/SCK1/RD1
18	PGED2/AN47/RPB7/RB7	50	ETXERR/AETXEN/RPD2/SDA3/RD2
19	AVDD	51	AERXERR/ETXCLK/RPD3/SCL3/RD3
20	AVSS	52	SQICS0/RPD4/PMWR/RD4
21	AN48/RPB8/PMA10/RB8	53	SQICS1/RPD5/PMRD/RD5
22	AN49/RPB9/PMA7/RB9	54	VDD
23	TMS/CVREFOUT/AN5/RPB10/PMA13/RB10	55	VSS
24	TDO/AN6/PMA12/RB11	56	ERXD3/AETXD1/RPF0/RF0
25	VSS	57	TRCLK/SQICLK/ERXD2/AETXD0/RPF1/RF1
26	VDD	58	TRD0/SQID0/ERXD1/PMD0/RE0
27	TCK/AN7/PMA11/RB12	59	VSS
28	TDI/AN8/RB13	60	VDD
29	AN9/RPB14/SCK3/PMA1/RB14	61	TRD1/SQID1/ERXD0/PMD1/RE1
30	AN10/EMDC/AEMDC/RPB15/OCFB/PMA0/RB15	62	TRD2/SQID2/ERXDV/ECRS/SDV/AECRS/SDV/PMD2/RE2
31	OSC1/CLK1/RC12	63	TRD3/SQID3/ERXCLK/EREFCLK/RPE3/PMD3/RE3
32	OSC2/CLK0/RC15	64	AN18/ERXERR/PMD4/RE4

- Note**
- 1: The RPN pins can be used by remappable peripherals. See Table 1 for the available peripherals and **Section 12.4 “Peripheral Pin Select (PPS)”** for restrictions.
 - 2: Every I/O port pin (RBx-RGx) can be used as a change notification pin (CNBx-CNGx). See **Section 12.0 “I/O Ports”** for more information.
 - 3: Shaded pins are 5V tolerant.
 - 4: The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to Vss externally.

124-PIN VTLA (BOTTOM VIEW)

Pin locations and part numbers shown in the bottom view:

- A17
- B13
- B29
- A34
- B1
- B56
- B41
- A51
- A1
- A68
- Polarity Indicator

Part numbers listed on the left:

- PIC32MZ0512EF(E/F/K)124
- PIC32MZ1024EF(G/H/M)124
- PIC32MZ1024EF(E/F/K)124
- PIC32MZ2048EF(G/H/M)124

Note	1: The RPN pins can be used by remappable peripherals. See Table 1 for the available peripherals and Section 12.4 “Peripheral Pin Select (PPS)” for restrictions. 2: Every I/O port pin (RAX-RJx) can be used as a change notification pin (CNAX-CNJx). See Section 12.0 “I/O Ports” for more information. 3: Shaded pins are 5V tolerant. 4: The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to Vss externally.
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Referenced Sources

This device data sheet is based on the following individual sections of the “PIC32 Family Reference Manual”. These documents should be considered as the general reference for the operation of a particular module or device feature.

Note: To access the following documents, browse the documentation section of the Microchip web site (www.microchip.com).

- **Section 1. “Introduction”** (DS60001127)
- **Section 7. “Resets”** (DS60001118)
- **Section 8. “Interrupt Controller”** (DS60001108)
- **Section 9. “Watchdog, Deadman, and Power-up Timers”** (DS60001114)
- **Section 10. “Power-Saving Features”** (DS60001130)
- **Section 12. “I/O Ports”** (DS60001120)
- **Section 13. “Parallel Master Port (PMP)”** (DS60001128)
- **Section 14. “Timers”** (DS60001105)
- **Section 15. “Input Capture”** (DS60001122)
- **Section 16. “Output Compare”** (DS60001111)
- **Section 19. “Comparator”** (DS60001110)
- **Section 20. “Comparator Voltage Reference (CVREF)”** (DS60001109)
- **Section 21. “Universal Asynchronous Receiver Transmitter (UART)”** (DS60001107)
- **Section 22. “12-bit High-Speed Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC)”** (DS60001344)
- **Section 23. “Serial Peripheral Interface (SPI)”** (DS60001106)
- **Section 24. “Inter-Integrated Circuit (I²C)”** (DS60001116)
- **Section 29. “Real-Time Clock and Calendar (RTCC)”** (DS60001125)
- **Section 31. “Direct Memory Access (DMA) Controller”** (DS60001117)
- **Section 32. “Configuration”** (DS60001124)
- **Section 33. “Programming and Diagnostics”** (DS60001129)
- **Section 34. “Controller Area Network (CAN)”** (DS60001154)
- **Section 35. “Ethernet Controller”** (DS60001155)
- **Section 41. “Prefetch Module for Devices with L1 CPU Cache”** (DS60001183)
- **Section 42. “Oscillators with Enhanced PLL”** (DS60001250)
- **Section 46. “Serial Quad Interface (SQI)”** (DS60001244)
- **Section 47. “External Bus Interface (EBI)”** (DS60001245)
- **Section 48. “Memory Organization and Permissions”** (DS60001214)
- **Section 49. “Crypto Engine (CE) and Random Number Generator (RNG)”** (DS60001246)
- **Section 50. “CPU for Devices with MIPS32[®] microAptiv[™] and M-Class Cores”** (DS60001192)
- **Section 51. “Hi-Speed USB with On-The-Go (OTG)”** (DS60001326)
- **Section 52. “Flash Program Memory with Support for Live Update”** (DS60001193)

REGISTER 4-3: SBTxELOG1: SYSTEM BUS TARGET 'x' ERROR LOG REGISTER 1 ('x' = 0-13) (CONTINUED)

- bit 7-4 **REGION<3:0>**: Requested Region Number bits
 1111 - 0000 = Target's region that reported a permission group violation
- bit 3 **Unimplemented**: Read as '0'
- bit 2-0 **CMD<2:0>**: Transaction Command of the Requester bits
 111 = Reserved
 110 = Reserved
 101 = Write (a non-posted write)
 100 = Reserved
 011 = Read (a locked read caused by a Read-Modify-Write transaction)
 010 = Read
 001 = Write
 000 = Idle

Note: Refer to Table 4-6 for the list of available targets and their descriptions.

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

REGISTER 5-7: NVMPWP: PROGRAM FLASH WRITE-PROTECT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-1	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	PWPULOCK	—	—	—	—	—	—	—
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PWP<23:16>							
15:8	R/W-0	R/W-0	R-0	R-0	R-0	R-0	R-0	R-0
	PWP<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	PWP<7:0>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31 **PWPULOCK:** Program Flash Memory Page Write-protect Unlock bit

1 = Register is not locked and can be modified

0 = Register is locked and cannot be modified

This bit is only clearable and cannot be set except by any reset.

bit 30-24 **Unimplemented:** Read as '0'

bit 23-0 **PWP<23:0>:** Flash Program Write-protect (Page) Address bits

Physical memory below address 0x1Dxxxxxx is write protected, where 'xxxxxx' is specified by PWP<23:0>.

When PWP<23:0> has a value of '0', write protection is disabled for the entire program Flash. If the specified address falls within the page, the entire page and all pages below the current page will be protected.

Note: The bits in this register are only writable when the NVMKEY unlock sequence is followed.

6.0 RESETS

Note: This data sheet summarizes the features of the PIC32MZ EF family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 7. “Resets”** (DS60001118) in the *“PIC32 Family Reference Manual”*, which is available from the Microchip web site (www.microchip.com/PIC32).

The Reset module combines all Reset sources and controls the device Master Reset signal, SYSRST. The device Reset sources are as follows:

- Power-on Reset (POR)
- Master Clear Reset pin ($\overline{\text{MCLR}}$)
- Software Reset (SWR)
- Watchdog Timer Reset (WDTR)
- Brown-out Reset (BOR)
- Configuration Mismatch Reset (CMR)
- Deadman Timer Reset (DMTR)

A simplified block diagram of the Reset module is illustrated in Figure 6-1.

FIGURE 6-1: SYSTEM RESET BLOCK DIAGRAM

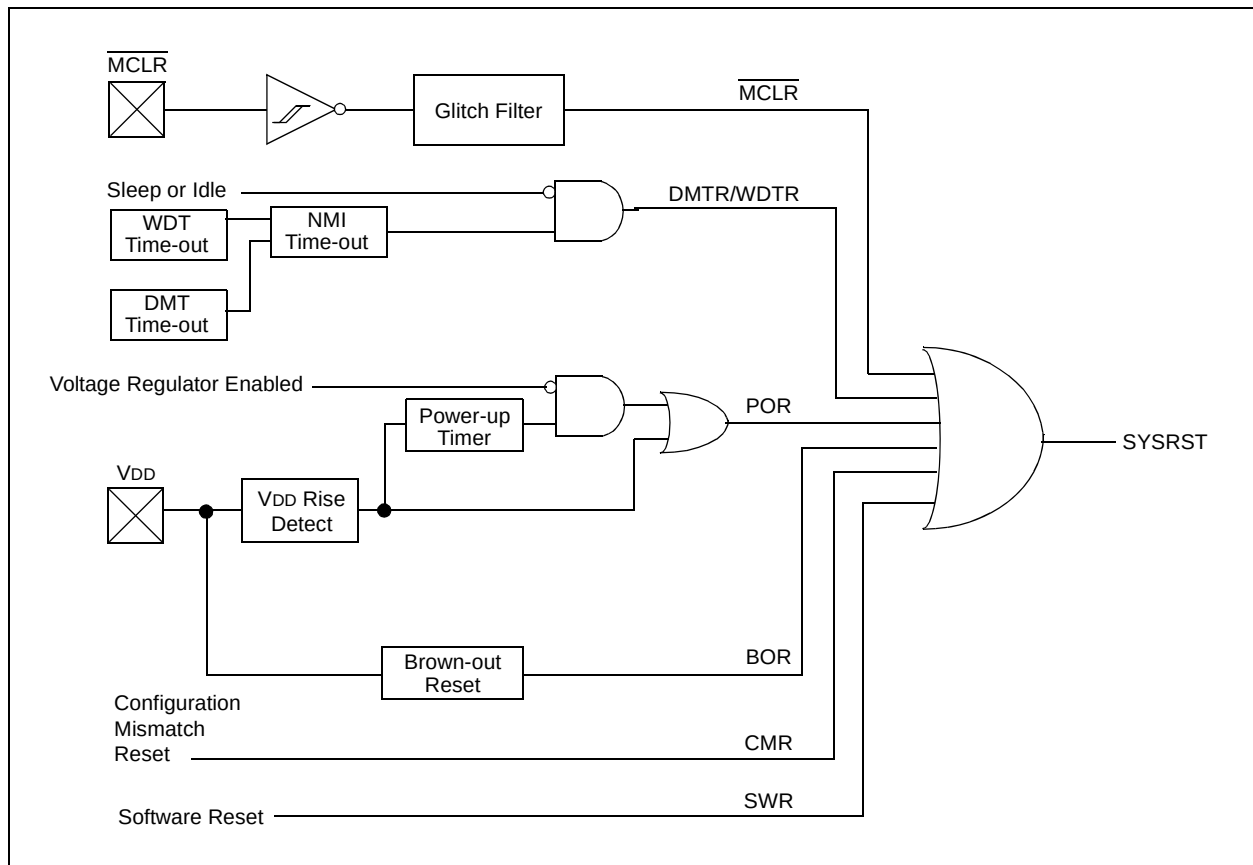


TABLE 7-1: MIPS32® M-CLASS MICROPROCESSOR CORE EXCEPTION TYPES (CONTINUED)

Exception Type (In Order of Priority)	Description	Branches to	Status Bits Set	Debug Bits Set	EXCCODE	XC32 Function Name
Instruction Validity Exceptions	An instruction could not be completed because it was not allowed to access the required resources (Coprocessor Unusable) or was illegal (Reserved Instruction). If both exceptions occur on the same instruction, the Coprocessor Unusable Exception takes priority over the Reserved Instruction Exception.	EBASE+0x180	EXL	—	0x0A or 0x0B	_general_exception_handler
Execute Exception	An instruction-based exception occurred: Integer overflow, trap, system call, breakpoint, floating point, or DSP ASE state disabled exception.	EBASE+0x180	EXL	—	0x08-0x0C	_general_exception_handler
Tr	Execution of a trap (when trap condition is true).	EBASE+0x180	EXL	—	0x0D	_general_exception_handler
DDBL/DDBS	EJTAG Data Address Break (address only) or EJTAG data value break on store (address + value).	0xBFC0_0480	—	DDBL or DDBS	—	—
WATCH	A reference to an address that is in one of the Watch registers (data).	EBASE+0x180	EXL	—	0x17	_general_exception_handler
AdEL	Load address alignment error. User mode load reference to kernel address.	EBASE+0x180	EXL	—	0x04	_general_exception_handler
AdES	Store address alignment error. User mode store to kernel address.	EBASE+0x180	EXL	—	0x05	_general_exception_handler
TLBL	Load TLB miss or load TLB hit to page with V = 0.	EBASE+0x180	EXL	—	0x02	_general_exception_handler
TLBS	Store TLB miss or store TLB hit to page with V = 0.	EBASE+0x180	EXL	—	0x03	_general_exception_handler
DBE	Load or store bus error.	EBASE+0x180	EXL	—	0x07	_general_exception_handler
DDBL	EJTAG data hardware breakpoint matched in load data compare.	0xBFC0_0480	—	DDBL	—	—
CBrk	EJTAG complex breakpoint.	0xBFC0_0480	—	DIBIMPR, DDBLIMPR, and/or DDBSIMPR	—	—
Lowest Priority						

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REGISTER 10-16: DCHxCSIZ: DMA CHANNEL x CELL-SIZE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHCSIZ<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHCSIZ<7:0>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **CHCSIZ<15:0>**: Channel Cell-Size bits

1111111111111111 = 65,535 bytes transferred on an event

.

.

0000000000000010 = 2 bytes transferred on an event

0000000000000001 = 1 byte transferred on an event

0000000000000000 = 65,536 bytes transferred on an event

REGISTER 10-17: DCHxCPTR: DMA CHANNEL x CELL POINTER REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	CHCPTR<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	CHCPTR<7:0>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **CHCPTR<15:0>**: Channel Cell Progress Pointer bits

1111111111111111 = 65,535 bytes have been transferred since the last event

.

.

0000000000000001 = 1 byte has been transferred since the last event

0000000000000000 = 0 bytes have been transferred since the last event

Note: When in Pattern Detect mode, this register is reset on a pattern detect.

11.1 USB OTG Control Registers

TABLE 11-1: USB REGISTER MAP 1

Virtual Address (BF8E_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
3000	USBCSR0	31:16	—	—	—	—	—	—	—	—	EP7TXIF	EP6TXIF	EP5TXIF	EP4TXIF	EP3TXIF	EP2TXIF	EP1TXIF	EP0IF	0000
		15:0	ISOUPD ⁽¹⁾	SOFT CONN ⁽¹⁾	HSEN	HSMODE	RESET	RESUME	SUSP MODE	SUSPEN	—	FUNC<6:0> ⁽¹⁾							2000
		— ⁽²⁾	— ⁽²⁾	— ⁽²⁾								— ⁽²⁾	— ⁽²⁾	— ⁽²⁾	— ⁽²⁾	— ⁽²⁾			
3004	USBCSR1	31:16	—	—	—	—	—	—	—	—	EP7TXIE	EP6TXIE	EP5TXIE	EP4TXIE	EP3TXIE	EP2TXIE	EP1TXIE	EP0IE	00FF
		15:0	—	—	—	—	—	—	—	—	EP7RXIF	EP6RXIF	EP5RXIF	EP4RXIF	EP3RXIF	EP2RXIF	EP1RXIF	—	0000
3008	USBCSR2	31:16	VBUSERRIE	SESSRQIE	DISCONIE	CONNIE	SOFIE	RESETIE	RESUMEIE	SUSPIE	VBUSERRIF	SESSREQIF	DISCONIF	CONNIF	SOFIF	RESETIF	RESUMEIF	SUSPIF	0000
		15:0	—	—	—	—	—	—	—	—	EP7RXIE	EP6RXIE	EP5RXIE	EP4RXIE	EP3RXIE	EP2RXIE	EP1RXIE	—	00FE
300C	USBCSR3	31:16	FORCEHST	FIFOACC	FORCEFS	FORCEHS	PACKET	TESTK	TESTJ	NAK	—	—	—	—	ENDPOINT<3:0>				0000
		15:0	—	—	—	—	—	RFRMNUM<10:0>											
3010	USB IE0CSR0 ⁽³⁾	31:16	—	—	—	—	— ⁽¹⁾	— ⁽¹⁾	— ⁽¹⁾	FLSHFIFO	SVC SETEND ⁽¹⁾	SVCPRP ⁽¹⁾	SEND STALL ⁽¹⁾	SETUP END ⁽¹⁾	DATAEND ⁽¹⁾	SENT STALL ⁽¹⁾	TXPKT RDY	RXPKT RDY	0000
		DISPING ⁽²⁾					DTWREN ⁽²⁾	DATA TGGL ⁽²⁾	NAK TMOUT ⁽²⁾		STATPKT ⁽²⁾	REQPKT ⁽²⁾	ERROR ⁽²⁾	SETUP PKT ⁽²⁾	RXSTALL ⁽²⁾	0000			
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
3018	USB IE0CSR2 ⁽³⁾	31:16	—	—	—	NAKLIM<4:0> ⁽²⁾				SPEED<1:0> ⁽²⁾		—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	RXCNT<6:0>							
301C	USB IE0CSR3 ⁽³⁾	31:16	MPRXEN	MPTXEN	BIGEND	HBRXEN	HBTXEN	DYNFIFOS	SOFTCONE	UTMIDWID	—	—	—	—	—	—	—	—	xx00
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
3010	USB IENCSR0 ⁽⁴⁾	31:16	AUTOSSET	ISO ⁽¹⁾	MODE	DMA REQEN	FRC DATTG	DMA REQMD	— ⁽¹⁾	— ⁽¹⁾	INCOMP TX ⁽¹⁾	CLRDT	SENT STALL ⁽¹⁾	SEND STALL ⁽¹⁾	FLUSH	UNDER RUN ⁽¹⁾	FIFONE	TXPKT RDY	0000
		—		DTWREN ⁽²⁾					DATA TGGL ⁽²⁾	NAK TMOUT ⁽²⁾	RXSTALL ⁽²⁾		SETUPPKT ⁽²⁾	ERROR ⁽²⁾		0000			
		15:0	MULT<4:0>						TXMAXP<10:0>										
3014	USB IENCSR1 ⁽⁴⁾	31:16	AUTOCLR	ISO ⁽¹⁾	DMA REQEN	DISNYET ⁽¹⁾	DMA REQMD	— ⁽¹⁾	— ⁽¹⁾	INCOM PRX	CLRDT	SENTSTALL ⁽¹⁾	SENDSTALL ⁽¹⁾	FLUSH	DATAERR ⁽¹⁾	OVERRUN ⁽¹⁾	FIFOFULL	RXPKT RDY	0000
		AUTORQ ⁽²⁾		PIDERR ⁽²⁾		DATA TWEN ⁽²⁾		DATA TGGL ⁽²⁾	RXSTALL ⁽²⁾			REQPKT ⁽²⁾	DERR- NAKT ⁽¹⁾		ERROR ⁽²⁾	0000			
		15:0	MULT<4:0>						RXMAXP<10:0>										
3018	USB IENCSR2 ⁽⁴⁾	31:16	TXINTERV<7:0> ⁽²⁾								SPEED<1:0> ⁽²⁾		PROTOCOL<1:0>		TEP<3:0>				0000
		15:0	—	—	RXCNT<13:0>												0000		
301C	USB IENCSR3 ^(1,3)	31:16	RXFIFOSZ<3:0>				TXFIFOSZ<3:0>				—	—	—	—	—	—	—	—	0000
		15:0	RXINTERV<7:0>								SPEED<1:0>		PROTOCOL<1:0>		TEP<3:0>				0000
3020	USB FIFO0	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
3024	USB FIFO1	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

- Note**
- 1: Device mode.
 - 2: Host mode.
 - 3: Definition for Endpoint 0 (ENDPOINT<3:0> (USBCSR<19:16>) = 0).
 - 4: Definition for Endpoints 1-7 (ENDPOINT<3:0> (USBCSR<19:16>) = 1 through 7).

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

REGISTER 11-10: USBIENCSR2: USB INDEXED ENDPOINT CONTROL STATUS REGISTER 2 (ENDPOINT 1-7)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	TXINTERV<7:0>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SPEED<1:0>		PROTOCOL<1:0>		TEP<3:0>			
15:8	U-0	U-0	R-0	R-0	R-0	R-0	R-0	R-0
	—	—	RXCNT<13:8>					
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	RXCNT<7:0>							

Legend:

HC = Hardware Cleared	HS = Hardware Set
R = Readable bit	W = Writable bit
U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set
	'0' = Bit is cleared
	x = Bit is unknown

bit 31-24 **TXINTERV<7:0>**: Endpoint TX Polling Interval/NAK Limit bits (*Host mode*)

For Interrupt and Isochronous transfers, this field defines the polling interval for the endpoint. For Bulk endpoints, this field sets the number of frames/microframes after which the endpoint should time out on receiving a stream of NAK responses.

The following table describes the valid values and interpretation for these bits:

Transfer Type	Speed	Valid Values (m)	Interpretation
Interrupt	Low/Full	0x01 to 0xFF	Polling interval is 'm' frames.
	High	0x01 to 0x10	Polling interval is $2^{(m-1)}$ frames.
Isochronous	Full or High	0x01 to 0x10	Polling interval is $2^{(m-1)}$ frames/microframes.
Bulk	Full or High	0x02 to 0x10	NAK limit is $2^{(m-1)}$ frames/microframes. A value of '0' or '1' disables the NAK time-out function.

bit 23-22 **SPEED<1:0>**: TX Endpoint Operating Speed Control bits (*Host mode*)

11 = Low-Speed
10 = Full-Speed
01 = Hi-Speed
00 = Reserved

bit 21-20 **PROTOCOL<1:0>**: TX Endpoint Protocol Control bits

11 = Interrupt
10 = Bulk
01 = Isochronous
00 = Control

bit 19-16 **TEP<3:0>**: TX Target Endpoint Number bits

This value is the endpoint number contained in the TX endpoint descriptor returned to the USB module during device enumeration.

bit 15-14 **Unimplemented**: Read as '0'

bit 13-0 **RXCNT<13:0>**: Receive Count bits

The number of received data bytes in the endpoint RX FIFO. The value returned changes as the contents of the FIFO change and is only valid while RXPkTRDY is set.

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REGISTER 11-12: USBFIFOx: USB FIFO DATA REGISTER 'x' ('x' = 0-7)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DATA<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DATA<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DATA<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DATA<7:0>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-0 **DATA<31:0>**: USB Transmit/Receive FIFO Data bits

Writes to this register loads data into the TxFIFO for the corresponding endpoint. Reading from this register unloads data from the RxFIFO for the corresponding endpoint.

Transfers may be 8-bit, 16-bit or 32-bit as required, and any combination of access is allowed provided the data accessed is contiguous. However, all transfers associated with one packet must be of the same width so that data is consistently byte-, word- or double-word aligned. The last transfer may contain fewer bytes than the previous transfers in order to complete an odd-byte or odd-word transfer.

REGISTER 19-1: SPIxCON: SPI CONTROL REGISTER (CONTINUED)

- bit 17 **SPIFE:** Frame Sync Pulse Edge Select bit (Framed SPI mode only)
 1 = Frame synchronization pulse coincides with the first bit clock
 0 = Frame synchronization pulse precedes the first bit clock
- bit 16 **ENHBUF:** Enhanced Buffer Enable bit⁽¹⁾
 1 = Enhanced Buffer mode is enabled
 0 = Enhanced Buffer mode is disabled
- bit 15 **ON:** SPI/I²S Module On bit
 1 = SPI/I²S module is enabled
 0 = SPI/I²S module is disabled
- bit 14 **Unimplemented:** Read as '0'
- bit 13 **SIDL:** Stop in Idle Mode bit
 1 = Discontinue operation when CPU enters in Idle mode
 0 = Continue operation in Idle mode
- bit 12 **DISSDO:** Disable SDOx pin bit⁽⁴⁾
 1 = SDOx pin is not used by the module. Pin is controlled by associated PORT register
 0 = SDOx pin is controlled by the module
- bit 11-10 **MODE<32,16>:** 32/16-Bit Communication Select bits
 When AUDEN = 1:
- | MODE32 | MODE16 | Communication |
|--------|--------|---|
| 1 | 1 | 24-bit Data, 32-bit FIFO, 32-bit Channel/64-bit Frame |
| 1 | 0 | 32-bit Data, 32-bit FIFO, 32-bit Channel/64-bit Frame |
| 0 | 1 | 16-bit Data, 16-bit FIFO, 32-bit Channel/64-bit Frame |
| 0 | 0 | 16-bit Data, 16-bit FIFO, 16-bit Channel/32-bit Frame |
- When AUDEN = 0:
- | MODE32 | MODE16 | Communication |
|--------|--------|---------------|
| 1 | x | 32-bit |
| 0 | 1 | 16-bit |
| 0 | 0 | 8-bit |
- bit 9 **SMP:** SPI Data Input Sample Phase bit
 Master mode (MSTEN = 1):
 1 = Input data sampled at end of data output time
 0 = Input data sampled at middle of data output time
 Slave mode (MSTEN = 0):
 SMP value is ignored when SPI is used in Slave mode. The module always uses SMP = 0.
- bit 8 **CKE:** SPI Clock Edge Select bit⁽²⁾
 1 = Serial output data changes on transition from active clock state to Idle clock state (see CKP bit)
 0 = Serial output data changes on transition from Idle clock state to active clock state (see CKP bit)
- bit 7 **SSEN:** Slave Select Enable (Slave mode) bit
 1 = $\overline{SSx}$ pin is used for Slave mode
 0 = $\overline{SSx}$ pin is not used for Slave mode, pin is controlled by the port function.
- bit 6 **CKP:** Clock Polarity Select bit⁽³⁾
 1 = Idle state for clock is a high level; active state is a low level
 0 = Idle state for clock is a low level; active state is a high level

- Note 1:** This bit can only be written when the ON bit = 0. Refer to **Section 37.0 “Electrical Characteristics”** for maximum clock frequency requirements.
- 2:** This bit is not used in the Framed SPI mode. The user should program this bit to '0' for the Framed SPI mode (FRMEN = 1).
- 3:** When AUDEN = 1, the SPI/I²S module functions as if the CKP bit is equal to '1', regardless of the actual value of the CKP bit.
- 4:** This bit present for legacy compatibility and is superseded by PPS functionality on these devices (see **Section 12.4 “Peripheral Pin Select (PPS)”** for more information).

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REGISTER 28-4: ADCTRGMODE: ADC TRIGGERING MODE FOR DEDICATED ADC REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
	—	—	—	—	—	—	SH4ALT<1:0>	
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SH3ALT<1:0>		SH2ALT<1:0>		SH1ALT<1:0>		SH0ALT<1:0>	
15:8	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	STRGEN4	STRGEN3	STRGEN2	STRGEN1	STRGEN0
7:0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	SSAMPEN4	SSAMPEN3	SSAMPEN2	SSAMPEN1	SSAMPEN0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-26 **Unimplemented:** Read as '0'

bit 25-24 **SH4ALT<1:0>**: ADC4 Analog Input Select bit

11 = Reserved
 10 = Reserved
 01 = AN49
 00 = AN4

bit 23-22 **SH3ALT<1:0>**: ADC3 Analog Input Select bit

11 = Reserved
 10 = Reserved
 01 = AN48
 00 = AN3

bit 21-20 **SH2ALT<1:0>**: ADC2 Analog Input Select bit

11 = Reserved
 10 = Reserved
 01 = AN47
 00 = AN2

bit 19-18 **SH1ALT<1:0>**: ADC1 Analog Input Select bit

11 = Reserved
 10 = Reserved
 01 = AN46
 00 = AN1

bit 17-16 **SH0ALT<1:0>**: ADC0 Analog Input Select bit

11 = Reserved
 10 = Reserved
 01 = AN45
 00 = AN0

bit 15-13 **Unimplemented:** Read as '0'

bit 12 **STRGEN4**: ADC4 Presynchronized Triggers bit

1 = ADC4 uses presynchronized triggers
 0 = ADC4 does not use presynchronized triggers

bit 11 **STRGEN3**: ADC3 Presynchronized Triggers bit

1 = ADC3 uses presynchronized triggers
 0 = ADC3 does not use presynchronized triggers

bit 10 **STRGEN2**: ADC2 Presynchronized Triggers bit

1 = ADC2 uses presynchronized triggers
 0 = ADC2 does not use presynchronized triggers

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

REGISTER 29-11: CiFLTCON1: CAN FILTER CONTROL REGISTER 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN7	MSEL7<1:0>		FSEL7<4:0>				
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN6	MSEL6<1:0>		FSEL6<4:0>				
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN5	MSEL5<1:0>		FSEL5<4:0>				
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN4	MSEL4<1:0>		FSEL4<4:0>				

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31 **FLTEN7**: Filter 7 Enable bit

1 = Filter is enabled

0 = Filter is disabled

bit 30-29 **MSEL7<1:0>**: Filter 7 Mask Select bits

11 = Acceptance Mask 3 selected

10 = Acceptance Mask 2 selected

01 = Acceptance Mask 1 selected

00 = Acceptance Mask 0 selected

bit 28-24 **FSEL7<4:0>**: FIFO Selection bits

11111 = Message matching filter is stored in FIFO buffer 31

11110 = Message matching filter is stored in FIFO buffer 30

•

•

•

00001 = Message matching filter is stored in FIFO buffer 1

00000 = Message matching filter is stored in FIFO buffer 0

bit 23 **FLTEN6**: Filter 6 Enable bit

1 = Filter is enabled

0 = Filter is disabled

bit 22-21 **MSEL6<1:0>**: Filter 6 Mask Select bits

11 = Acceptance Mask 3 selected

10 = Acceptance Mask 2 selected

01 = Acceptance Mask 1 selected

00 = Acceptance Mask 0 selected

bit 20-16 **FSEL6<4:0>**: FIFO Selection bits

11111 = Message matching filter is stored in FIFO buffer 31

11110 = Message matching filter is stored in FIFO buffer 30

•

•

•

00001 = Message matching filter is stored in FIFO buffer 1

00000 = Message matching filter is stored in FIFO buffer 0

Note: The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

REGISTER 29-15: CFLTCON5: CAN FILTER CONTROL REGISTER 5 (CONTINUED)

- bit 15 **FLTEN21**: Filter 21 Enable bit
 1 = Filter is enabled
 0 = Filter is disabled
- bit 14-13 **MSEL21<1:0>**: Filter 21 Mask Select bits
 11 = Acceptance Mask 3 selected
 10 = Acceptance Mask 2 selected
 01 = Acceptance Mask 1 selected
 00 = Acceptance Mask 0 selected
- bit 12-8 **FSEL21<4:0>**: FIFO Selection bits
 11111 = Message matching filter is stored in FIFO buffer 31
 11110 = Message matching filter is stored in FIFO buffer 30
 •
 •
 •
 00001 = Message matching filter is stored in FIFO buffer 1
 00000 = Message matching filter is stored in FIFO buffer 0
- bit 7 **FLTEN20**: Filter 20 Enable bit
 1 = Filter is enabled
 0 = Filter is disabled
- bit 6-5 **MSEL20<1:0>**: Filter 20 Mask Select bits
 11 = Acceptance Mask 3 selected
 10 = Acceptance Mask 2 selected
 01 = Acceptance Mask 1 selected
 00 = Acceptance Mask 0 selected
- bit 4-0 **FSEL20<4:0>**: FIFO Selection bits
 11111 = Message matching filter is stored in FIFO buffer 31
 11110 = Message matching filter is stored in FIFO buffer 30
 •
 •
 •
 00001 = Message matching filter is stored in FIFO buffer 1
 00000 = Message matching filter is stored in FIFO buffer 0

Note: The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

REGISTER 29-22: CiFIFOUn: CAN FIFO USER ADDRESS REGISTER 'n' ('n' = 0-31)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
	CiFIFOUn<31:24>							
23:16	R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
	CiFIFOUn<23:16>							
15:8	R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
	CiFIFOUn<15:8>							
7:0	R-x	R-x	R-x	R-x	R-x	R-x	R-0 ⁽¹⁾	R-0 ⁽¹⁾
	CiFIFOUn<7:0>							

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-0 **CiFIFOUn<31:0>**: CAN FIFO User Address bits

TXEN = 1: (FIFO configured as a Transmit Buffer)

A read of this register will return the address where the next message is to be written (FIFO head).

TXEN = 0: (FIFO configured as a Receive Buffer)

A read of this register will return the address where the next message is to be read (FIFO tail).

Note 1: This bit will always read '0', which forces byte-alignment of messages.

Note: This register is not guaranteed to read correctly in Configuration mode, and should only be accessed when the module is not in Configuration mode.

REGISTER 29-23: CiFIFOIn: CAN MODULE MESSAGE INDEX REGISTER 'n' ('n' = 0-31)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	R-0	R-0	R-0	R-0	R-0
	—	—	—	CiFIFOIn<4:0>				

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-5 **Unimplemented:** Read as '0'

bit 4-0 **CiFIFOIn<4:0>**: CAN Side FIFO Message Index bits

TXEN = 1: (FIFO configured as a Transmit Buffer)

A read of this register will return an index to the message that the FIFO will next attempt to transmit.

TXEN = 0: (FIFO configured as a Receive Buffer)

A read of this register will return an index to the message that the FIFO will use to save the next message.

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

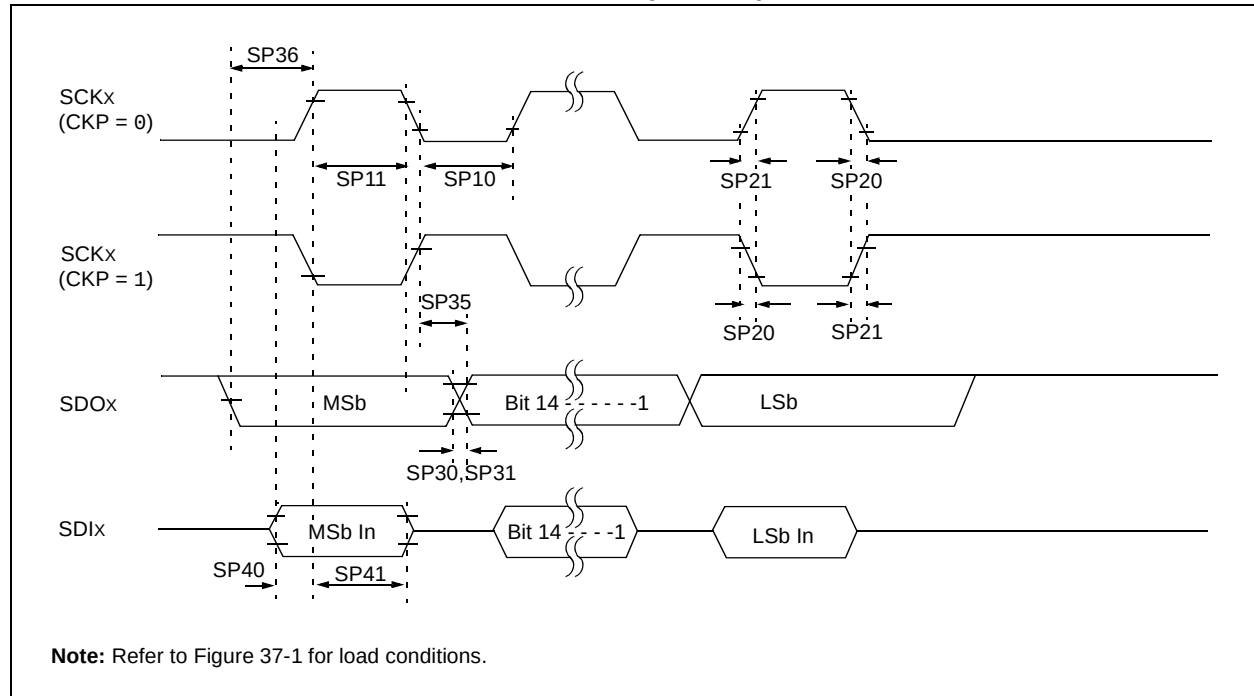
TABLE 33-1: PERIPHERAL MODULE DISABLE BITS AND LOCATIONS⁽¹⁾ (CONTINUED)

Peripheral	PMDx bit Name	Register Name and Bit Location
UART3	U3MD	PMD5<2>
UART4	U4MD	PMD5<3>
UART5	U5MD	PMD5<4>
UART6	U6MD	PMD5<5>
SPI1	SPI1MD	PMD5<8>
SPI2	SPI2MD	PMD5<9>
SPI3	SPI3MD	PMD5<10>
SPI4	SPI4MD	PMD5<11>
SPI5	SPI5MD	PMD5<12>
SPI6	SPI6MD	PMD5<13>
I2C1	I2C1MD	PMD5<16>
I2C2	I2C2MD	PMD5<17>
I2C3	I2C3MD	PMD5<18>
I2C4	I2C4MD	PMD5<19>
I2C5	I2C5MD	PMD5<20>
USB ⁽²⁾	USBMD	PMD5<24>
CAN1	CAN1MD	PMD5<28>
CAN2	CAN2MD	PMD5<29>
RTCC	RTCCMD	PMD6<0>
Reference Clock Output 1	REFO1MD	PMD6<8>
Reference Clock Output 2	REFO2MD	PMD6<9>
Reference Clock Output 3	REFO3MD	PMD6<10>
Reference Clock Output 4	REFO4MD	PMD6<11>
PMP	PMPMD	PMD6<16>
EBI	EBIMD	PMD6<17>
SQI1	SQI1MD	PMD6<23>
Ethernet	ETHMD	PMD6<28>
DMA	DMAMD	PMD7<4>
Random Number Generator	RNGMD	PMD7<20>
Crypto	CRYPTMD	PMD7<22>

Note 1: Not all modules and associated PMDx bits are available on all devices. See **TABLE 1: “PIC32MZ EF Family Features”** for the lists of available peripherals.

2: Module must not be busy after clearing the associated ON bit and prior to setting the USBMD bit.

FIGURE 37-11: SPIx MODULE MASTER MODE (CKE = 1) TIMING CHARACTERISTICS



39.2 AC Characteristics and Timing Parameters

The information contained in this section defines PIC32MZ EF device AC characteristics and timing parameters.

TABLE 39-5: SYSTEM TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param. No.	Symbol	Characteristics	Minimum	Typical	Maximum	Units	Conditions
MOS51	FSys	System Frequency	DC	—	252	MHz	USB module disabled
			60	—	252	MHz	USB module enabled
MOS55a	FPB	Peripheral Bus Frequency	DC	—	100	MHz	For PBCLKx, 'x' ≠ 4, 7 (see Note 1)
MOS55b			DC	—	200	MHz	For PBCLK4
MOS55c			DC	—	252	MHz	For PBCLK7
MOS56	FREF	Reference Clock Frequency	—	—	50	MHz	For REFCLKI1, 3, 4 and REFCLKO1, 3, 4 pins

Note 1: If the DEVCFG registers are configured for a SYSCLK speed greater than 200 MHz, these PBCLKs will be running faster than the maximum rating when the device comes out of Reset. To ensure proper operation, firmware must start the device at a speed less than or equal to 200 MHz, adjust the speed of the PBCLKs, and then raise the SYSCLK speed to the desired speed.

TABLE 39-6: PLL CLOCK TIMING SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param. No.	Symbol	Characteristics ⁽¹⁾	Min.	Typical	Max.	Units	Conditions
MOS54a	FPLL	PLL Output Frequency Range	10	—	252	MHz	—

Note 1: These parameters are characterized, but not tested in manufacturing.

2: This jitter specification is based on clock-cycle by clock-cycle measurements. To get the effective jitter for individual time-bases on communication clocks, use the following formula:

$$EffectiveJitter = \frac{D_{CLK}}{\sqrt{\frac{PBCLK2}{CommunicationClock}}}$$

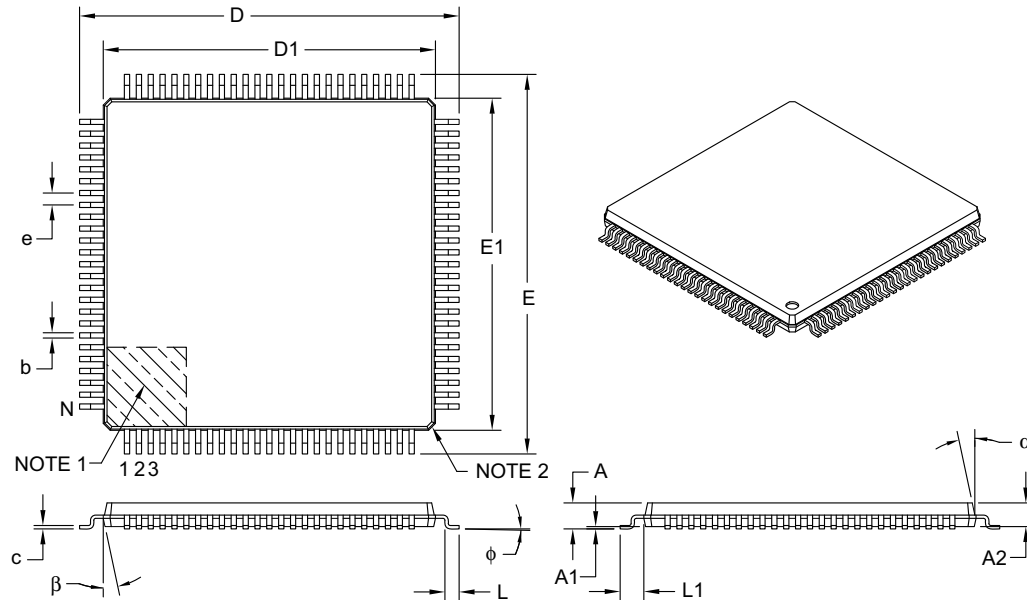
For example, if PBCLK2 = 100 MHz and SPI bit rate = 50 MHz, the effective jitter is as follows:

$$EffectiveJitter = \frac{D_{CLK}}{\sqrt{\frac{100}{50}}} = \frac{D_{CLK}}{1.41}$$

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100-Lead Plastic Thin Quad Flatpack (PF) – 14x14x1 mm Body, 2.00 mm [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



		Units	MILLIMETERS		
Dimension Limits			MIN	NOM	MAX
Number of Leads	N		100		
Lead Pitch	e		0.50 BSC		
Overall Height	A		–	–	1.20
Molded Package Thickness	A2		0.95	1.00	1.05
Standoff	A1		0.05	–	0.15
Foot Length	L		0.45	0.60	0.75
Footprint	L1		1.00 REF		
Foot Angle	φ		0°	3.5°	7°
Overall Width	E		16.00 BSC		
Overall Length	D		16.00 BSC		
Molded Package Width	E1		14.00 BSC		
Molded Package Length	D1		14.00 BSC		
Lead Thickness	c		0.09	–	0.20
Lead Width	b		0.17	0.22	0.27
Mold Draft Angle Top	α		11°	12°	13°
Mold Draft Angle Bottom	β		11°	12°	13°

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Chamfers at corners are optional; size may vary.
- Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-110B