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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	MIPS32® M-Class
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	EBI/EMI, Ethernet, I ² C, PMP, SPI, SQI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	120
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	2.1V ~ 3.6V
Data Converters	A/D 48x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-TQFP
Supplier Device Package	144-TQFP (16x16)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mz2048efg144-i-ph

3.0 CPU

Note 1: This data sheet summarizes the features of the PIC32MZ EF family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 50. "CPU for Devices with MIPS32® microAptiv™ and M-Class Cores"** (DS60001192) of the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

2: The Series 5 Warrior M-class CPU core resources are available at: www.imgtec.com.

The MIPS32® M-Class Core is the heart of the PIC32MZ EF family device processor. The CPU fetches instructions, decodes each instruction, fetches source operands, executes each instruction and writes the results of instruction execution to the proper destinations.

Key features include:

- 5-stage pipeline
- 32-bit address and data paths
- MIPS32 Enhanced Architecture (Release 5):
 - Multiply-accumulate and multiply-subtract instructions
 - Targeted multiply instruction
 - Zero/One detect instructions
 - WAIT instruction
 - Conditional move instructions (MOVN, MOVZ)
 - Vectored interrupts
 - Programmable exception vector base
 - Atomic interrupt enable/disable
 - GPR shadow registers to minimize latency for interrupt handlers
 - Bit field manipulation instructions
 - Virtual memory support
- microMIPS™ compatible instruction set:
 - Improves code size density over MIPS32, while maintaining MIPS32 performance.
 - Supports all MIPS32 instructions (except branch-likely instructions)
 - Fifteen additional 32-bit instructions and 39 16-bit instructions corresponding to commonly-used MIPS32 instructions
 - Stack pointer implicit in instruction
 - MIPS32 assembly and ABI compatible
- MMU with Translation Lookaside Buffer (TLB) mechanism:
 - 16 dual-entry fully associative Joint TLB
 - 4-entry fully associative Instruction and Data TLB
 - 4 KB pages
- Separate L1 data and instruction caches:
 - 16 KB 4-way Instruction Cache (I-Cache)
 - 4 KB 4-way Data Cache (D-Cache)
- Autonomous Multiply/Divide Unit (MDU):
 - Maximum issue rate of one 32x32 multiply per clock
 - Early-in iterative divide. Minimum 12 and maximum 38 clock latency (dividend (rs) sign extension-dependent)
- Power Control:
 - Minimum frequency: 0 MHz
 - Low-Power mode (triggered by WAIT instruction)
 - Extensive use of local gated clocks
- EJTAG Debug and Instruction Trace:
 - Support for single stepping
 - Virtual instruction and data address/value breakpoints
 - Hardware breakpoint supports both address match and address range triggering.
 - Eight instruction and four data complex breakpoints
- iFlowtrace® version 2.0 support:
 - Real-time instruction program counter
 - Special events trace capability
 - Two performance counters with 34 user-selectable countable events
 - Disabled if the processor enters Debug mode
 - Program Counter sampling
- Four Watch registers:
 - Instruction, Data Read, Data Write options
 - Address match masking options
- DSP ASE Extension:
 - Native fractional format data type operations
 - Register Single Instruction Multiple Data (SIMD) operations (add, subtract, multiply, shift)
 - GPR-based shift
 - Bit manipulation
 - Compare-Pick
 - DSP Control Access
 - Indexed-Load
 - Branch
 - Multiplication of complex operands
 - Variable bit insertion and extraction
 - Virtual circular buffers
 - Arithmetic saturation and overflow handling
 - Zero-cycle overhead saturation and rounding operations
- Floating Point Unit (FPU):
 - 1985 IEEE-754 compliant Floating Point Unit
 - Supports single and double precision datatypes
 - 2008 IEEE-754 compatibility control of NaN handling and Abs/Neg instructions
 - Runs at 1:1 core/FPU clock ratio

5.1 Flash Control Registers

TABLE 5-1: FLASH CONTROLLER REGISTER MAP

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets	
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0		
0600	NVMCON ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	WR	WREN	WRERR	LVDERR	—	—	—	—	PFSWAP	BFSWAP	—	—	NVMOP<3:0>				00x0	
0610	NVMKEY	31:16	NVMKEY<31:0>																0000	
		15:0																	0000	
0620	NVMADDR ⁽¹⁾	31:16	NVMADDR<31:0>																0000	
		15:0																	0000	
0630	NVMDATA0	31:16	NVMDATA0<31:0>																0000	
		15:0																	0000	
0640	NVMDATA1	31:16	NVMDATA1<31:0>																0000	
		15:0																	0000	
0650	NVMDATA2	31:16	NVMDATA2<31:0>																0000	
		15:0																	0000	
0660	NVMDATA3	31:16	NVMDATA3<31:0>																0000	
		15:0																	0000	
0670	NVMSRC ADDR	31:16	NVMSRCADDR<31:0>																0000	
		15:0																	0000	
0680	NVMPWP ⁽¹⁾	31:16	PWPLOCK	—	—	—	—	—	—	—	PWP<23:16>									8000
		15:0	PWP<15:0>																0000	
0690	NVMBWP ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	LBWPLOCK	—	—	LBWP4	LBWP3	LBWP2	LBWP1	LBWP0	UBWPLOCK	—	—	UBWP4	UBWP3	UBWP2	UBWP1	UBWP0	9FDF	
06A0	NVMCON2 ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	001F	
		15:0	—	—	—	—	—	—	—	—	SWAPLOCK<1:0>			—	—	—	—	—	0000	

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 “CLR, SET, and INV Registers”** for more information.

10.0 DIRECT MEMORY ACCESS (DMA) CONTROLLER

Note: This data sheet summarizes the features of the PIC32MZ EF family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 31. “Direct Memory Access (DMA) Controller”** (DS60001117) in the *“PIC32 Family Reference Manual”*, which is available from the Microchip web site (www.microchip.com/PIC32).

The Direct Memory Access (DMA) Controller is a bus master module useful for data transfers between different devices without CPU intervention. The source and destination of a DMA transfer can be any of the memory mapped modules existent in the device such as SPI, UART, PMP, etc., or memory itself.

The following are key features of the DMA Controller:

- Eight identical channels, each featuring:
 - Auto-increment source and destination address registers
 - Source and destination pointers
 - Memory to memory and memory to peripheral transfers
- Automatic word-size detection:
 - Transfer granularity, down to byte level
 - Bytes need not be word-aligned at source and destination
- Fixed priority channel arbitration

- Flexible DMA channel operating modes:
 - Manual (software) or automatic (interrupt) DMA requests
 - One-Shot or Auto-Repeat Block Transfer modes
 - Channel-to-channel chaining
- Flexible DMA requests:
 - A DMA request can be selected from any of the peripheral interrupt sources
 - Each channel can select any (appropriate) observable interrupt as its DMA request source
 - A DMA transfer abort can be selected from any of the peripheral interrupt sources
 - Up to 2-byte Pattern (data) match transfer termination
- Multiple DMA channel status interrupts:
 - DMA channel block transfer complete
 - Source empty or half empty
 - Destination full or half full
 - DMA transfer aborted due to an external event
 - Invalid DMA address generated
- DMA debug support features:
 - Most recent error address accessed by a DMA channel
 - Most recent DMA channel to transfer data
- CRC Generation module:
 - CRC module can be assigned to any of the available channels
 - CRC module is highly configurable

FIGURE 10-1: DMA BLOCK DIAGRAM

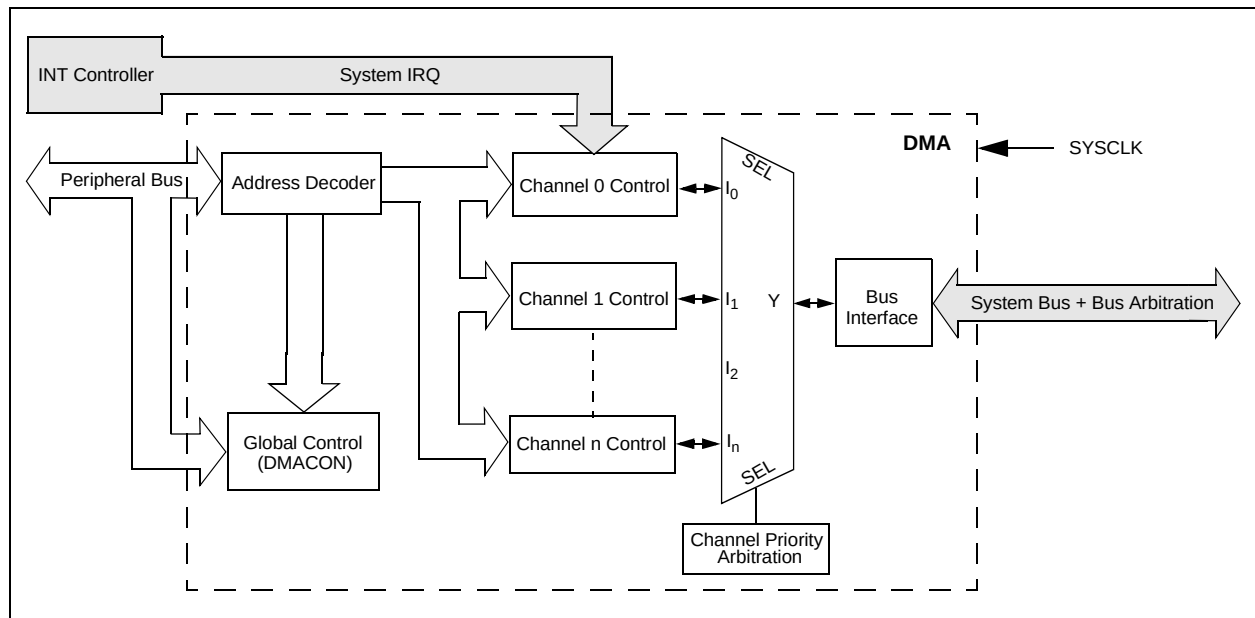


TABLE 10-3: DMA CHANNEL 0 THROUGH CHANNEL 7 REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name ⁽¹⁾	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
15B0	DCH7ECON	31:16	—	—	—	—	—	—	—	—	CHAIRQ<7:0>								00FF
		15:0	CHSIRQ<7:0>								CFORCE	CABORT	PATEN	SIRQEN	AIRQEN	—	—	—	FF00
15C0	DCH7INT	31:16	—	—	—	—	—	—	—	—	CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE	CHERIE	0000
		15:0	—	—	—	—	—	—	—	—	CHSDIF	CHSHIF	CHDDIF	CHDHIF	CHBCIF	CHCCIF	CHTAIF	CHERIF	0000
15D0	DCH7SSA	31:16	CHSSA<31:0>																0000
		15:0																	0000
15E0	DCH7DSA	31:16	CHDSA<31:0>																0000
		15:0																	0000
15F0	DCH7SSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSSIZ<15:0>																0000
1600	DCH7DSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDSIZ<15:0>																0000
1610	DCH7SPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSPTR<15:0>																0000
1620	DCH7DPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDPTR<15:0>																0000
1630	DCH7CSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCSIZ<15:0>																0000
1640	DCH7CPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCPTR<15:0>																0000
1650	DCH7DAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHPDAT<15:0>																0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 “CLR, SET, and INV Registers”** for more information.

TABLE 12-12: PORTE REGISTER MAP FOR 64-PIN DEVICES ONLY

Virtual Address (BF86_#)	Register Name(s)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0400	ANSELE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	ANSE7	ANSE6	ANSE5	ANSE4	—	—	—	—	00F0
0410	TRISE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	TRISE7	TRISE6	TRISE5	TRISE4	TRISE3	TRISE2	TRISE1	TRISE0	00FF
0420	PORTE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	RE7	RE6	RE5	RE4	RE3	RE2	RE1	RE0	xxxx
0430	LATE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	LATE7	LATE6	LATE5	LATE4	LATE3	LATE2	LATE1	LATE0	xxxx
0440	ODCE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	ODCE7	ODCE6	ODCE5	ODCE4	ODCE3	ODCE2	ODCE1	ODCE0	0000
0450	CNPUE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CNPUE7	CNPUE6	CNPUE5	CNPUE4	CNPUE3	CNPUE2	CNPUE1	CNPUE0	0000
0460	CNPDE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CNPDE7	CNPDE6	CNPDE5	CNPDE4	CNPDE3	CNPDE2	CNPDE1	CNPDE0	0000
0470	CNCONE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	EDGE DETECT	—	—	—	—	—	—	—	—	—	—	—	0000
0480	CNENE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CNENE7	CNENE6	CNENE5	CNENE4	CNENE3	CNENE2	CNENE1	CNENE0	0000
0490	CNSTATE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CN STATE7	CN STATE6	CN STATE5	CN STATE4	CN STATE3	CN STATE2	CN STATE1	CN STATE0	0000
04A0	CNNEE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CNNEE7	CNNEE6	CNNEE5	CNNEE4	CNNEE3	CNNEE2	CNNEE1	CNNEE0	0000
04B0	CNFE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CNFE7	CNFE6	CNFE5	CNFE4	CNFE3	CNFE2	CNFE1	CNFE0	0000
04C0	SRCON0E	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	SR0E3	SR0E2	SR0E1	SR0E0	0000
04D0	SRCON1E	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	SR1E3	SR1E2	SR1E1	SR1E0	0000

Legend: x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 “CLR, SET, and INV Registers”** for more information.

TABLE 12-16: PORTG REGISTER MAP FOR 64-PIN DEVICES ONLY

Virtual Address (BF86_#)	Register Name(s)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0600	ANSELG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	ANSG9	ANSG8	ANSG7	ANSG6	—	—	—	—	—	—	03C0
0610	TRISG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	TRISG9	TRISG8	TRISG7	TRISG6	—	—	—	—	—	—	03C0
0620	PORTG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	RG9	RG8	RG7	RG6	—	—	—	—	—	—	xxxx
0630	LATG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	LATG9	LATG8	LATG7	LATG6	—	—	—	—	—	—	xxxx
0640	ODCG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	ODCG9	ODCG8	ODCG7	ODCG6	—	—	—	—	—	—	0000
0650	CNPUG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CNPUG9	CNPUG8	CNPUG7	CNPUG6	—	—	—	—	—	—	0000
0660	CNPDG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CNPDG9	CNPDG8	CNPDG7	CNPDG6	—	—	—	—	—	—	0000
0670	CNCONG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	EDGE DETECT	—	—	—	—	—	—	—	—	—	—	—	0000
0680	CNENG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CNENG9	CNENG8	CNENG7	CNENG6	—	—	—	—	—	—	0000
0690	CNSTATG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CN STATG9	CN STATG8	CN STATG7	CN STATG6	—	—	—	—	—	—	0000
06A0	CNNEG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CNNEG9	CNNEG8	CNNEG7	CNNEG6	—	—	—	—	—	—	0000
06B0	CNFG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CNFG9	CNFG8	CNFG7	CNFG6	—	—	—	—	—	—	0000
06C0	SRCON0G	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	SR0G9	—	—	SR0G6	—	—	—	—	—	—	0000
06D0	SRCON1G	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	SR1G9	—	—	SR1G6	—	—	—	—	—	—	0000

Legend: x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 “CLR, SET, and INV Registers”** for more information.

TABLE 18-2: OUTPUT COMPARE 1 THROUGH OUTPUT COMPARE 9 REGISTER MAP (CONTINUED)

Virtual Address (BF84_#)	Register Name ⁽¹⁾	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
4A00	OC6CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	OC32	OCFLT	OCTSEL	OCM<2:0>			0000
4A10	OC6R	31:16	OC6R<31:0>																XXXX
		15:0																	XXXX
4A20	OC6RS	31:16	OC6RS<31:0>																XXXX
		15:0																	XXXX
4C00	OC7CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	OC32	OCFLT	OCTSEL	OCM<2:0>			0000
4C10	OC7R	31:16	OC7R<31:0>																XXXX
		15:0																	XXXX
4C20	OC7RS	31:16	OC7RS<31:0>																XXXX
		15:0																	XXXX
4E00	OC8CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	OC32	OCFLT	OCTSEL	OCM<2:0>			0000
4E10	OC8R	31:16	OC8R<31:0>																XXXX
		15:0																	XXXX
4E20	OC8RS	31:16	OC8RS<31:0>																XXXX
		15:0																	XXXX
5000	OC9CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	OC32	OCFLT	OCTSEL	OCM<2:0>			0000
5010	OC9R	31:16	OC9R<31:0>																XXXX
		15:0																	XXXX
5020	OC9RS	31:16 15:0	OC9RS<31:0>																XXXX

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 "CLR, SET, and INV Registers"** for more information.

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

REGISTER 20-26: SQI1XCON4: SQI XIP CONTROL REGISTER 4

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0 —	U-0 —	U-0 —	R/W-0 INIT2SCHECK	R/W-0 INIT2COUNT<1:0>	R/W-0	R/W-0 INIT2TYPE<1:0>	R/W-0
23:16	R/W-0	R/W-0	R/W-0	R/W-0 INIT2CMD3<7:0> ⁽¹⁾	R/W-0	R/W-0	R/W-0	R/W-0
15:8	R/W-0	R/W-0	R/W-0	R/W-0 INIT2CMD2<7:0> ⁽¹⁾	R/W-0	R/W-0	R/W-0	R/W-0
7:0	R/W-0	R/W-0	R/W-0	R/W-0 INIT2CMD1<7:0> ⁽¹⁾	R/W-0	R/W-0	R/W-0	R/W-0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-29 **Unimplemented:** Read as '0'

bit 28 **INIT2SCHECK:** Flash Initialization 2 Command Status Check bit

1 = Check the status after executing the INIT2 command

0 = Do not check the status

bit 27-26 **INIT2COUNT<1:0>:** Flash Initialization 2 Command Count bits

11 = INIT2CMD1, INIT2CMD2, and INIT2CMD3 are sent

10 = INIT2CMD1 and INIT2CMD2 are sent, but INIT2CMD3 is still pending

01 = INIT2CMD1 is sent, but INIT2CMD2 and INIT2CMD3 are still pending

00 = No commands are sent

bit 25-24 **INIT2TYPE<1:0>:** Flash Initialization 2 Command Type bits

11 = Reserved

10 = INIT2 commands are sent in Quad Lane mode

01 = INIT2 commands are sent in Dual Lane mode

00 = INIT2 commands are sent in Single Lane mode

bit 24-16 **INIT2CMD3<7:0>:** Flash Initialization Command 3 bits⁽¹⁾

Third command of the Flash initialization.

bit 15-8 **INIT2CMD2<7:0>:** Flash Initialization Command 2 bits⁽¹⁾

Second command of the Flash initialization.

bit 7-0 **INIT2CMD1<7:0>:** Flash Initialization Command 1 bits⁽¹⁾

First command of the Flash initialization.

Note 1: INIT2CMD1 can be WEN and INIT2CMD2 can be SECTOR UNPROTECT.

Note: Some Flash devices require Write Enable and Sector Unprotect commands before read/write operations and this register is useful in working with those Flash types (XIP mode only)

23.1 PMP Control Registers

TABLE 23-1: PARALLEL MASTER PORT REGISTER MAP

Virtual Address (BF82..#)	Register Name ⁽¹⁾	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
E000	PMCON	31:16	—	—	—	—	—	—	—	—	RDSTART	—	—	—	—	—	DUALBUF	—	0000
		15:0	ON	—	SIDL	ADRMUX<1:0>		PMPCTL	PTWREN	PTRDEN	CSF<1:0>		ALP	CS2P	CS1P	—	WRSP	RDSP	0000
E010	PMMODE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	BUSY	IRQM<1:0>		INCM<1:0>		MODE16	MODE<1:0>		WAITB<1:0>			WAITM<3:0>			WAITE<1:0>		0000
E020	PMADDR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CS2	CS1	ADDR<13:0>														0000
			ADDR15	ADDR14															0000
E030	PMDOUT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	DATAOUT<15:0>																0000
E040	PMDIN	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	DATAIN<15:0>																0000
E050	PMAEN	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PTEN<15:0>																0000
E060	PMSTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	IBF	IBOV	—	—	IB3F	IB2F	IB1F	IB0F	OBE	OBUF	—	—	OB3E	OB2E	OB1E	OB0E	008F
E070	PMWADDR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	WCS2	WCS1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
			WADDR15	WADDR14	WADDR<13:0>														0000
E080	PMRADDR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RCS2	RCS1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
			RADDR15	RADDR14	RADDR<13:0>														0000
E090	PMRDIN	31:16	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	15:0	RDATAIN<15:0>															

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 12.3 “CLR, SET, and INV Registers” for more information.

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

REGISTER 25-2: RTCALRM: REAL-TIME CLOCK ALARM CONTROL REGISTER (CONTINUED)

bit 7-0 **ARPT<7:0>**: Alarm Repeat Counter Value bits⁽²⁾

11111111 = Alarm will trigger 256 times

•
•
•

00000000 = Alarm will trigger one time

The counter decrements on any alarm event. The counter only rolls over from 0x00 to 0xFF if CHIME = 1.

Note 1: Hardware clears the ALRMEN bit anytime the alarm event occurs, when ARPT<7:0> = 00 and CHIME = 0.

2: This field should not be written when the RTCC ON bit = '1' (RTCCON<15>) and ALRMSYNC = 1.

Note: This register is reset only on a Power-on Reset (POR).

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

REGISTER 25-3: RTCTIME: REAL-TIME CLOCK TIME VALUE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	HR10<3:0>				HR01<3:0>			
23:16	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	MIN10<3:0>				MIN01<3:0>			
15:8	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	SEC10<3:0>				SEC01<3:0>			
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-28 **HR10<3:0>**: Binary-Coded Decimal Value of Hours bits, 10 digits; contains a value from 0 to 2

bit 27-24 **HR01<3:0>**: Binary-Coded Decimal Value of Hours bits, 1 digit; contains a value from 0 to 9

bit 23-20 **MIN10<3:0>**: Binary-Coded Decimal Value of Minutes bits, 10 digits; contains a value from 0 to 5

bit 19-16 **MIN01<3:0>**: Binary-Coded Decimal Value of Minutes bits, 1 digit; contains a value from 0 to 9

bit 15-12 **SEC10<3:0>**: Binary-Coded Decimal Value of Seconds bits, 10 digits; contains a value from 0 to 5

bit 11-8 **SEC01<3:0>**: Binary-Coded Decimal Value of Seconds bits, 1 digit; contains a value from 0 to 9

bit 7-0 **Unimplemented**: Read as '0'

Note: This register is only writable when RTCWREN = 1 (RTCCON<3>).

REGISTER 26-5: CESTAT: CRYPTO ENGINE STATUS REGISTER (CONTINUED)

bit 16 **ACTIVE:** Buffer Descriptor Processor Status bit

1 = BDP is active

0 = BDP is idle

bit 15-0 **BDCTRL<15:0>:** Descriptor Control Word Status bits

These bits contain the Control Word for the current Buffer Descriptor.

REGISTER 28-3: ADCCON3: ADC CONTROL REGISTER 3 (CONTINUED)

bit 18 **DIGEN2:** ADC2 Digital Enable bit
1 = ADC2 is digital enabled
0 = ADC2 is digital disabled

bit 17 **DIGEN1:** ADC1 Digital Enable bit
1 = ADC1 is digital enabled
0 = ADC1 is digital disabled

bit 16 **DIGEN0:** ADC0 Digital Enable bit
1 = ADC0 is digital enabled
0 = ADC0 is digital disabled

bit 15-13 **VREFSEL<2:0>:** Voltage Reference (VREF) Input Selection bits

VREFSEL<2:0>	ADREF+	ADREF-
1xx	Reserved; do not use	
011	External VREFH	External VREFL
010	AVDD	External VREFL
001	External VREFH	AVss
000	AVDD	AVss

bit 12 **TRGSUSP:** Trigger Suspend bit
1 = Triggers are blocked from starting a new analog-to-digital conversion, but the ADC module is not disabled
0 = Triggers are not blocked

bit 11 **UPDIEN:** Update Ready Interrupt Enable bit
1 = Interrupt will be generated when the UPDRDY bit is set by hardware
0 = No interrupt is generated

bit 10 **UPDRDY:** ADC Update Ready Status bit
1 = ADC SFRs can be updated
0 = ADC SFRs cannot be updated

Note: This bit is only active while the TRGSUSP bit is set and there are no more running conversions of any ADC modules.

bit 9 **SAMP:** Class 2 and Class 3 Analog Input Sampling Enable bit^(1,2,3,4)
1 = The ADC S&H amplifier is sampling
0 = The ADC S&H amplifier is holding

bit 8 **RQCNVRT:** Individual ADC Input Conversion Request bit
This bit and its associated ADINSEL<5:0> bits enable the user to individually request an analog-to-digital conversion of an analog input through software.
1 = Trigger the conversion of the selected ADC input as specified by the ADINSEL<5:0> bits
0 = Do not trigger the conversion

Note: This bit is automatically cleared in the next ADC clock cycle.

bit 7 **GLSWTRG:** Global Level Software Trigger bit
1 = Trigger conversion for ADC inputs that have selected the GLSWTRG bit as the trigger signal, either through the associated TRGSRC<4:0> bits in the ADCTRGx registers or through the STRGSRC<4:0> bits in the ADCCON1 register
0 = Do not trigger an analog-to-digital conversion

Note 1: The SAMP bit has the highest priority and setting this bit will keep the S&H circuit in Sample mode until the bit is cleared. Also, usage of the SAMP bit will cause settings of SAMC<9:0> bits (ADCCON2<25:16>) to be ignored.

2: The SAMP bit only connects Class 2 and Class 3 analog inputs to the shared ADC, ADC7. All Class 1 analog inputs are not affected by the SAMP bit.

3: The SAMP bit is not a self-clearing bit and it is the responsibility of application software to first clear this bit and only after setting the RQCNVRT bit to start the analog-to-digital conversion.

4: Normally, when the SAMP and RQCNVRT bits are used by software routines, all TRGSRCx<4:0> bits and STRGSRC<4:0> bits should be set to '00000' to disable all external hardware triggers and prevent them from interfering with the software-controlled sampling command signal SAMP and with the software-controlled trigger RQCNVRT.

REGISTER 28-32: ADCANCON: ADC ANALOG WARM-UP CONTROL REGISTER (CONTINUED)

- bit 7 **ANEN7:** Shared ADC (ADC7) Analog and Bias Circuitry Enable bit
1 = Analog and bias circuitry enabled. Once the analog and bias circuit is enabled, the ADC module needs a warm-up time, as defined by the WKUPCLKCNT<3:0> bits.
0 = Analog and bias circuitry disabled
- bit 5-6 **Unimplemented:** Read as '0'
- bit 4-0 **ANEN4:ANEN0:** ADC4-ADC0 Analog and Bias Circuitry Enable bits
1 = Analog and bias circuitry enabled. Once the analog and bias circuit is enabled, the ADC module needs a warm-up time, as defined by the WKUPCLKCNT<3:0> bits.
0 = Analog and bias circuitry disabled

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

REGISTER 29-10: CiFLTCON0: CAN FILTER CONTROL REGISTER 0

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN3	MSEL3<1:0>		FSEL3<4:0>				
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN2	MSEL2<1:0>		FSEL2<4:0>				
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN1	MSEL1<1:0>		FSEL1<4:0>				
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN0	MSEL0<1:0>		FSEL0<4:0>				

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31 **FLTEN3:** Filter 3 Enable bit

1 = Filter is enabled

0 = Filter is disabled

bit 30-29 **MSEL3<1:0>:** Filter 3 Mask Select bits

11 = Acceptance Mask 3 selected

10 = Acceptance Mask 2 selected

01 = Acceptance Mask 1 selected

00 = Acceptance Mask 0 selected

bit 28-24 **FSEL3<4:0>:** FIFO Selection bits

11111 = Message matching filter is stored in FIFO buffer 31

11110 = Message matching filter is stored in FIFO buffer 30

.

.

.

00001 = Message matching filter is stored in FIFO buffer 1

00000 = Message matching filter is stored in FIFO buffer 0

bit 23 **FLTEN2:** Filter 2 Enable bit

1 = Filter is enabled

0 = Filter is disabled

bit 22-21 **MSEL2<1:0>:** Filter 2 Mask Select bits

11 = Acceptance Mask 3 selected

10 = Acceptance Mask 2 selected

01 = Acceptance Mask 1 selected

00 = Acceptance Mask 0 selected

bit 20-16 **FSEL2<4:0>:** FIFO Selection bits

11111 = Message matching filter is stored in FIFO buffer 31

11110 = Message matching filter is stored in FIFO buffer 30

.

.

.

00001 = Message matching filter is stored in FIFO buffer 1

00000 = Message matching filter is stored in FIFO buffer 0

Note: The bits in this register can only be modified if the corresponding filter enable (FLTENN) bit is '0'.

NOTES:

FIGURE 37-22: PARALLEL MASTER PORT READ TIMING DIAGRAM

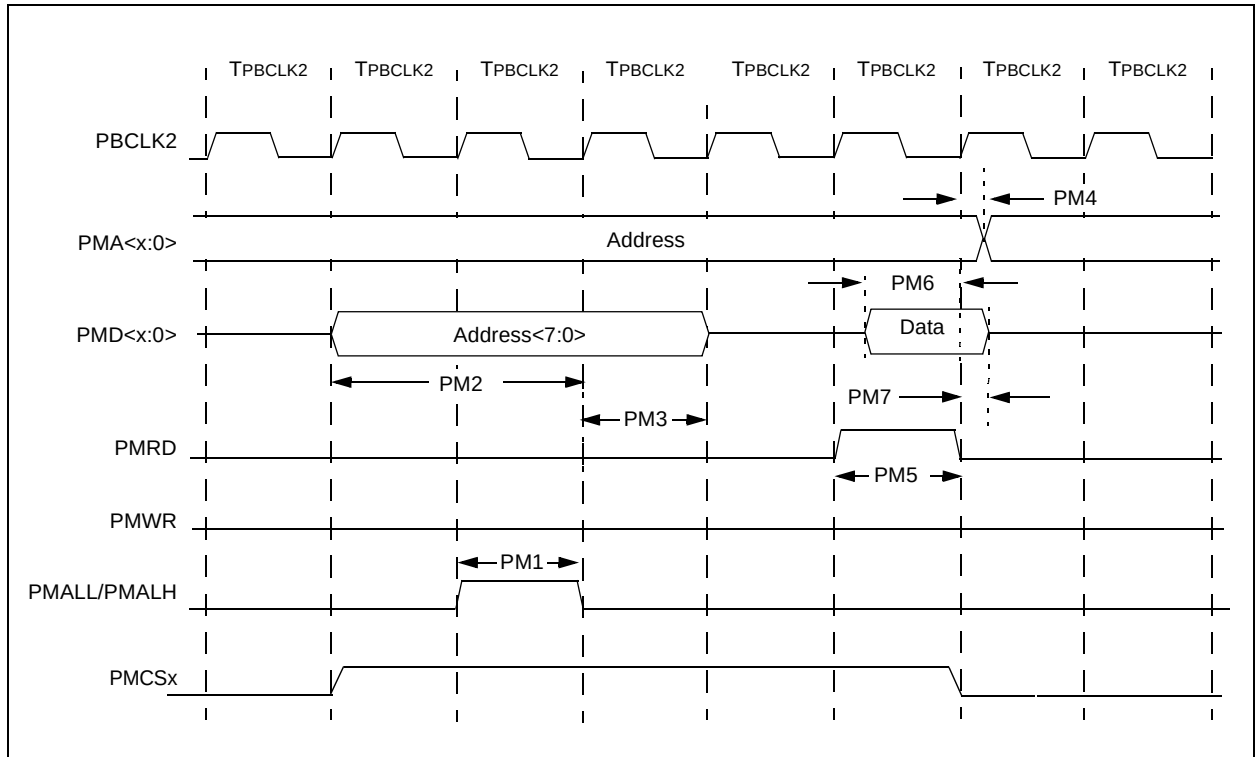


TABLE 37-43: PARALLEL MASTER PORT READ TIMING REQUIREMENTS

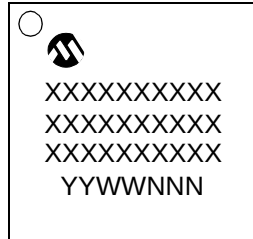
AC CHARACTERISTICS			Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ Ta ≤ +85°C for Industrial -40°C ≤ Ta ≤ +125°C for Extended				
Param. No.	Symbol	Characteristics ⁽¹⁾	Min.	Typ.	Max.	Units	Conditions
PM1	TLAT	PMALL/PMALH Pulse Width	—	1 TPBCLK2	—	—	—
PM2	TADSU	Address Out Valid to PMALL/PMALH Invalid (address setup time)	—	2 TPBCLK2	—	—	—
PM3	TADHOLD	PMALL/PMALH Invalid to Address Out Invalid (address hold time)	—	1 TPBCLK2	—	—	—
PM4	TAHOLD	PMRD Inactive to Address Out Invalid (address hold time)	5	—	—	ns	—
PM5	TRD	PMRD Pulse Width	—	1 TPBCLK2	—	—	—
PM6	TDSU	PMRD or PMENB Active to Data In Valid (data setup time)	15	—	—	ns	—
PM7	TDHOLD	PMRD or PMENB Inactive to Data In Invalid (data hold time)	—	80	—	ns	—

Note 1: These parameters are characterized, but not tested in manufacturing.

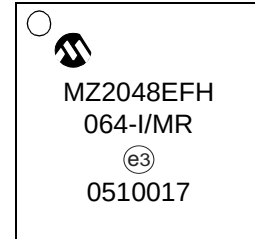
41.0 PACKAGING INFORMATION

41.1 Package Marking Information

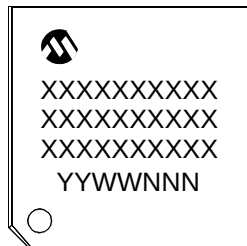
64-Lead QFN (9x9x0.9 mm)



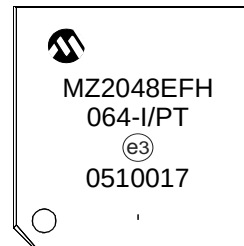
Example



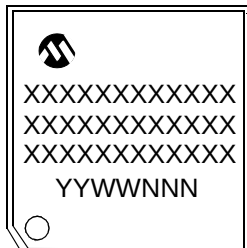
64-Lead TQFP (10x10x1 mm)



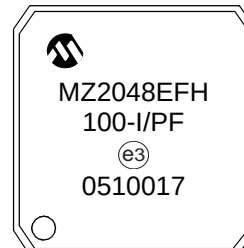
Example



100-Lead TQFP (14x14x1 mm)



Example



Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	*	Pb-free JEDEC designator for Matte Tin (Sn)
		This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.	

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

M

Memory Maps

Devices with 1024 KB Program Memory and 256 KB RAM	63
Devices with 1024 KB Program Memory and 512 KB RAM	64
Devices with 2048 KB Program Memory	65
Devices with 512 KB Program Memory	62
Memory Organization	61
Layout	61
Microchip Internet Web Site	733
MPLAB Assembler, Linker, Librarian	608
MPLAB ICD 3 In-Circuit Debugger System	609
MPLAB PM3 Device Programmer	609
MPLAB REAL ICE In-Circuit Emulator System	609
MPLAB X Integrated Development Environment Software	607
MPLINK Object Linker/MPLIB Object Librarian	608

O

Oscillator Configuration	153
Output Compare	309

P

Packaging	677
Details	679
Marking	677
Parallel Master Port (PMP)	369
PICKIT 3 In-Circuit Debugger/Programmer	609
Pinout I/O Descriptions	
ADC	16
Alternate Ethernet MII	33
Alternate Ethernet RMII	33
CAN	31
Comparators and CVREF	27
EBI	29
Ethernet MII	32
Ethernet RMII	32
External Interrupts	19
I2C	27
Input Capture	18
JTAG, Trace, and Programming/Debugging	35
Oscillator	18
Output Compare	19
PMP	28
Ports	20
Power, Ground, and Voltage Reference	34
SPI	26
SQI	34
Timers	24
UART	25
USB	31
Power-on Reset (POR) and On-Chip Voltage Regulator	603
Power-Saving Features	575
with CPU Running	575
Prefetch Module	169

R

Random Number Generator (RNG)	421
Real-Time Clock and Calendar (RTCC)	391
Register Map	
ADEVCFG (Alternate Device Configuration Word Summary)	583
CAN1 Register Summary	486

CAN2 Register Summary	488
Comparator	568
Comparator Voltage Reference	572
Deadman Timer	294
DEVCFG (Device Configuration Word Summary)	582
Device ADC Calibration Summary	585
Device ID, Revision, and Configuration Summary	584
Device Serial Number Summary	584
DMA Channel 0-7	175
DMA CRC	174
DMA Global	174
EBI	384
Ethernet Controller Register Summary	525
Flash Controller	100
I2C1 Through I2C5	355
Input Capture 1-9	307
Interrupt	126
Oscillator Configuration	156
Output Compare1-9	311
Parallel Master Port	370
Peripheral Pin Select Input	274
Peripheral Pin Select Output	278
PORTA	256
PORTB	257
PORTC	258, 259
PORTD	260, 261, 262
ORTE	263, 264
PORTF	265, 266
PORTG	268
PORTH	269, 270
PORTJ	271, 272
PORTK	273
Prefetch	170
Resets	110
RTCC	392
SPI1 through SPI6	316
System Bus	76
System Bus Target 0	76
System Bus Target 1	77
System Bus Target 10	87
System Bus Target 11	88
System Bus Target 12	89
System Bus Target 13	90
System Bus Target 2	79
System Bus Target 3	80
System Bus Target 4	81
System Bus Target 5	82
System Bus Target 6	83
System Bus Target 7	84
System Bus Target 8	85
System Bus Target 9	86
Timer1	284
Timer1-Timer9	289
UART1-6	362
USB	199, 205
Watchdog Timer	302

Registers

[pin name]R (Peripheral Pin Select Input)	281
ADCANCON (ADC Analog Warm-up Control Register)	480
ADCBASE (ADC Base)	473
ADCCMP1CON (ADC Digital Comparator 1 Control Register)	467
ADCCMPENx (ADC Digital Comparator 'x' Enable Register ('x' = 1 through 6))	460

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

DMSTAT (Deadman Timer Status)	297
DMTCLR (Deadman Timer Clear)	296
DMTCNT (Deadman Timer Count)	298
DMTCON (Deadman Timer Control)	295
DMTPRECLR (Deadman Timer Preclear)	295
DMTPSINTV (Post Status Configure DMT Interval Status)	299
EBICSx (External Bus Interface Chip Select)	385
EBIFTRPDx (External Bus Interface Flash Timing) ..	388
EBIMSKx (External Bus Interface Address Mask)	386
EBISMCON (External Bus Interface Static Memory Control)	389
EBISMTx (External Bus Interface Static Memory Timing) ..	387
EMAC1CFG1 (Ethernet Controller MAC Configuration 1) ..	550
EMAC1CFG2 (Ethernet Controller MAC Configuration 2) ..	551
EMAC1CLRT (Ethernet Controller MAC Collision Window/Retry Limit)	555
EMAC1IPGR (Ethernet Controller MAC Non-Back-to-Back Interpacket Gap)	554
EMAC1IPGT (Ethernet Controller MAC Back-to-Back Interpacket Gap)	553
EMAC1MADR (Ethernet Controller MAC MII Management Address)	561
EMAC1MAXF (Ethernet Controller MAC Maximum Frame Length)	556
EMAC1MCFG (Ethernet Controller MAC MII Management Configuration)	559
EMAC1MCMD (Ethernet Controller MAC MII Management Command)	560
EMAC1MIND (Ethernet Controller MAC MII Management Indicators)	563
EMAC1MRDD (Ethernet Controller MAC MII Management Read Data)	562
EMAC1MWTD (Ethernet Controller MAC MII Management Write Data)	562
EMAC1SA0 (Ethernet Controller MAC Station Address 0)	564
EMAC1SA1 (Ethernet Controller MAC Station Address 1)	565
EMAC1SA2 (Ethernet Controller MAC Station Address 2)	566
EMAC1SUPP (Ethernet Controller MAC PHY Support) ..	557
EMAC1TEST (Ethernet Controller MAC Test)	558
ETHALGNERR (Ethernet Controller Alignment Errors Statistics)	549
ETHCON1 (Ethernet Controller Control 1)	528
ETHCON2 (Ethernet Controller Control 2)	530
ETHFCSERR (Ethernet Controller Frame Check Sequence Error Statistics)	548
ETHFRMRXOK (Ethernet Controller Frames Received OK Statistics)	547
ETHFRMTXOK (Ethernet Controller Frames Transmitted OK Statistics)	544
ETHHT0 (Ethernet Controller Hash Table 0)	532
ETHHT1 (Ethernet Controller Hash Table 1)	532
ETHIEN (Ethernet Controller Interrupt Enable)	538
ETHIRQ (Ethernet Controller Interrupt Request)	539
ETHMCOLFRM (Ethernet Controller Multiple Collision Frames Statistics)	546
ETHPM0 (Ethernet Controller Pattern Match Offset) ..	534
ETHPMCS (Ethernet Controller Pattern Match Checksum)	534
ETHPMM0 (Ethernet Controller Pattern Match Mask 0) ..	533
ETHPMM1 (Ethernet Controller Pattern Match Mask 1) ..	533
ETHRXFC (Ethernet Controller Receive Filter Configuration)	535
ETHRXOVFLOW (Ethernet Controller Receive Overflow Statistics)	543
ETHRXST (Ethernet Controller RX Packet Descriptor Start Address)	531
ETHRXWM (Ethernet Controller Receive Watermarks) ..	537
ETHSCOLFRM (Ethernet Controller Single Collision Frames Statistics)	545
ETHSTAT (Ethernet Controller Status)	541
ETHTXST (Ethernet Controller TX Packet Descriptor Start Address)	531
FCCR (Floating Point Condition Codes Register - CP1 Register 25)	56
FCSR (Floating Point Control and Status Register - CP1 Register 31)	59
FENR (Floating Point Exceptions and Modes Enable Register - CP1 Register 28)	58
FEXR (Floating Point Exceptions Status Register - CP1 Register 26)	57
FIR (Floating Point Implementation Register - CP1 Register 0)	55
I2CxCON (I2C Control)	357
I2CxSTAT (I2C Status)	359
ICxCON (Input Capture x Control)	308
IECx (Interrupt Enable Control)	149
IFSx (Interrupt Flag Status)	149
INTCON (Interrupt Control)	145
INTSTAT (Interrupt Status)	148
IPCx (Interrupt Priority Control)	150
IPTM (Interrupt Proximity Timer)	148
NVMADDR (Flash Address)	104
NVMBWP (Flash Boot (Page) Write-protect)	107
NVMCON (Programming Control)	101, 103
NVMDATAx (Flash Data ('x' = 0-3))	105
NVMKEY (Programming Unlock)	104
NVMPWP (Program Flash Write-Protect)	106
NVMSRCADDR (Source Data Address)	105
OCxCON (Output Compare x Control)	313
OSCCON (Oscillator Control)	158
OSCTUN (FRC Tuning)	160
PMADDR (Parallel Port Address)	375
PMAEN (Parallel Port Pin Enable)	377
PMCON (Parallel Port Control)	371
PMDIN (Parallel Port Input Data)	376, 381
PMDOUT (Parallel Port Output Data)	376
PMODE (Parallel Port Mode)	373
PMRADDR (Parallel Port Read Address)	380
PMSTAT (Parallel Port Status (Slave Modes Only)) ..	378
PMWADDR (Parallel Port Write Address)	379
PRECON (Prefetch Module Control)	171
PRESTAT (Prefetch Module Status)	172
PRISS (Priority Shadow Select)	146
PSCNT (Post Status Configure DMT Count Status) ..	298
PWRCON (Power Control)	114
REFOxCON (Reference Oscillator Control ('x' = 1-4)) ...	163
REFOxTRIM (Reference Oscillator Trim ('x' = 1-4)) ..	164
RNMICON (Non-maskable Interrupt Control)	113