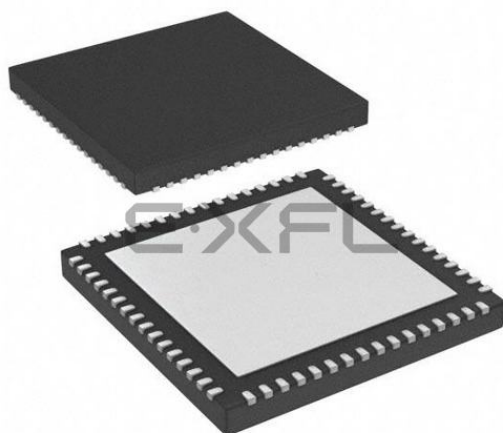




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Details

Product Status	Active
Core Processor	MIPS32® M-Class
Core Size	32-Bit Single-Core
Speed	250MHz
Connectivity	CANbus, Ethernet, I ² C, PMP, SPI, SQI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	46
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	2.1V ~ 3.6V
Data Converters	A/D 24x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 80°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mz2048efh064-250i-mr

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

TABLE 1-6: PORTA THROUGH PORTK PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number				Pin Type	Buffer Type	Description
	64-pin QFN/ TQFP	100-pin TQFP	124-pin VTLA	144-pin TQFP/ LQFP			
PORTD							
RD0	46	71	A48	104	I/O	ST	PORTD is a bidirectional I/O port
RD1	49	76	A52	109	I/O	ST	
RD2	50	77	B42	110	I/O	ST	
RD3	51	78	A53	111	I/O	ST	
RD4	52	81	A56	118	I/O	ST	
RD5	53	82	B46	119	I/O	ST	
RD6	—	—	A57	120	I/O	ST	
RD7	—	—	B47	121	I/O	ST	
RD9	43	68	B38	97	I/O	ST	
RD10	44	69	A46	98	I/O	ST	
RD11	45	70	B39	99	I/O	ST	
RD12	—	79	B43	112	I/O	ST	
RD13	—	80	A54	113	I/O	ST	
RD14	—	47	B27	69	I/O	ST	
RD15	—	48	A32	70	I/O	ST	
PORTE							
RE0	58	91	B52	135	I/O	ST	PORTE is a bidirectional I/O port
RE1	61	94	A64	138	I/O	ST	
RE2	62	98	A66	142	I/O	ST	
RE3	63	99	B56	143	I/O	ST	
RE4	64	100	A67	144	I/O	ST	
RE5	1	3	A3	3	I/O	ST	
RE6	2	4	B2	4	I/O	ST	
RE7	3	5	A4	5	I/O	ST	
RE8	—	18	B10	23	I/O	ST	
RE9	—	19	A12	24	I/O	ST	
PORTF							
RF0	56	85	A59	124	I/O	ST	PORTF is a bidirectional I/O port
RF1	57	86	B49	125	I/O	ST	
RF2	—	57	B31	79	I/O	ST	
RF3	38	56	A38	78	I/O	ST	
RF4	41	64	B36	90	I/O	ST	
RF5	42	65	A44	91	I/O	ST	
RF8	—	58	A39	80	I/O	ST	
RF12	—	40	B22	58	I/O	ST	
RF13	—	39	A26	57	I/O	ST	

Legend: CMOS = CMOS-compatible input or output Analog = Analog input P = Power
ST = Schmitt Trigger input with CMOS levels O = Output I = Input
TTL = Transistor-transistor Logic input buffer PPS = Peripheral Pin Select

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

TABLE 1-6: PORTA THROUGH PORTK PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number				Pin Type	Buffer Type	Description
	64-pin QFN/ TQFP	100-pin TQFP	124-pin VTLA	144-pin TQFP/ LQFP			
PORTG							
RG0	—	88	B50	128	I/O	ST	PORTG is a bidirectional I/O port
RG1	—	87	A60	127	I/O	ST	
RG6	4	10	B6	14	I/O	ST	
RG7	5	11	A8	15	I/O	ST	
RG8	6	12	B7	16	I/O	ST	
RG9	10	16	B9	21	I/O	ST	
RG12	—	96	A65	140	I/O	ST	
RG13	—	97	B55	141	I/O	ST	
RG14	—	95	B54	139	I/O	ST	
RG15	—	1	A2	1	I/O	ST	
PORTH							
RH0	—	—	B17	43	I/O	ST	PORTH is a bidirectional I/O port
RH1	—	—	A22	44	I/O	ST	
RH2	—	—	—	45	I/O	ST	
RH3	—	—	—	46	I/O	ST	
RH4	—	—	A30	65	I/O	ST	
RH5	—	—	B26	66	I/O	ST	
RH6	—	—	A31	67	I/O	ST	
RH7	—	—	—	68	I/O	ST	
RH8	—	—	B32	81	I/O	ST	
RH9	—	—	A40	82	I/O	ST	
RH10	—	—	B33	83	I/O	ST	
RH11	—	—	—	84	I/O	ST	
RH12	—	—	A47	100	I/O	ST	
RH13	—	—	B40	101	I/O	ST	
RH14	—	—	—	102	I/O	ST	
RH15	—	—	—	103	I/O	ST	
PORTJ							
RJ0	—	—	B44	114	I/O	ST	PORTJ is a bidirectional I/O port
RJ1	—	—	A55	115	I/O	ST	
RJ2	—	—	B45	116	I/O	ST	
RJ3	—	—	—	117	I/O	ST	
RJ4	—	—	A62	131	I/O	ST	
RJ5	—	—	—	132	I/O	ST	
RJ6	—	—	—	133	I/O	ST	
RJ7	—	—	—	134	I/O	ST	
RJ8	—	—	A5	7	I/O	ST	
RJ9	—	—	B4	8	I/O	ST	
RJ10	—	—	—	10	I/O	ST	
RJ11	—	—	B12	27	I/O	ST	
RJ12	—	—	—	9	I/O	ST	
RJ13	—	—	—	28	I/O	ST	
RJ14	—	—	—	29	I/O	ST	
RJ15	—	—	—	30	I/O	ST	

Legend: CMOS = CMOS-compatible input or output
ST = Schmitt Trigger input with CMOS levels
TTL = Transistor-transistor Logic input buffer

Analog = Analog input
O = Output
PPS = Peripheral Pin Select

P = Power
I = Input

4.1.1 BOOT FLASH SEQUENCE AND CONFIGURATION SPACES

Sequence space is used to identify which boot Flash is aliased by aliased regions. If the value programmed into the TSEQ<15:0> bits of the BF1SEQ3 word is equal to or greater than the value programmed into the TSEQ<15:0> bits of the BF2SEQ3 word, boot Flash 1 is aliased by the lower boot alias region, and boot Flash 2 is aliased by the upper boot alias region. If the TSEQ<15:0> bits of the BF2SEQ3 word is greater than the TSEQ<15:0> bits of the BF1SEQ3 word, the opposite is true (see Table 4-2 and Table 4-3 for BFxSEQ3 word memory locations).

The CSEQ<15:0> bits must contain the one's complement value of the TSEQ<15:0> bits; otherwise, the value of the TSEQ<15:0> bits is considered invalid, and an alternate sequence is used. See **Section 4.1.2 “Alternate Sequence and Configuration Words”** for more information.

Once boot Flash memories are aliased, configuration space located in the lower boot alias region is used as the basis for the Configuration words, DEVSIGN0, DEVCP0, and DEVCFGx (and the associated alternate configuration registers). This means that the boot Flash region to be aliased by lower boot alias region memory must contain configuration values in the appropriate memory locations.

Note: Do not use word program operation (NVMOP<3:0> = 0001) when programming data into the sequence and configuration spaces.
--

4.1.2 ALTERNATE SEQUENCE AND CONFIGURATION WORDS

Every word in the configuration space and sequence space has an associated alternate word (designated by the letter A as the first letter in the name of the word). During device start-up, primary words are read and if uncorrectable ECC errors are found, the BCFGERR (RCON<27>) flag is set and alternate words are used. If uncorrectable ECC errors are found in primary and alternate words, the BCFGFAIL (RCON<26>) flag is set and the default configuration is used.

TABLE 4-2: BOOT FLASH 1 SEQUENCE AND CONFIGURATION WORDS SUMMARY

Virtual Address (BFC4_#)	Register Name	Bit Range	Bits																All Reset
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
FF40	ABF1DEVCFG3	31:0	Note: See Table 34-2 for the bit descriptions.																XXXX
FF44	ABF1DEVCFG2	31:0																	XXXX
FF48	ABF1DEVCFG1	31:0																	XXXX
FF4C	ABF1DEVCFG0	31:0																	XXXX
FF50	ABF1DEVCP3	31:0																	XXXX
FF54	ABF1DEVCP2	31:0																	XXXX
FF58	ABF1DEVCP1	31:0																	XXXX
FF5C	ABF1DEVCP0	31:0																	XXXX
FF60	ABF1DEVSIGN3	31:0																	XXXX
FF64	ABF1DEVSIGN2	31:0																	XXXX
FF68	ABF1DEVSIGN1	31:0																	XXXX
FF6C	ABF1DEVSIGN0	31:0																	XXXX
FFC0	BF1DEVCFG3	31:0	Note: See Table 34-1 for the bit descriptions.																XXXX
FFC4	BF1DEVCFG2	31:0																	XXXX
FFC8	BF1DEVCFG1	31:0																	XXXX
FFCC	BF1DEVCFG0	31:0																	XXXX
FFD0	BF1DEVCP3	31:0																	XXXX
FFD4	BF1DEVCP2	31:0																	XXXX
FFD8	BF1DEVCP1	31:0																	XXXX
FFDC	BF1DEVCP0	31:0																	XXXX
FFE0	BF1DEVSIGN3	31:0																	XXXX
FFE4	BF1DEVSIGN2	31:0																	XXXX
FFE8	BF1DEVSIGN1	31:0																	XXXX
FFEC	BF1DEVSIGN0	31:0																	XXXX
FFF0	BF1SEQ3	31:16	CSEQ<15:0>																XXXX
		15:0	TSEQ<15:0>																XXXX
FFF4	BF1SEQ2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	XXXX	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	XXXX	
FFF8	BF1SEQ1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	XXXX	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	XXXX	
FFFC	BF1SEQ0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	XXXX	
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	XXXX	

Legend: x = unknown value on Reset; — = Reserved, read as '1'. Reset values are shown in hexadecimal.

4.2 System Bus Arbitration

Note: The System Bus interconnect implements one or more instantiations of the SonicsSX[®] interconnect from Sonics, Inc. This document contains materials that are (c) 2003-2015 Sonics, Inc., and that constitute proprietary information of Sonics, Inc. SonicsSX is a registered trademark of Sonics, Inc. All such materials and trademarks are used under license from Sonics, Inc.

As shown in the PIC32MZ EF Family Block Diagram (see Figure 1-1), there are multiple initiator modules (I1 through I14) in the system that can access various target modules (T1 through T13). Table 4-4 illustrates which initiator can access which target. The System Bus supports simultaneous access to targets by initiators, so long as the initiators are accessing different targets. The System Bus will perform arbitration, if multiple initiators attempt to access the same target.

TABLE 4-18: SYSTEM BUS TARGET 10 REGISTER MAP

Virtual Address (BF8E_#)	Register Name	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	
A820	SBT10ELOG1	31:16	MULTI	—	—	—	CODE<3:0>				—	—	—	—	—	—	—	0000
		15:0	INITID<7:0>							REGION<3:0>				—	CMD<2:0>			0000
A824	SBT10ELOG2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	GROUP<1:0>		0000
A828	SBT10ECON	31:16	—	—	—	—	—	—	ERRP	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
A830	SBT10ECLRS	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
A838	SBT10ECLRM	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
A840	SBT10REG0	31:16	BASE<21:6>															xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—
A850	SBT10RD0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0
A858	SBT10WR0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note: For reset values listed as 'xxxx', please refer to Table 4-6 for the actual reset values.

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

REGISTER 6-2: RSWRST: SOFTWARE RESET REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	W-0, HC
	—	—	—	—	—	—	—	SWRST ^(1,2)

Legend:

R = Readable bit
 W = Writable bit
 U = Unimplemented bit, read as '0'
 -n = Value at POR
 '1' = Bit is set
 '0' = Bit is cleared
 x = Bit is unknown

bit 31-1 **Unimplemented:** Read as '0'

bit 0 **SWRST:** Software Reset Trigger bit^(1,2)
 1 = Enable software Reset event
 0 = No effect

Note 1: The system unlock sequence must be performed before the SWRST bit can be written. Refer to **Section 42. "Oscillators with Enhanced PLL"** in the *"PIC32 Family Reference Manual"* for details.

2: Once this bit is set, any read of the RSWRST register will cause a reset to occur.

7.2 Interrupts

The PIC32MZ EF family uses variable offsets for vector spacing. This allows the interrupt vector spacing to be configured according to application needs. A unique interrupt vector offset can be set for each vector using its associated OFFx register.

For details on the Variable Offset feature, refer to **8.5.2 “Variable Offset”** in **Section 8. “Interrupt Controller”** (DS60001108) of the *“PIC32 Family Reference Manual”*.

Table 7-2 provides the Interrupt IRQ, vector and bit location information.

TABLE 7-2: INTERRUPT IRQ, VECTOR, AND BIT LOCATION

Interrupt Source ⁽¹⁾	XC32 Vector Name	IRQ #	Vector #	Interrupt Bit Location				Persistent Interrupt
				Flag	Enable	Priority	Sub-priority	
Highest Natural Order Priority								
Core Timer Interrupt	_CORE_TIMER_VECTOR	0	OFF000<17:1>	IFS0<0>	IEC0<0>	IPC0<4:2>	IPC0<1:0>	No
Core Software Interrupt 0	_CORE_SOFTWARE_0_VECTOR	1	OFF001<17:1>	IFS0<1>	IEC0<1>	IPC0<12:10>	IPC0<9:8>	No
Core Software Interrupt 1	_CORE_SOFTWARE_1_VECTOR	2	OFF002<17:1>	IFS0<2>	IEC0<2>	IPC0<20:18>	IPC0<17:16>	No
External Interrupt 0	_EXTERNAL_0_VECTOR	3	OFF003<17:1>	IFS0<3>	IEC0<3>	IPC0<28:26>	IPC0<25:24>	No
Timer1	_TIMER_1_VECTOR	4	OFF004<17:1>	IFS0<4>	IEC0<4>	IPC1<4:2>	IPC1<1:0>	No
Input Capture 1 Error	_INPUT_CAPTURE_1_ERROR_VECTOR	5	OFF005<17:1>	IFS0<5>	IEC0<5>	IPC1<12:10>	IPC1<9:8>	Yes
Input Capture 1	_INPUT_CAPTURE_1_VECTOR	6	OFF006<17:1>	IFS0<6>	IEC0<6>	IPC1<20:18>	IPC1<17:16>	Yes
Output Compare 1	_OUTPUT_COMPARE_1_VECTOR	7	OFF007<17:1>	IFS0<7>	IEC0<7>	IPC1<28:26>	IPC1<25:24>	No
External Interrupt 1	_EXTERNAL_1_VECTOR	8	OFF008<17:1>	IFS0<8>	IEC0<8>	IPC2<4:2>	IPC2<1:0>	No
Timer2	_TIMER_2_VECTOR	9	OFF009<17:1>	IFS0<9>	IEC0<9>	IPC2<12:10>	IPC2<9:8>	No
Input Capture 2 Error	_INPUT_CAPTURE_2_ERROR_VECTOR	10	OFF010<17:1>	IFS0<10>	IEC0<10>	IPC2<20:18>	IPC2<17:16>	Yes
Input Capture 2	_INPUT_CAPTURE_2_VECTOR	11	OFF011<17:1>	IFS0<11>	IEC0<11>	IPC2<28:26>	IPC2<25:24>	Yes
Output Compare 2	_OUTPUT_COMPARE_2_VECTOR	12	OFF012<17:1>	IFS0<12>	IEC0<12>	IPC3<4:2>	IPC3<1:0>	No
External Interrupt 2	_EXTERNAL_2_VECTOR	13	OFF013<17:1>	IFS0<13>	IEC0<13>	IPC3<12:10>	IPC3<9:8>	No
Timer3	_TIMER_3_VECTOR	14	OFF014<17:1>	IFS0<14>	IEC0<14>	IPC3<20:18>	IPC3<17:16>	No
Input Capture 3 Error	_INPUT_CAPTURE_3_ERROR_VECTOR	15	OFF015<17:1>	IFS0<15>	IEC0<15>	IPC3<28:26>	IPC3<25:24>	Yes
Input Capture 3	_INPUT_CAPTURE_3_VECTOR	16	OFF016<17:1>	IFS0<16>	IEC0<16>	IPC4<4:2>	IPC4<1:0>	Yes
Output Compare 3	_OUTPUT_COMPARE_3_VECTOR	17	OFF017<17:1>	IFS0<17>	IEC0<17>	IPC4<12:10>	IPC4<9:8>	No
External Interrupt 3	_EXTERNAL_3_VECTOR	18	OFF018<17:1>	IFS0<18>	IEC0<18>	IPC4<20:18>	IPC4<17:16>	No
Timer4	_TIMER_4_VECTOR	19	OFF019<17:1>	IFS0<19>	IEC0<19>	IPC4<28:26>	IPC4<25:24>	No
Input Capture 4 Error	_INPUT_CAPTURE_4_ERROR_VECTOR	20	OFF020<17:1>	IFS0<20>	IEC0<20>	IPC5<4:2>	IPC5<1:0>	Yes
Input Capture 4	_INPUT_CAPTURE_4_VECTOR	21	OFF021<17:1>	IFS0<21>	IEC0<21>	IPC5<12:10>	IPC5<9:8>	Yes

Note 1: Not all interrupt sources are available on all devices. See **TABLE 1: “PIC32MZ EF Family Features”** for the list of available peripherals.

- 2:** This interrupt source is not available on 64-pin devices.
- 3:** This interrupt source is not available on 100-pin devices.
- 4:** This interrupt source is not available on 124-pin devices.

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

REGISTER 7-7: IPCx: INTERRUPT PRIORITY CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	IP3<2:0>			IS3<1:0>	
23:16	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	IP2<2:0>			IS2<1:0>	
15:8	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	IP1<2:0>			IS1<1:0>	
7:0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	IP0<2:0>			IS0<1:0>	

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-29 **Unimplemented:** Read as '0'

bit 28-26 **IP3<2:0>:** Interrupt Priority bits

111 = Interrupt priority is 7

.

.

.

010 = Interrupt priority is 2

001 = Interrupt priority is 1

000 = Interrupt is disabled

bit 25-24 **IS3<1:0>:** Interrupt Subpriority bits

11 = Interrupt subpriority is 3

10 = Interrupt subpriority is 2

01 = Interrupt subpriority is 1

00 = Interrupt subpriority is 0

bit 23-21 **Unimplemented:** Read as '0'

bit 20-18 **IP2<2:0>:** Interrupt Priority bits

111 = Interrupt priority is 7

.

.

.

010 = Interrupt priority is 2

001 = Interrupt priority is 1

000 = Interrupt is disabled

bit 17-16 **IS2<1:0>:** Interrupt Subpriority bits

11 = Interrupt subpriority is 3

10 = Interrupt subpriority is 2

01 = Interrupt subpriority is 1

00 = Interrupt subpriority is 0

bit 15-13 **Unimplemented:** Read as '0'

Note: This register represents a generic definition of the IPCx register. Refer to Table 7-2 for the exact bit definitions.

REGISTER 7-7: IPCx: INTERRUPT PRIORITY CONTROL REGISTER (CONTINUED)

bit 12-10 **IP1<2:0>**: Interrupt Priority bits

111 = Interrupt priority is 7

•
•
•

010 = Interrupt priority is 2

001 = Interrupt priority is 1

000 = Interrupt is disabled

bit 9-8 **IS1<1:0>**: Interrupt Subpriority bits

11 = Interrupt subpriority is 3

10 = Interrupt subpriority is 2

01 = Interrupt subpriority is 1

00 = Interrupt subpriority is 0

bit 7-5 **Unimplemented**: Read as '0'

bit 4-2 **IP0<2:0>**: Interrupt Priority bits

111 = Interrupt priority is 7

•
•
•

010 = Interrupt priority is 2

001 = Interrupt priority is 1

000 = Interrupt is disabled

bit 1-0 **IS0<1:0>**: Interrupt Subpriority bits

11 = Interrupt subpriority is 3

10 = Interrupt subpriority is 2

01 = Interrupt subpriority is 1

00 = Interrupt subpriority is 0

Note: This register represents a generic definition of the IPCx register. Refer to Table 7-2 for the exact bit definitions.
--

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

TABLE 12-3: OUTPUT PIN SELECTION

RPN Port Pin	RPNR SFR	RPNR bits	RPNR Value to Peripheral Selection
RPD2	RPD2R	RPD2R<3:0>	0000 = No Connect
RPG8	RPG8R	RPG8R<3:0>	0001 = U3TX
RPF4	RPF4R	RPF4R<3:0>	0010 = U4RTS
RPD10	RPD10R	RPD10R<3:0>	0011 = Reserved
RPF1	RPF1R	RPF1R<3:0>	0100 = Reserved
RPB9	RPB9R	RPB9R<3:0>	0101 = SDO1
RPB10	RPB10R	RPB10R<3:0>	0110 = SDO2
RPC14	RPC14R	RPC14R<3:0>	0111 = SDO3
RPB5	RPB5R	RPB5R<3:0>	1000 = Reserved
RPC1 ⁽¹⁾	RPC1R ⁽¹⁾	RPC1R<3:0> ⁽¹⁾	1001 = SDO5 ⁽¹⁾
RPD14 ⁽¹⁾	RPD14R ⁽¹⁾	RPD14R<3:0> ⁽¹⁾	1010 = SS6 ⁽¹⁾
RPG1 ⁽¹⁾	RPG1R ⁽¹⁾	RPG1R<3:0> ⁽¹⁾	1011 = OC3
RPA14 ⁽¹⁾	RPA14R ⁽¹⁾	RPA14R<3:0> ⁽¹⁾	1100 = OC6
RPD6 ⁽²⁾	RPD6R ⁽²⁾	RPD6R<3:0> ⁽²⁾	1101 = REFCLKO4
			1110 = C2OUT
			1111 = C1TX ⁽³⁾
RPD3	RPD3R	RPD3R<3:0>	0000 = No Connect
RPG7	RPG7R	RPG7R<3:0>	0001 = U1TX
RPF5	RPF5R	RPF5R<3:0>	0010 = U2RTS
RPD11	RPD11R	RPD11R<3:0>	0011 = U5TX
RPF0	RPF0R	RPF0R<3:0>	0100 = U6RTS
RPB1	RPB1R	RPB1R<3:0>	0101 = SDO1
RPE5	RPE5R	RPE5R<3:0>	0110 = SDO2
RPC13	RPC13R	RPC13R<3:0>	0111 = SDO3
RPB3	RPB3R	RPB3R<3:0>	1000 = SDO4
RPC4 ⁽¹⁾	RPC4R ⁽¹⁾	RPC4R<3:0> ⁽¹⁾	1001 = SDO5 ⁽¹⁾
RPD15 ⁽¹⁾	RPD15R ⁽¹⁾	RPD15R<3:0> ⁽¹⁾	1010 = Reserved
RPG0 ⁽¹⁾	RPG0R ⁽¹⁾	RPG0R<3:0> ⁽¹⁾	1011 = OC4
RPA15 ⁽¹⁾	RPA15R ⁽¹⁾	RPA15R<3:0> ⁽¹⁾	1100 = OC7
RPD7 ⁽²⁾	RPD7R ⁽²⁾	RPD7R<3:0> ⁽²⁾	1101 = Reserved
			1110 = Reserved
			1111 = REFCLKO1
RPD9	RPD9R	RPD9R<3:0>	0000 = No Connect
RPG6	RPG6R	RPG6R<3:0>	0001 = U3RTS
RPB8	RPB8R	RPB8R<3:0>	0010 = U4TX
RPB15	RPB15R	RPB15R<3:0>	0011 = Reserved
RPD4	RPD4R	RPD4R<3:0>	0100 = U6TX
RPB0	RPB0R	RPB0R<3:0>	0101 = SS1
RPE3	RPE3R	RPE3R<3:0>	0110 = Reserved
RPB7	RPB7R	RPB7R<3:0>	0111 = SS3
RPF12 ⁽¹⁾	RPF12R ⁽¹⁾	RPF12R<3:0> ⁽¹⁾	1000 = SS4
RPD12 ⁽¹⁾	RPD12R ⁽¹⁾	RPD12R<3:0> ⁽¹⁾	1001 = SS5 ⁽¹⁾
RPF8 ⁽¹⁾	RPF8R ⁽¹⁾	RPF8R<3:0> ⁽¹⁾	1010 = SDO6 ⁽¹⁾
RPC3 ⁽¹⁾	RPC3R ⁽¹⁾	RPC3R<3:0> ⁽¹⁾	1011 = OC5
RPE9 ⁽¹⁾	RPE9R ⁽¹⁾	RPE9R<3:0> ⁽¹⁾	1100 = OC8
			1101 = Reserved
			1110 = C1OUT
			1111 = REFCLKO3

Note 1: This selection is not available on 64-pin devices.

2: This selection is not available on 64-pin or 100-pin devices.

3: This selection is not available on devices without a CAN module.

TABLE 12-22: PERIPHERAL PIN SELECT INPUT REGISTER MAP

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
1404	INT1R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	INT1R<3:0>				0000
1408	INT2R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	INT2R<3:0>				0000
140C	INT3R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	INT3R<3:0>				0000
1410	INT4R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	INT4R<3:0>				0000
1418	T2CKR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	T2CKR<3:0>				0000
141C	T3CKR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	T3CKR<3:0>				0000
1420	T4CKR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	T4CKR<3:0>				0000
1424	T5CKR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	T5CKR<3:0>				0000
1428	T6CKR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	T6CKR<3:0>				0000
142C	T7CKR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	T7CKR<3:0>				0000
1430	T8CKR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	T8CKR<3:0>				0000
1434	T9CKR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	T9CKR<3:0>				0000
1438	IC1R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	IC1R<3:0>				0000
143C	IC2R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	IC2R<3:0>				0000
1440	IC3R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	IC3R<3:0>				0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

- Note** 1: This register is not available on 64-pin devices.
 2: This register is not available on devices without a CAN module.

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

REGISTER 15-5: DMTCNT: DEADMAN TIMER COUNT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	COUNTER<31:24>							
23:16	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	COUNTER<23:16>							
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	COUNTER<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	COUNTER<7:0>							

Legend:

R = Readable bit

-n = Value at POR

W = Writable bit

'1' = Bit is set

U = Unimplemented bit, read as '0'

'0' = Bit is cleared

x = Bit is unknown

bit 31-8 **COUNTER<31:0>**: Read current contents of DMT counter

REGISTER 15-6: DMTPSCNT: POST STATUS CONFIGURE DMT COUNT STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	PSCNT<31:24>							
23:16	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	PSCNT<23:16>							
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	PSCNT<15:8>							
7:0	R-0	R-0	R-0	R-y	R-y	R-y	R-y	R-y
	PSCNT<7:0>							

Legend:

R = Readable bit

-n = Value at POR

W = Writable bit

'1' = Bit is set

y = Value set from Configuration bits on POR

U = Unimplemented bit, read as '0'

'0' = Bit is cleared

x = Bit is unknown

bit 31-8 **PSCNT<31:0>**: DMT Instruction Count Value Configuration Status bits
This is always the value of the DMTCNT<4:0> bits in the DEVCFG1 Configuration register.

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

REGISTER 26-9: CEHDLEN: CRYPTO ENGINE HEADER LENGTH REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	HDRLEN<7:0>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7-0 **HDRLEN<7:0>:** DMA Header Length bits

For every packet, skip this length of locations and start filling the data.

REGISTER 26-10: CETRLLEN: CRYPTO ENGINE TRAILER LENGTH REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	TRLRLLEN<7:0>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7-0 **TRLRLLEN<7:0>:** DMA Trailer Length bits

For every packet, skip this length of locations at the end of the current packet and start putting the next packet.

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

REGISTER 28-7: ADCIMCON3: ADC INPUT MODE CONTROL REGISTER 3 (CONTINUED)

bit 16	SIGN40: AN40 Signed Data Mode bit ⁽²⁾ 1 = AN40 is using Signed Data mode 0 = AN40 is using Unsigned Data mode
bit 15	DIFF39: AN39 Mode bit ⁽²⁾ 1 = AN39 is using Differential mode 0 = AN39 is using Single-ended mode
bit 14	SIGN39: AN39 Signed Data Mode bit ⁽²⁾ 1 = AN39 is using Signed Data mode 0 = AN39 is using Unsigned Data mode
bit 13	DIFF38: AN38 Mode bit ⁽²⁾ 1 = AN38 is using Differential mode 0 = AN38 is using Single-ended mode
bit 12	SIGN38: AN38 Signed Data Mode bit ⁽²⁾ 1 = AN38 is using Signed Data mode 0 = AN38 is using Unsigned Data mode
bit 11	DIFF37: AN37 Mode bit ⁽²⁾ 1 = AN37 is using Differential mode 0 = AN37 is using Single-ended mode
bit 10	SIGN37: AN37 Signed Data Mode bit ⁽²⁾ 1 = AN37 is using Signed Data mode 0 = AN37 is using Unsigned Data mode
bit 9	DIFF36: AN36 Mode bit ⁽²⁾ 1 = AN36 is using Differential mode 0 = AN36 is using Single-ended mode
bit 8	SIGN36: AN36 Signed Data Mode bit ⁽²⁾ 1 = AN36 is using Signed Data mode 0 = AN36 is using Unsigned Data mode
bit 7	DIFF35: AN35 Mode bit ⁽²⁾ 1 = AN35 is using Differential mode 0 = AN35 is using Single-ended mode
bit 6	SIGN35: AN35 Signed Data Mode bit ⁽²⁾ 1 = AN35 is using Signed Data mode 0 = AN35 is using Unsigned Data mode
bit 5	DIFF34: AN34 Mode bit ⁽¹⁾ 1 = AN34 is using Differential mode 0 = AN34 is using Single-ended mode
bit 4	SIGN34: AN34 Signed Data Mode bit ⁽¹⁾ 1 = AN34 is using Signed Data mode 0 = AN34 is using Unsigned Data mode
bit 3	DIFF33: AN33 Mode bit ⁽¹⁾ 1 = AN33 is using Differential mode 0 = AN33 is using Single-ended mode
bit 2	SIGN33: AN33 Signed Data Mode bit ⁽¹⁾ 1 = AN33 is using Signed Data mode 0 = AN33 is using Unsigned Data mode

Note 1: This bit is not available on 64-pin devices.

2: This bit is not available on 64-pin and 100-pin devices.

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

REGISTER 28-24: ADCBASE: ADC BASE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ADCBASE<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ADCBASE<7:0>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-0 **Unimplemented:** Read as '0'

bit 15-0 **ADCBASE<15:0>:** ADC ISR Base Address bits

This register, when read, contains the base address of the user's ADC ISR jump table. The interrupt vector address is determined by the IRQVS<2:0> bits of the ADCCON1 register specifying the amount of left shift done to the ARDYx status bits in the ADCDSTAT1 and ADCDSTAT2 registers, prior to adding with ADCBASE register.

Interrupt Vector Address = Read Value of ADCBASE and Read Value of ADCBASE = Value written to ADCBASE + x << IRQVS<2:0>, where 'x' is the smallest active analog input ID from the ADCDSTAT1 or ADCDSTAT2 registers (which has highest priority).

REGISTER 29-10: C_iFLTCON0: CAN FILTER CONTROL REGISTER 0 (CONTINUED)

bit 15	FLTEN1: Filter 1 Enable bit 1 = Filter is enabled 0 = Filter is disabled
bit 14-13	MSEL1<1:0>: Filter 1 Mask Select bits 11 = Acceptance Mask 3 selected 10 = Acceptance Mask 2 selected 01 = Acceptance Mask 1 selected 00 = Acceptance Mask 0 selected
bit 12-8	FSEL1<4:0>: FIFO Selection bits 11111 = Message matching filter is stored in FIFO buffer 31 11110 = Message matching filter is stored in FIFO buffer 30 • • • 00001 = Message matching filter is stored in FIFO buffer 1 00000 = Message matching filter is stored in FIFO buffer 0
bit 7	FLTEN0: Filter 0 Enable bit 1 = Filter is enabled 0 = Filter is disabled
bit 6-5	MSEL0<1:0>: Filter 0 Mask Select bits 11 = Acceptance Mask 3 selected 10 = Acceptance Mask 2 selected 01 = Acceptance Mask 1 selected 00 = Acceptance Mask 0 selected
bit 4-0	FSEL0<4:0>: FIFO Selection bits 11111 = Message matching filter is stored in FIFO buffer 31 11110 = Message matching filter is stored in FIFO buffer 30 • • • 00001 = Message matching filter is stored in FIFO buffer 1 00000 = Message matching filter is stored in FIFO buffer 0

Note: The bits in this register can only be modified if the corresponding filter enable (FLTEN_n) bit is '0'.

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TABLE 37-23: I/O TIMING REQUIREMENTS (CONTINUED)

AC CHARACTERISTICS		Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended					
Param. No.	Symbol	Characteristics ⁽²⁾	Min.	Typ. ⁽¹⁾	Max.	Units	Conditions
DO32	TioF	Port Output Fall Time I/O Pins: 4x Source Driver Pins - RA3, RA9, RA10, RA14, RA15 RB0-RB2, RB4, RB6-RB7, RB11, RB13 RC12-RC15 RD0, RD6-RD7, RD11, RD14 RE8, RE9 RF2, RF3, RF8 RG15 RH0, RH1, RH4-RH6, RH8-RH13 RJ0-RJ2, RJ8, RJ9, RJ11	—	—	9.5	ns	CLOAD = 50 pF
			—	—	6	ns	CLOAD = 20 pF
		Port Output Fall Time I/O Pins: 8x Source Driver Pins - RA0-RA2, RA4, RA5 RB3, RB5, RB8-RB10, RB12, RB14, RB15 RC1-RC4 RD1-RD5, RD9, RD10, RD12, RD13, RD15 RE4-RE7 RF0, RF4, RF5, RF12, RF13 RG0, RG1, RG6-RG9 RH2, RH3, RH7, RH14, RH15 RJ3-RJ7, RJ10, RJ12-RJ15 RK0-RK7	—	—	8	ns	CLOAD = 50 pF
			—	—	6	ns	CLOAD = 20 pF
		Port Output Fall Time I/O Pins: 12x Source Driver Pins - RA6, RA7 RE0-RE3 RF1 RG12-RG14	—	—	3.5	ns	CLOAD = 50 pF
			—	—	2	ns	CLOAD = 20 pF
DI35	TINP	INTx Pin High or Low Time	5	—	—	ns	—
DI40	TRBP	CNx High or Low Time (input)	5	—	—	ns	—

Note 1: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

Note 2: This parameter is characterized, but not tested in manufacturing.

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

TABLE 37-38: ADC MODULE SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	Symbol	Characteristics	Min.	Typ.	Max.	Units	Conditions
Device Supply							
AD01	AVDD	Module VDD Supply	Greater of VDD – 0.3 or 2.1	—	Lesser of VDD + 0.3 or 3.6	V	—
AD02	AVSS	Module Vss Supply	VSS	—	VSS + 0.3	V	—
Reference Inputs							
AD05	VREFH	Reference Voltage High	VREFL + 1.8	—	AVDD	V	(Note 1)
AD06	VREFL	Reference Voltage Low	AVSS	—	VREFH – 1.8	V	(Note 1)
AD07	VREF	Absolute Reference Voltage (VREFH – VREFL)	1.8	—	AVDD	V	(Note 2)
AD08	IREF	Current Drain	—	102	—	μA	Per ADCx ('x' = 0-4, 7)
Analog Input							
AD12	VINH-VINL	Full-Scale Input Span	VREFL	—	VREFH	V	—
AD13	VINL	Absolute VINL Input Voltage	AVSS	—	VREFL	V	—
AD14	VINH	Absolute VINH Input Voltage	AVSS	—	VREFH	V	—
ADC Accuracy – Measurements with External VREF+/VREF-							
AD20c	Nr	Resolution	6	—	12	bits	Selectable 6, 8, 10, 12 Resolution Ranges
AD21c	INL	Integral Nonlinearity	—	±3	—	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.3V
AD22c	DNL	Differential Nonlinearity	—	±1	—	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.3V
AD23c	GERR	Gain Error	—	±8	—	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.3V
AD24c	EOFF	Offset Error	—	±2	—	LSb	VINL = AVSS = 0V, AVDD = 3.3V
Dynamic Performance							
AD31b	SINAD	Signal to Noise and Distortion	—	67	—	dB	Single-ended (Notes 2,3)
AD34b	ENOB	Effective Number of bits	—	10.5	—	bits	(Notes 2,3)

Note 1: These parameters are not characterized or tested in manufacturing.

2: These parameters are characterized, but not tested in manufacturing.

3: Characterized with a 1 kHz sine wave.

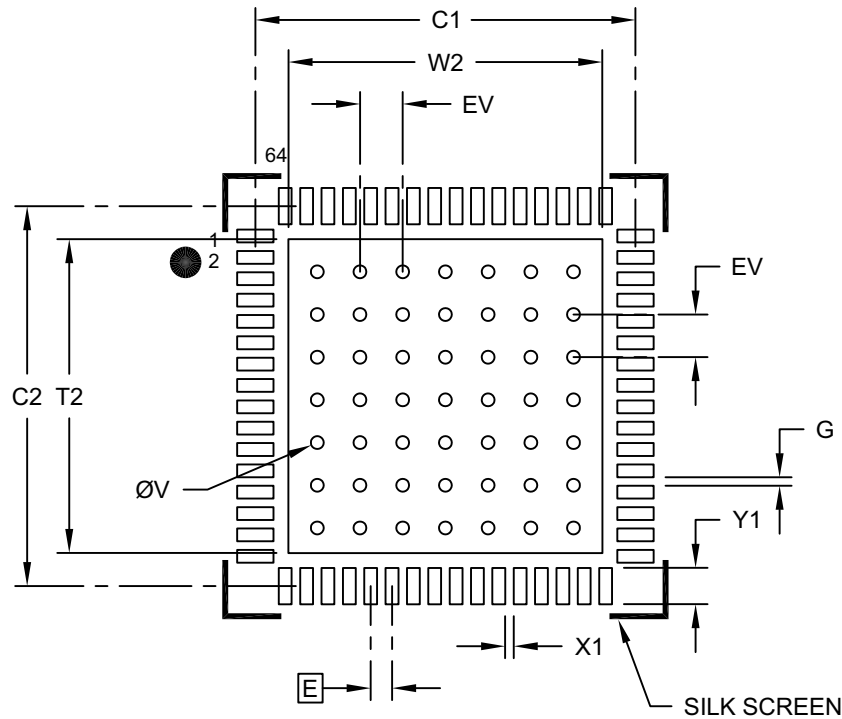
4: The ADC module is functional at VBORMIN < VDD < VDDMIN, but with degraded performance. Unless otherwise stated, module functionality is guaranteed, but not characterized.

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

41.2 Package Details

64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body [QFN]
With 0.40 mm Contact Length and 7.70x7.70mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Optional Center Pad Width	W2			7.50
Optional Center Pad Length	T2			7.50
Contact Pad Spacing	C1		8.90	
Contact Pad Spacing	C2		8.90	
Contact Pad Width (X20)	X1			0.30
Contact Pad Length (X20)	Y1			0.90
Contact Pad to Center Pad (X20)	G	0.20		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

- Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
- For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing No. C04-2213B