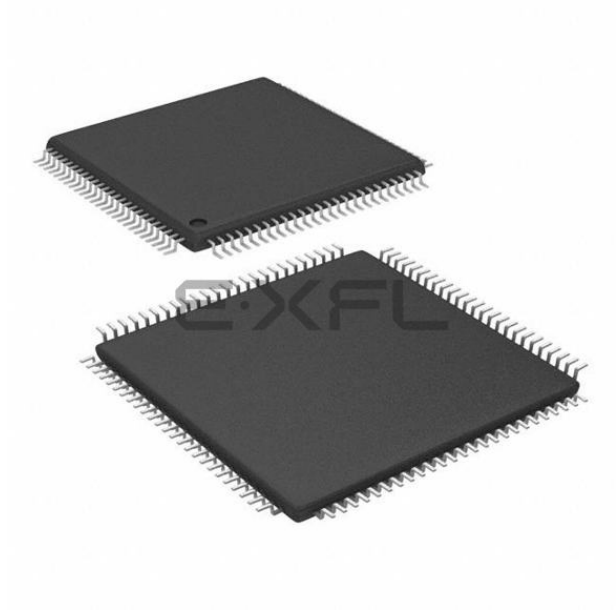
Microchip Technology - PIC32MZ2048EFH100-250I/PF Datasheet



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Applications of "Embedded - Microcontrollers"

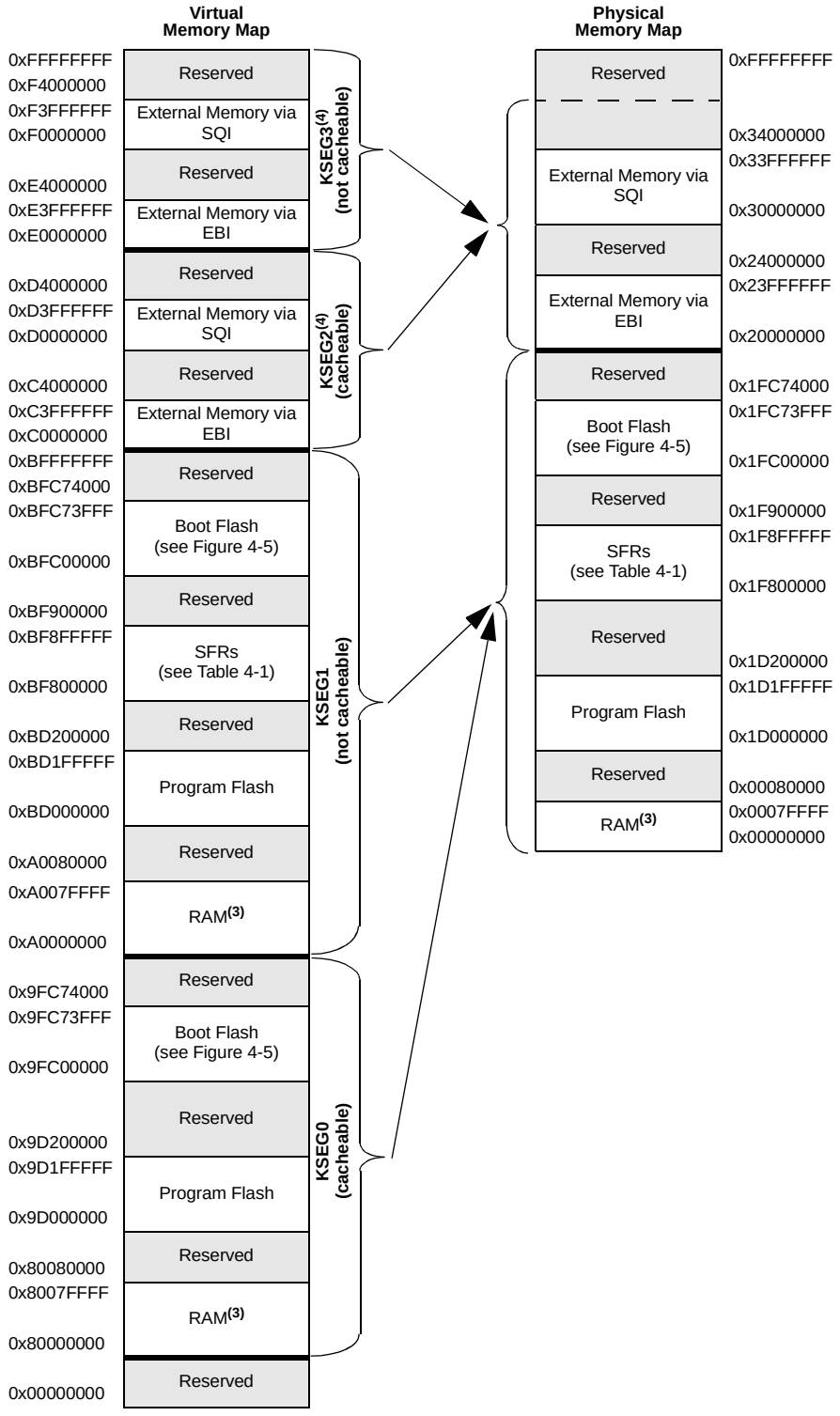
Details	
Product Status	Active
Core Processor	MIPS32® M-Class
Core Size	32-Bit Single-Core
Speed	250MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, PMP, SPI, SQI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	78
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	2.1V ~ 3.6V
Data Converters	A/D 40x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mz2048efh100-250i-pf

TABLE 1-6: PORTA THROUGH PORTK PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number				Pin Type	Buffer Type	Description
	64-pin QFN/ TQFP	100-pin TQFP	124-pin VTLA	144-pin TQFP/ LQFP			
PORTG							
RG0	—	88	B50	128	I/O	ST	PORTG is a bidirectional I/O port
RG1	—	87	A60	127	I/O	ST	
RG6	4	10	B6	14	I/O	ST	
RG7	5	11	A8	15	I/O	ST	
RG8	6	12	B7	16	I/O	ST	
RG9	10	16	B9	21	I/O	ST	
RG12	—	96	A65	140	I/O	ST	
RG13	—	97	B55	141	I/O	ST	
RG14	—	95	B54	139	I/O	ST	
RG15	—	1	A2	1	I/O	ST	
PORTH							
RH0	—	—	B17	43	I/O	ST	PORTH is a bidirectional I/O port
RH1	—	—	A22	44	I/O	ST	
RH2	—	—	—	45	I/O	ST	
RH3	—	—	—	46	I/O	ST	
RH4	—	—	A30	65	I/O	ST	
RH5	—	—	B26	66	I/O	ST	
RH6	—	—	A31	67	I/O	ST	
RH7	—	—	—	68	I/O	ST	
RH8	—	—	B32	81	I/O	ST	
RH9	—	—	A40	82	I/O	ST	
RH10	—	—	B33	83	I/O	ST	
RH11	—	—	—	84	I/O	ST	
RH12	—	—	A47	100	I/O	ST	
RH13	—	—	B40	101	I/O	ST	
RH14	—	—	—	102	I/O	ST	
RH15	—	—	—	103	I/O	ST	
PORTJ							
RJ0	—	—	B44	114	I/O	ST	PORTJ is a bidirectional I/O port
RJ1	—	—	A55	115	I/O	ST	
RJ2	—	—	B45	116	I/O	ST	
RJ3	—	—	—	117	I/O	ST	
RJ4	—	—	A62	131	I/O	ST	
RJ5	—	—	—	132	I/O	ST	
RJ6	—	—	—	133	I/O	ST	
RJ7	—	—	—	134	I/O	ST	
RJ8	—	—	A5	7	I/O	ST	
RJ9	—	—	B4	8	I/O	ST	
RJ10	—	—	—	10	I/O	ST	
RJ11	—	—	B12	27	I/O	ST	
RJ12	—	—	—	9	I/O	ST	
RJ13	—	—	—	28	I/O	ST	
RJ14	—	—	—	29	I/O	ST	
RJ15	—	—	—	30	I/O	ST	

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

FIGURE 4-4: MEMORY MAP FOR DEVICES WITH 2048 KB OF PROGRAM MEMORY(1,2)



Note 1: Memory areas are not shown to scale.

2: The Cache, MMU, and TLB are initialized by compiler start-up code.

3: RAM memory is divided into two equal banks: RAM Bank 1 and RAM Bank 2 on a half boundary.

4: The MMU must be enabled and the TLB must be set up to access this segment.

REGISTER 4-9: SBTxRDy: SYSTEM BUS TARGET 'x' REGION 'y' READ PERMISSIONS REGISTER ('x' = 0-13; 'y' = 0-8)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	R/W-0	R/W-1	R/W-1	R/W-1
	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared

bit 31-4 **Unimplemented:** Read as '0'

bit 3 **Group3:** Group3 Read Permissions bits
- 1 = Privilege Group 3 has read permission
- 0 = Privilege Group 3 does not have read permission

bit 2 **Group2:** Group2 Read Permissions bits
- 1 = Privilege Group 2 has read permission
- 0 = Privilege Group 2 does not have read permission

bit 1 **Group1:** Group1 Read Permissions bits
- 1 = Privilege Group 1 has read permission
- 0 = Privilege Group 1 does not have read permission

bit 0 **Group0:** Group0 Read Permissions bits
- 1 = Privilege Group 0 has read permission
- 0 = Privilege Group 0 does not have read permission

Note 1: Refer to Table 4-6 for the list of available targets and their descriptions.

2: For some target regions, certain bits in this register are read-only with preset values. See Table 4-6 for more information.

9.0 PREFETCH MODULE

Note: This data sheet summarizes the features of the PIC32MZ EF family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 41. "Prefetch Module for Devices with L1 CPU Cache"** (DS60001183) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

The Prefetch module is a performance enhancing module that is included in the PIC32MZ EF family of devices. When running at high-clock rates, Wait states must be inserted into Program Flash Memory (PFM) read transactions to meet the access time of the PFM. Wait states can be hidden to the core by prefetching and storing instructions in a temporary holding area that the CPU can access quickly. Although the data path to the CPU is 32 bits wide, the data path to the PFM is 128 bits wide. This wide data path provides the same bandwidth to the CPU as a 32-bit path running at four times the frequency.

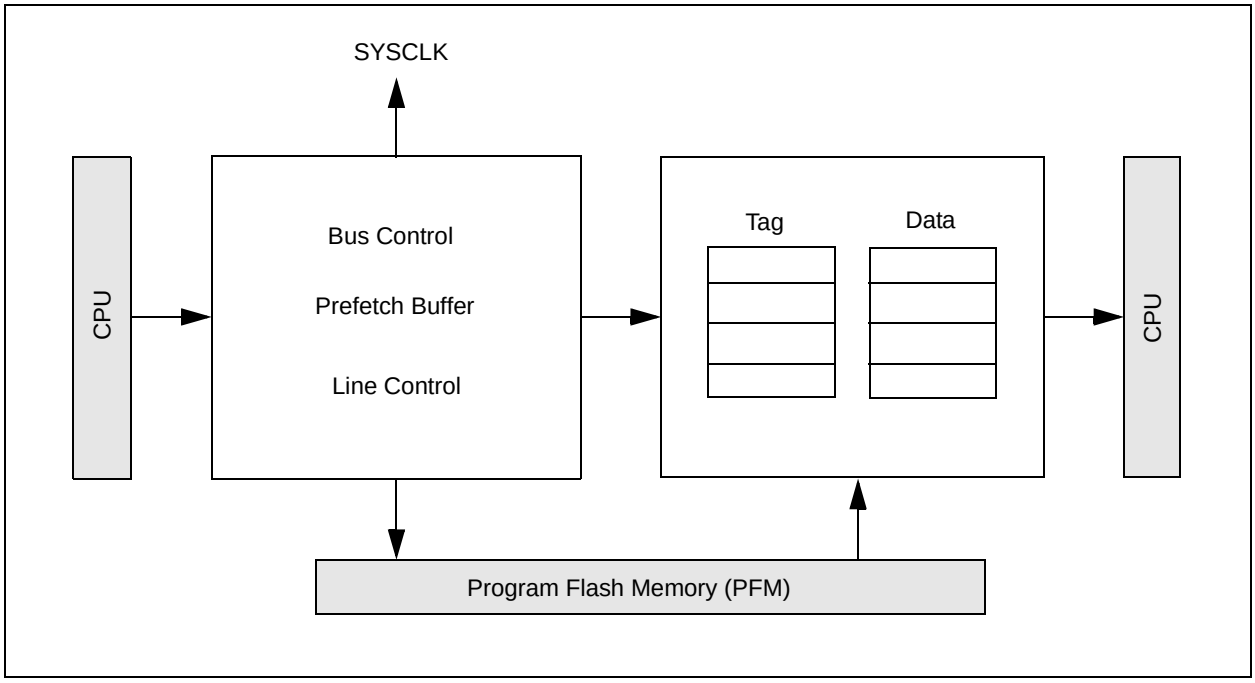
The Prefetch module holds a subset of PFM in temporary holding spaces known as lines. Each line contains a tag and data field. Normally, the lines hold a copy of what is currently in memory to make instructions or data available to the CPU without Flash Wait states.

The following are key features of the Prefetch module:

- 4x16 byte fully-associative lines
- One line for CPU instructions
- One line for CPU data
- Two lines for peripheral data
- 16-byte parallel memory fetch
- Configurable predictive prefetch
- Error detection and correction

A simplified block diagram of the Prefetch module is shown in Figure 9-1.

FIGURE 9-1: PREFETCH MODULE BLOCK DIAGRAM



REGISTER 11-8: USBIENCSR0: USB INDEXED ENDPOINT CONTROL STATUS REGISTER 0 (ENDPOINT 1-7)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	AUTOSET	ISO	MODE	DMAREQEN	FRCDATTG	DMAREQMD	—	—
		—					DATAWEN	DATATGGL
23:16	R/W-0, HS	R/W-0, HC	R/W-0, HS	R/W-0	R/W-0	R/W-0, HS	R/W-0	R/W-0, HC
	INCOMPTX	CLRDT	SENTSTALL	SENDSTALL	FLUSH	UNDERRUN	FIFONE	TXPKTRDY
	NAKTMOUT		RXSTALL	SETUPPKT		ERROR		
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	MULT<4:0>					TXMAXP<10:8>		
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	TXMAXP<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **AUTOSET:** Auto Set Control bit

1 = TXPKTRDY will be automatically set when data of the maximum packet size (value in TXMAXP) is loaded into the TX FIFO. If a packet of less than the maximum packet size is loaded, then TXPKTRDY will have to be set manually.
0 = TXPKTRDY must be set manually for all packet sizes

bit 30 **ISO:** Isochronous TX Endpoint Enable bit (Device mode)

1 = Enables the endpoint for Isochronous transfers
0 = Disables the endpoint for Isochronous transfers and enables it for Bulk or Interrupt transfers.
This bit only has an effect in Device mode. In Host mode, it always returns zero.

bit 29 **MODE:** Endpoint Direction Control bit

1 = Endpoint is TX
0 = Endpoint is RX

This bit only has any effect where the same endpoint FIFO is used for both TX and RX transactions.

bit 28 **DMAREQEN:** Endpoint DMA Request Enable bit

1 = DMA requests are enabled for this endpoint
0 = DMA requests are disabled for this endpoint

bit 27 **FRCDATTG:** Force Endpoint Data Toggle Control bit

1 = Forces the endpoint data toggle to switch and the data packet to be cleared from the FIFO, regardless of whether an ACK was received.
0 = No forced behavior

bit 26 **DMAREQMD:** Endpoint DMA Request Mode Control bit

1 = DMA Request Mode 1
0 = DMA Request Mode 0

This bit must not be cleared either before or in the same cycle as the above DMAREQEN bit is cleared.

bit 25 **DATAWEN:** Data Toggle Write Enable bit (Host mode)

1 = Enable the current state of the TX Endpoint data toggle (DATATGGL) to be written
0 = Disables writing the DATATGGL bit

bit 24 **DATATGGL:** Data Toggle Control bit (Host mode)

When read, this bit indicates the current state of the TX Endpoint data toggle. If DATAWEN = 1, this bit may be written with the required setting of the data toggle. If DATAWEN = 0, any value written to this bit is ignored.

REGISTER 11-16: USBINFO: USB INFORMATION REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0
	VPLEN<7:0>							
23:16	R/W-0	R/W-1	R/W-0	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0
	WTCON<3:0>				WTID<3:0>			
15:8	R-1	R-0	R-0	R-0	R-1	R-1	R-0	R-0
	DMACHANS<3:0>				RAMBITS<3:0>			
7:0	R-0	R-1	R-1	R-1	R-0	R-1	R-1	R-1
	RXENDPTS<3:0>				TXENDPTS<3:0>			

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-24 **VPLEN<7:0>:** VBUS pulsing charge length bits

Sets the duration of the VBUS pulsing charge in units of 546.1 µs. (The default setting corresponds to 32.77 ms.)

bit 23-20 **WTCON<3:0>:** Connect/Disconnect filter control bits

Sets the wait to be applied to allow for the connect/disconnect filter in units of 533.3 ns. The default setting corresponds to 2.667 µs.

bit 19-6 **WTID<3:0>:** ID delay valid control bits

Sets the delay to be applied from IDPULLUP being asserted to IDDIG being considered valid in units of 4.369ms. The default setting corresponds to 52.43ms.

bit 15-12 **DMACHANS<3:0>:** DMA Channels bits

These read-only bits provide the number of DMA channels in the USB module. For the PIC32MZ EF family, this number is 8.

bit 11-8 **RAMBITS<3:0>:** RAM address bus width bits

These read-only bits provide the width of the RAM address bus. For the PIC32MZ EF family, this number is 12.

bit 7-4 **RXENDPTS<3:0>:** Included RX Endpoints bits

This read-only register gives the number of RX endpoints in the design. For the PIC32MZ EF family, this number is 7.

bit 3-0 **TXENDPTS<3:0>:** Included TX Endpoints bits

These read-only bits provide the number of TX endpoints in the design. For the PIC32MZ EF family, this number is 7.

REGISTER 14-1: TxCON: TYPE B TIMER CONTROL REGISTER ('x' = 2-9)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
	ON(1)	—	SIDL(2)	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	U-0
	TGATE(1)	TCKPS<2:0>(1)			T32(3)	—	TCS(1)	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Timer On bit(1)
- 1 = Module is enabled
- 0 = Module is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit(2)
- 1 = Discontinue operation when device enters Idle mode
- 0 = Continue operation even in Idle mode

bit 12-8 **Unimplemented:** Read as '0'

bit 7 **TGATE:** Timer Gated Time Accumulation Enable bit(1)

When TCS = 1:
This bit is ignored and is read as '0'.

When TCS = 0:
- 1 = Gated time accumulation is enabled
- 0 = Gated time accumulation is disabled

bit 6-4 **TCKPS<2:0>:** Timer Input Clock Prescale Select bits(1)
- 111 = 1:256 prescale value
- 110 = 1:64 prescale value
- 101 = 1:32 prescale value
- 100 = 1:16 prescale value
- 011 = 1:8 prescale value
- 010 = 1:4 prescale value
- 001 = 1:2 prescale value
- 000 = 1:1 prescale value

bit 3 **T32:** 32-Bit Timer Mode Select bit(3)
- 1 = Odd numbered and even numbered timers form a 32-bit timer
- 0 = Odd numbered and even numbered timers form separate 16-bit timers

Note 1: While operating in 32-bit mode, this bit has no effect for odd numbered timers (Timer1, Timer3, Timer5, Timer7, and Timer9). All timer functions are set through the even numbered timers.

2: While operating in 32-bit mode, this bit must be cleared on odd numbered timers to enable the 32-bit timer in Idle mode.

3: This bit is available only on even numbered timers (Timer2, Timer4, Timer6, and Timer8).

18.0 OUTPUT COMPARE

Note: This data sheet summarizes the features of the PIC32MZ EF family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 16. "Output Compare"** (DS60001111) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

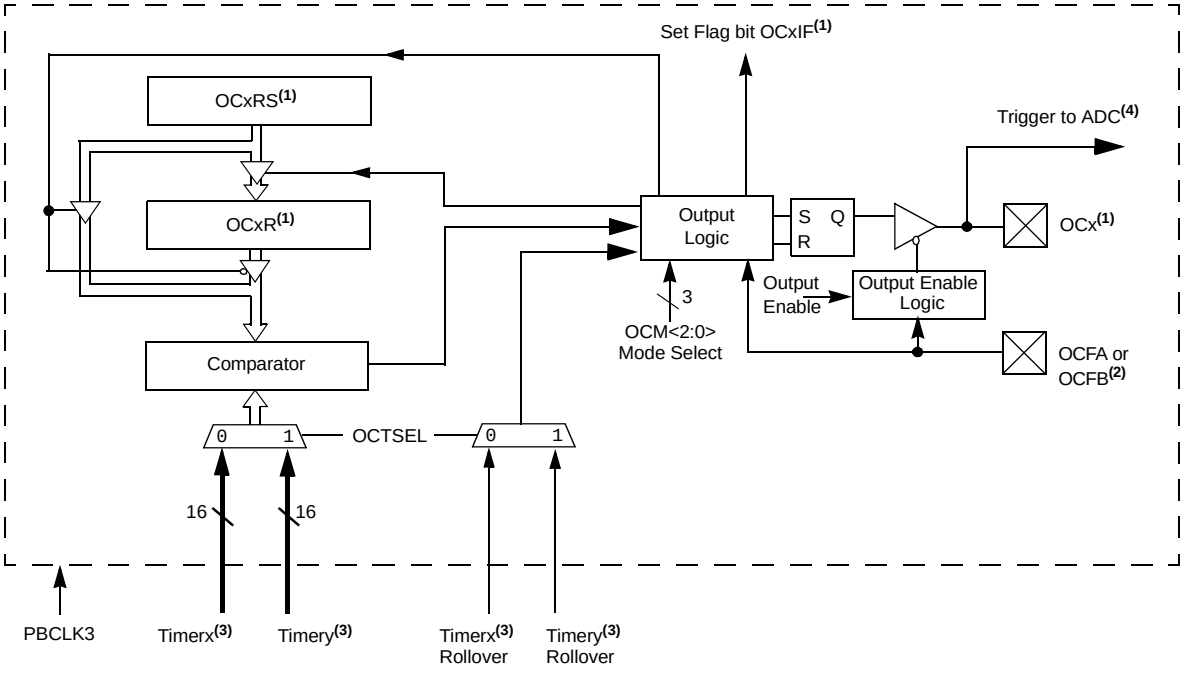
The Output Compare module is used to generate a single pulse or a train of pulses in response to selected time base events.

For all modes of operation, the Output Compare module compares the values stored in the OCxR and/or the OCxRS registers to the value in the selected timer. When a match occurs, the Output Compare module generates an event based on the selected mode of operation.

The following are key features of the Output Compare module:

- Multiple Output Compare modules in a device
- Programmable interrupt generation on compare event
- Single and Dual Compare modes
- Single and continuous output pulse generation
- Pulse-Width Modulation (PWM) mode
- Hardware-based PWM Fault detection and automatic output disable
- Programmable selection of 16-bit or 32-bit time bases
- Can operate from either of two available 16-bit time bases or a single 32-bit time base
- ADC event trigger

FIGURE 18-1: OUTPUT COMPARE MODULE BLOCK DIAGRAM



Note 1: Where 'x' is shown, reference is made to the registers associated with the respective output compare channels, 1 through 9.

2: The OCFA pin controls the OC1, OC3, and OC7-OC9 channels. The OCFB pin controls the OC4-OC6 channels.

3: Refer to Table 18-1 for Timerx and Timery selections.

4: The ADC event trigger is only available on OC1, OC3, and OC 5.

REGISTER 19-1: SPIxCON: SPI CONTROL REGISTER (CONTINUED)

bit 5 **MSTEN:** Master Mode Enable bit
1 = Master mode
0 = Slave mode

bit 4 **DISSDI:** Disable SDI bit(4)
1 = SDI pin is not used by the SPI module (pin is controlled by PORT function)
0 = SDI pin is controlled by the SPI module

bit 3-2 **STXISEL<1:0>:** SPI Transmit Buffer Empty Interrupt Mode bits
11 = Interrupt is generated when the buffer is not full (has one or more empty elements)
10 = Interrupt is generated when the buffer is empty by one-half or more
01 = Interrupt is generated when the buffer is completely empty
00 = Interrupt is generated when the last transfer is shifted out of SPISR and transmit operations are complete

bit 1-0 **SRXISEL<1:0>:** SPI Receive Buffer Full Interrupt Mode bits
11 = Interrupt is generated when the buffer is full
10 = Interrupt is generated when the buffer is full by one-half or more
01 = Interrupt is generated when the buffer is not empty
00 = Interrupt is generated when the last word in the receive buffer is read (i.e., buffer is empty)

Note 1: This bit can only be written when the ON bit = 0. Refer to **Section 37.0 "Electrical Characteristics"** for maximum clock frequency requirements.

2: This bit is not used in the Framed SPI mode. The user should program this bit to '0' for the Framed SPI mode (FRMEN = 1).

3: When AUDEN = 1, the SPI/I^2S module functions as if the CKP bit is equal to '1', regardless of the actual value of the CKP bit.

4: This bit present for legacy compatibility and is superseded by PPS functionality on these devices (see **Section 12.4 "Peripheral Pin Select (PPS)"** for more information).

REGISTER 24-4: EBIFTRPD: EXTERNAL BUS INTERFACE FLASH TIMING REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	TRPD<11:8>			
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	TRPD<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-12 **Unimplemented:** Read as '0'

bit 11-0 **TRPD<11:0>:** Flash Timing bits

These bits define the number of clock cycles to wait after resetting the external Flash memory before any read/write access.

REGISTER 25-1: RTCCON: REAL-TIME CLOCK AND CALENDAR CONTROL REGISTER (CONTINUED)

bit 10-9 **RTCCLKSEL<1:0>:** RTCC Clock Select bits

When a new value is written to these bits, the Seconds Value register should also be written to properly reset the clock prescalers in the RTCC.

11 = Reserved
10 = Reserved
01 = RTCC uses the external 32.768 kHz Secondary Oscillator (SOSC)
00 = RTCC uses the internal 32 kHz oscillator (LPRC)

bit 8-7 **RTCOUTSEL<1:0>:** RTCC Output Data Select bits(2)

11 = Reserved
10 = RTCC Clock is presented on the RTCC pin
01 = Seconds Clock is presented on the RTCC pin
00 = Alarm Pulse is presented on the RTCC pin when the alarm interrupt is triggered

bit 6 **RTCCLKON:** RTCC Clock Enable Status bit(5)

1 = RTCC Clock is actively running
0 = RTCC Clock is not running

bit 5-4 **Unimplemented:** Read as '0'

bit 3 **RTCWREN:** Real-Time Clock Value Registers Write Enable bit(3)

1 = Real-Time Clock Value registers can be written to by the user
0 = Real-Time Clock Value registers are locked out from being written to by the user

bit 2 **RTCSYNC:** Real-Time Clock Value Registers Read Synchronization bit

1 = Real-time clock value registers can change while reading (due to a rollover ripple that results in an invalid data read). If the register is read twice and results in the same data, the data can be assumed to be valid.
0 = Real-time clock value registers can be read without concern about a rollover ripple

bit 1 **HALFSEC:** Half-Second Status bit(4)

1 = Second half period of a second
0 = First half period of a second

bit 0 **RTCOE:** RTCC Output Enable bit

1 = RTCC output is enabled
0 = RTCC output is not enabled

Note 1: The ON bit is only writable when RTCWREN = 1.
2: Requires RTCOE = 1 (RTCCON<0>) for the output to be active.
3: The RTCWREN bit can be set only when the write sequence is enabled.
4: This bit is read-only. It is cleared to '0' on a write to the seconds bit fields (RTCTIME<14:8>).
5: This bit is undefined when RTCCLKSEL<1:0> = 00 (LPRC is the clock source).

Note:	This register is reset only on a Power-on Reset (POR).

TABLE 26-4: CRYPTO ENGINE SECURITY ASSOCIATION STRUCTURE (CONTINUED)

Name		Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
SA_ENCIV1	31:24	ENCIV<31:24>							
	23:16	ENCIV<23:16>							
	15:8	ENCIV<15:8>							
	7:0	ENCIV<7:0>							
SA_ENCIV2	31:24	ENCIV<31:24>							
	23:16	ENCIV<23:16>							
	15:8	ENCIV<15:8>							
	7:0	ENCIV<7:0>							
SA_ENCIV3	31:24	ENCIV<31:24>							
	23:16	ENCIV<23:16>							
	15:8	ENCIV<15:8>							
	7:0	ENCIV<7:0>							
SA_ENCIV4	31:24	ENCIV<31:24>							
	23:16	ENCIV<23:16>							
	15:8	ENCIV<15:8>							
	7:0	ENCIV<7:0>							

TABLE 34-3: DEVICE ID, REVISION, AND CONFIGURATION SUMMARY

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets(1)
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0000	CFGCON	31:16	—	—	—	—	—	—	DMAPRI	CPUPRI	—	—	—	—	—	—	ICACLK	OCACLK	0000
		15:0	—	—	IOLOCK	PMDLOCK	PGLOCK	—	—	USBSSEN	IOANCPEN	—	ECCCON<1:0>		JTAGEN	TROEN	—	TDOEN	000B
0020	DEVID	31:16	VER<3:0>				DEVID<27:16>												xxxx
		15:0	DEVID<15:0>																xxxx
0030	SYSKEY	31:16	SYSKEY<31:0>																0000
		15:0																	0000
00C0	CFGEBIA(2)	31:16	EBIPINEN	—	—	—	—	—	—	—	EBIA23EN	EBIA22EN	EBIA21EN	EBIA20EN	EBIA19EN	EBIA18EN	EBIA17EN	EBIA16EN	0000
		15:0	EBIA15EN	EBIA14EN	EBIA13EN	EBIA12EN	EBIA11EN	EBIA10EN	EBIA9EN	EBIA8EN	EBIA7EN	EBIA6EN	EBIA5EN	EBIA4EN	EBIA3EN	EBIA2EN	EBIA1EN	EBIA0EN	0000
00D0	CFGEBIC(2)	31:16	EBI RDYINV3	EBI RDYINV2	EBI RDYINV1	—	EBI RDYEN3	EBI RDYEN2	EBI RDYEN1	—	—	—	—	—	—	—	EBI RDYLVL	EBIRPEN	0000
		15:0	—	—	EBIWEEN	EBIOEEN	—	—	EBIBSEN1	EBIBSEN0	EBICSEN3	EBICSEN2	EBICSEN1	EBICSEN0	—	—	EBIDEN1	EBIDEN0	0000
00E0	CFGPG	31:16	ICD1PG<1:0>		—	—	—	—	CRYPTPG<1:0>		FCPG<1:0>		SQI1PG<1:0>		—	—	ETHPG<1:0>		0000
		15:0	CAN2PG<1:0>		CAN1PG<1:0>		—	—	USBPG<1:0>		—	—	DMAPG<1:0>		—	—	CPUPG<1:0>		0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.
Note 1: Reset values are dependent on the device variant.
2: This register is not available on 64-pin devices.

TABLE 34-4: DEVICE SERIAL NUMBER SUMMARY

Virtual Address (BFC5_#)	Register Name	Bit Range	Bits																All Resets(1)
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
4020	DEVSN0	31:16	Device Serial Number <31:16>																xxxx
		15:0	Device Serial Number <15:0>																xxxx
4024	DEVSN1	31:16	Device Serial Number <31:16>																xxxx
		15:0	Device Serial Number <15:0>																xxxx

Legend: x = unknown value on Reset.
Note 1: Reset values are dependent on the device variant.

36.2 MPLAB XC Compilers

The MPLAB XC Compilers are complete ANSI C compilers for all of Microchip's 8, 16, and 32-bit MCU and DSC devices. These compilers provide powerful integration capabilities, superior code optimization and ease of use. MPLAB XC Compilers run on Windows, Linux or MAC OS X.

For easy source level debugging, the compilers provide debug information that is optimized to the MPLAB X IDE.

The free MPLAB XC Compiler editions support all devices and commands, with no time or memory restrictions, and offer sufficient code optimization for most applications.

MPLAB XC Compilers include an assembler, linker and utilities. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. MPLAB XC Compiler uses the assembler to produce its object file. Notable features of the assembler include:

- Support for the entire device instruction set
- Support for fixed-point and floating-point data
- Command-line interface
- Rich directive set
- Flexible macro language
- MPLAB X IDE compatibility

36.3 MPASM Assembler

The MPASM Assembler is a full-featured, universal macro assembler for PIC10/12/16/18 MCUs.

The MPASM Assembler generates relocatable object files for the MPLINK Object Linker, Intel® standard HEX files, MAP files to detail memory usage and symbol reference, absolute LST files that contain source lines and generated machine code, and COFF files for debugging.

The MPASM Assembler features include:

- Integration into MPLAB X IDE projects
- User-defined macros to streamline assembly code
- Conditional assembly for multipurpose source files
- Directives that allow complete control over the assembly process

36.4 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK Object Linker combines relocatable objects created by the MPASM Assembler. It can link relocatable objects from precompiled libraries, using directives from a linker script.

The MPLIB Object Librarian manages the creation and modification of library files of precompiled code. When a routine from a library is called from a source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications.

The object linker/library features include:

- Efficient linking of single libraries instead of many smaller files
- Enhanced code maintainability by grouping related modules together
- Flexible creation of libraries with easy module listing, replacement, deletion and extraction

36.5 MPLAB Assembler, Linker and Librarian for Various Device Families

MPLAB Assembler produces relocatable machine code from symbolic assembly language for PIC24, PIC32 and dsPIC DSC devices. MPLAB XC Compiler uses the assembler to produce its object file. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. Notable features of the assembler include:

- Support for the entire device instruction set
- Support for fixed-point and floating-point data
- Command-line interface
- Rich directive set
- Flexible macro language
- MPLAB X IDE compatibility

TABLE 38-4: DC CHARACTERISTICS: POWER-DOWN CURRENT (I_{PD})

DC CHARACTERISTICS			Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ T_A ≤ +125°C for Extended		
Param. No.	**Typical(2)**	**Maximum(5)**	**Units**	**Conditions**	
Power-Down Current (I_{PD}) (Note 1)					
EDC40m	20	46	mA	+125ºC	Base Power-Down Current
Module Differential Current					
EDC41e	15	50	µA	3.6V	Watchdog Timer Current: ΔI_{WDT} **(Note 3)**
EDC42e	25	50	µA	3.6V	RTCC + Timer1 w/32 kHz Crystal: ΔI_{RTCC} **(Note 3)**
EDC43d	3	3.8	mA	3.6V	ADC: ΔI_{ADC} **(Notes 3, 4)**
EDC44	15	50	µA	3.6V	Deadman Timer Current: ΔI_{DMT} **(Note 3)**

Note 1: The test conditions for I_{PD} current measurements are as follows:

- Oscillator mode is EC (for 8 MHz and below) and EC+PLL (for above 8 MHz) with OSC1 driven by external square wave from rail-to-rail, (OSC1 input clock input over/undershoot < 100 mV required)
- OSC2/CLKO is configured as an I/O input pin
- USB PLL is disabled (USBMD = 1), V_{USB3V3} is connected to V_{SS}
- CPU is in Sleep mode
- L1 Cache and Prefetch modules are disabled
- No peripheral modules are operating, (ON bit = 0), and the associated PMD bit is set. All clocks are disabled ON bit (PBxDIV<15>) = 0 (x ≠ 1,7)
- WDT, DMT, Clock Switching, Fail-Safe Clock Monitor, and Secondary Oscillator are disabled
- All I/O pins are configured as inputs and pulled to V_{SS}
- $\overline{MCLR}$ = V_{DD}
- RTCC and JTAG are disabled
- Voltage regulator is in Stand-by mode (VREGS = 0)

2: Data in the "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

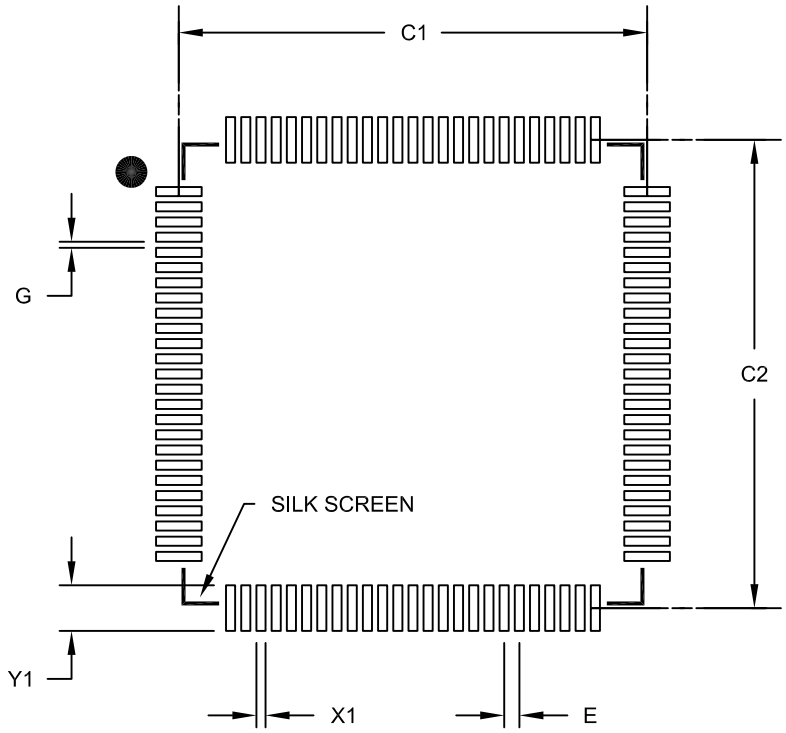
3: The Δ current is the additional current consumed when the module is enabled. This current should be added to the base I_{PD} current.

4: Voltage regulator is operational (VREGS = 1).

5: Data in the "Maximum" column is at 3.3V, +125ºC at specified operating frequency, unless otherwise stated. Parameters are for design guidance only and are not tested.

100-Lead Plastic Thin Quad Flatpack (PF) - 14x14x1 mm Body 2.00 mm Footprint [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Contact Pad Spacing	C1		15.40	
Contact Pad Spacing	C2		15.40	
Contact Pad Width (X100)	X1			0.30
Contact Pad Length (X100)	Y1			1.50
Distance Between Pads	G	0.20		

Notes:

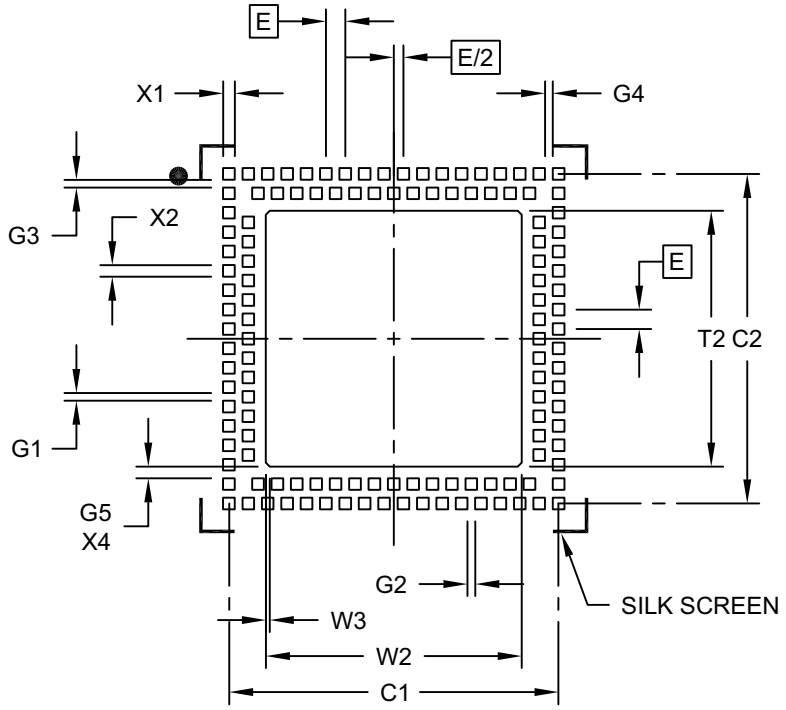
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2110B

124-Very Thin Leadless Array Package (TL) – 9x9x0.9 mm Body [VTLA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Pad Clearance	G1	0.20		
Pad Clearance	G2	0.20		
Pad Clearance	G3	0.20		
Pad Clearance	G4	0.20		
Contact to Center Pad Clearance (X4)	G5	0.30		
Optional Center Pad Width	T2			6.60
Optional Center Pad Length	W2			6.60
Optional Center Pad Chamfer (X4)	W3		0.10	
Contact Pad Spacing	C1		8.50	
Contact Pad Spacing	C2		8.50	
Contact Pad Width (X124)	X1			0.30
Contact Pad Length (X124)	X2			0.30

Notes:

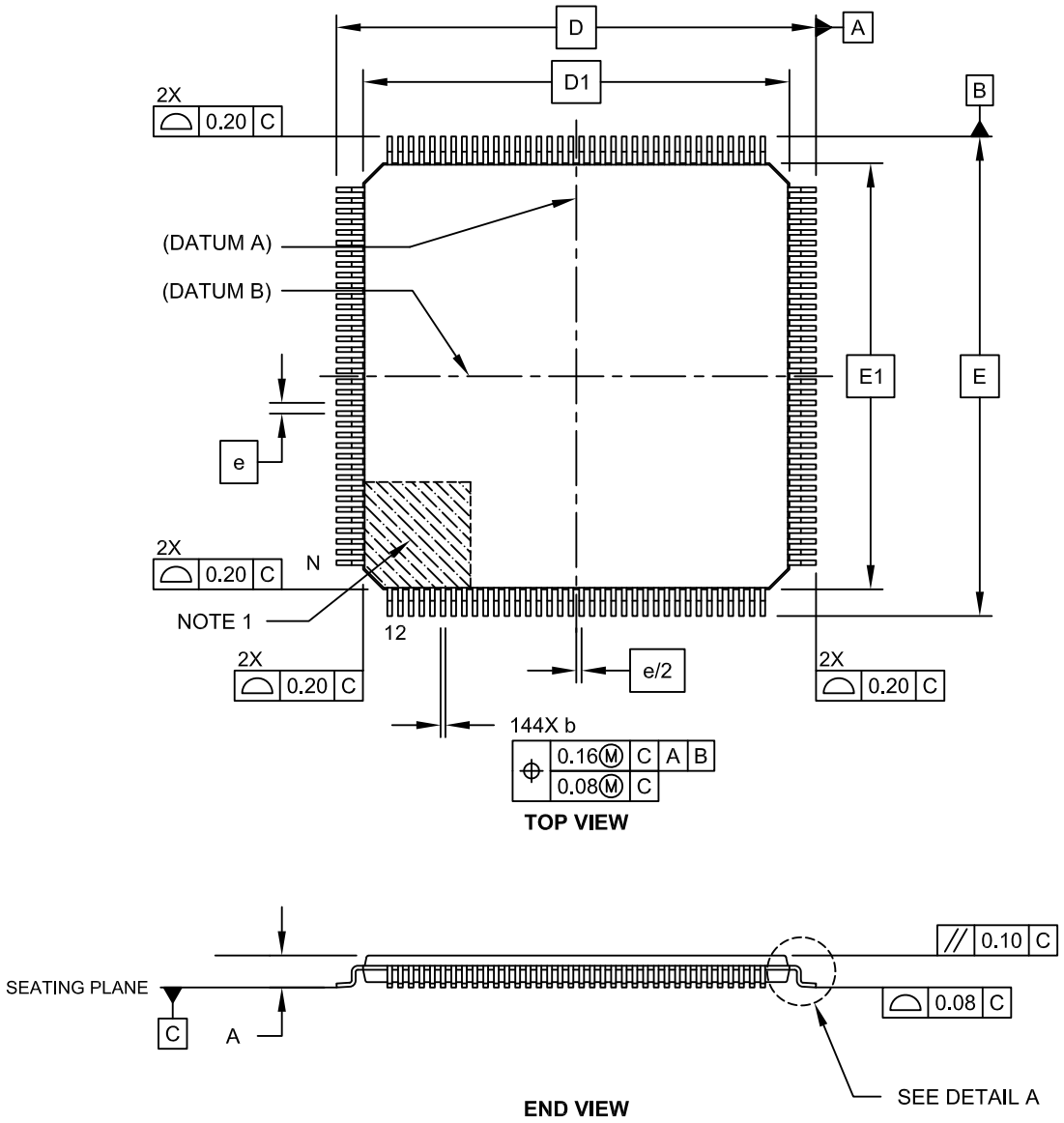
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2193A

144-Lead Plastic Thin Quad Flatpack (PH)-16x16x1mm Body, 2.00 mm Footprint [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-155B Sheet 1 of 2

A.4 Resets

The PIC32MZ EF family of devices has updated the resets modules to incorporate the new handling of NMI resets from the WDT, DMT, and the FSCM. In addition, some bits have been moved, as summarized in Table A-5.

TABLE A-5: RESET DIFFERENCES

PIC32MX5XX/6XX/7XX Feature	PIC32MZ EF Feature
Power Reset	
	The VREGS bit, which controls whether the internal regulator is enabled in Sleep mode, has been moved from RCON in PIC32MX5XX/6XX/7XX devices to a new PWRCON register in PIC32MZ EF devices.
VREGS (**RCON<8>**) 1 = Regulator is enabled and is on during Sleep mode 0 = Regulator is disabled and is off during Sleep mode	VREGS (**PWRCON<0>**) 1 = Voltage regulator will remain active during Sleep 0 = Voltage regulator will go to Stand-by mode during Sleep
Watchdog Timer Reset	
On PIC32MX devices, a WDT expiration immediately triggers a device reset.	On PIC32MZ EF devices, the WDT expiration now causes a NMI. The WDTO bit in RNMICON indicates that the WDT caused the NMI. A new timer, NMICNT, runs when the WDT NMI is triggered, and if it expires, the device is reset.
WDT expiration immediately causes a device reset.	**WDT expiration causes a NMI, which can then trigger the device reset.** **WDTO (RNMICON<24>)** **1 = WDT time-out has occurred and caused a NMI** **0 = WDT time-out has not occurred** **NMICNT<7:0> (RNMICON<7:0>)**

A.5 USB

The PIC32MZ EF family of devices has a new Hi-Speed USB module, which requires the updated USB stack from Microchip. In addition, the USB PLL was also updated. See **A.1 "Oscillator and PLL Configuration"** for more information and Table A-6 for a list of additional differences.

TABLE A-6: USB DIFFERENCES

PIC32MX5XX/6XX/7XX Feature	PIC32MZ EF Feature
Debug Mode	
On PIC32MX devices, when stopping on a breakpoint during debugging, the USB module can be configured to stop or continue execution from the Freeze Peripherals dialog in MPLAB X IDE.	On PIC32MZ EF devices, the USB module continues operating when stopping on a breakpoint during debugging.
VBUSON Pin	
PIC32MX devices feature a VBUSON pin for controlling the external transceiver power supply.	On PIC32MZ EF devices, the VBUSON pin is not available. A port pin can be used to achieve the same functionality.

TABLE A-9: FLASH PROGRAMMING DIFFERENCES (CONTINUED)

PIC32MX5XX/6XX/7XX Feature	PIC32MZ EF Feature
Flash Programming	
	The op codes for programming the Flash memory have been changed to accommodate the new quad-word programming and dual-panel features. The row size has changed to 2 KB (512 IW) from 128 IW. The page size has changed to 16 KB (4K IW) from 4 KB (1K IW). Note that the NVMOP register is now protected, and requires the WREN bit be set to enable modification.
NVMOP<3:0> (NVMCON<3:0>) 1111 = Reserved • • • **0111 = Reserved** **0110 = No operation** **0101 = Program Flash (PFM) erase operation** 0100 = Page erase operation 0011 = Row program operation **0010 = No operation** 0001 = Word program operation 0000 = No operation	NVMOP<3:0> (NVMCON<3:0>) 1111 = Reserved • • • 1000 = Reserved **0111 = Program erase operation** **0110 = Upper program Flash memory erase operation** **0101 = Lower program Flash memory erase operation** 0100 = Page erase operation 0011 = Row program operation **0010 = Quad Word (128-bit) program operation** 0001 = Word program operation 0000 = No operation
PIC32MX devices feature a single NVMDATA register for word programming. NVMDATA	On PIC32MZ EF devices, to support quad word programming, the NVMDATA register has been expanded to four words. NVMDATA**x**, where 'x' = 0 through 3
Flash Endurance and Retention	
PIC32MX devices support Flash endurance and retention of up to 20K E/W cycles and 20 years.	On PIC32MZ EF devices, ECC must be enabled to support the same endurance and retention as PIC32MX devices.
Configuration Words	
On PIC32MX devices, Configuration Words can be programmed with **Word or Row program** operation.	On PIC32MZ EF devices, all Configuration Words must be programmed with **Quad Word or Row Program** operations.
Configuration Words Reserved Bit	
On PIC32MX devices, the **DEVCFG0<15>** bit is Reserved and must be programmed to '0'.	On PIC32MZ EF devices, this bit is **DEVSIGN0<31>**.