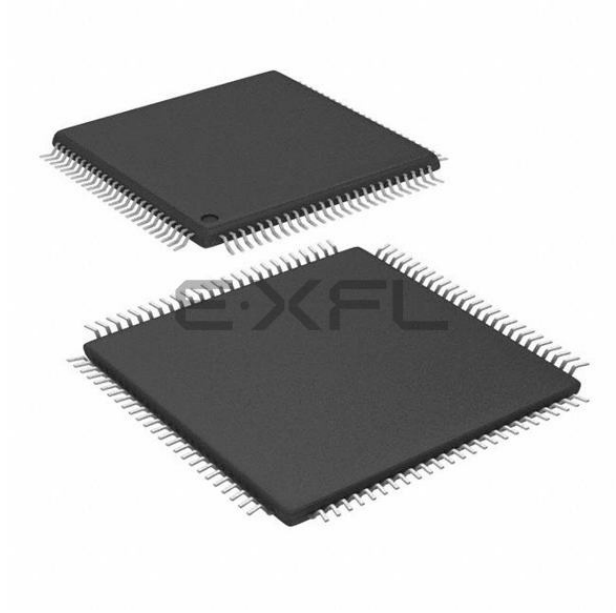
Microchip Technology - PIC32MZ2048EFH100-E/PT Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® M-Class
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, PMP, SPI, SQI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	78
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	2.1V ~ 3.6V
Data Converters	A/D 40x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mz2048efh100-e-pt

TABLE 5: PIN NAMES FOR 144-PIN DEVICES (CONTINUED)

144-PIN LQFP AND TQFP (TOP VIEW)

PIC32MZ0512EF(E/F/K)144
PIC32MZ1024EF(G/H/M)144
PIC32MZ1024EF(E/F/K)144
PIC32MZ2048EF(G/H/M)144

144

1

Pin Number	Full Pin Name	Pin Number	Full Pin Name
73	VBUS	109	RPD1/SCK1/RD1
74	VUSB3V3	110	EBID14/RPD2/PMD14/RD2
75	VSS	111	EBID15/RPD3/PMD15/RD3
76	D-	112	EBID12/RPD12/PMD12/RD12
77	D+	113	EBID13/PMD13/RD13
78	RPF3/USBID/RF3	114	ETXERR/RJ0
79	SDA3/RPF2/RF2	115	EMDIO/RJ1
80	SCL3/RPF8/RF8	116	EBIRDY3/RJ2
81	ERXD0/RH8	117	EBIA22/RJ3
82	ERXD3/RH9	118	$\overline{\text{SQICS0}}$/RPD4/RD4
83	ECOL/RH10	119	$\overline{\text{SQICS1}}$/RPD5/RD5
84	EBIRDY2/RH11	120	ETXEN/RPD6/RD6
85	SCL2/RA2	121	ETXCLK/RPD7/RD7
86	EBIRDY1/SDA2/RA3	122	VDD
87	EBIA14/PMCS1/PMA14/RA4	123	VSS
88	VDD	124	EBID11/RPF0/PMD11/RF0
89	VSS	125	EBID10/RPF1/PMD10/RF1
90	EBIA9/RPF4/SDA5/PMA9/RF4	126	EBIA21/RK7
91	EBIA8/RPF5/SCL5/PMA8/RF5	127	EBID9/RPG1/PMD9/RG1
92	EBIA18/RK4	128	EBID8/RPG0/PMD8/RG0
93	EBIA19/RK5	129	TRCLK/SQICLK/RA6
94	EBIA20/RK6	130	TRD3/SQID3/RA7
95	RPA14/SCL1/RA14	131	$\overline{\text{EBICS0}}$/RJ4
96	RPA15/SDA1/RA15	132	$\overline{\text{EBICS1}}$/RJ5
97	EBIA15/RPD9/PMCS2/PMA15/RD9	133	$\overline{\text{EBICS2}}$/RJ6
98	RPD10/SCK4/RD10	134	$\overline{\text{EBICS3}}$/RJ7
99	EMDC/RPD11/RD11	135	EBID0/PMD0/RE0
100	ECRS/RH12	136	VSS
101	ERXDV/ECRSDV/RH13	137	VDD
102	RH14	138	EBID1/PMD1/RE1
103	EBIA23/RH15	139	TRD2/SQID2/RG14
104	RPD0/RTCC/INT0/RD0	140	TRD1/SQID1/RG12
105	SOSCI/RPC13/RC13	141	TRD0/SQID0/RG13
106	SOSCO/RPC14/T1CK/RC14	142	EBID2/PMD2/RE2
107	VDD	143	EBID3/RPE3/PMD3/RE3
108	VSS	144	EBID4/AN18/PMD4/RE4

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and **Section 12.4 "Peripheral Pin Select (PPS)"** for restrictions.

2: Every I/O port pin (RAx-RKx) can be used as a change notification pin (CNAx-CNKx). See **Section 12.0 "I/O Ports"** for more information.

3: Shaded pins are 5V tolerant.

REGISTER 4-1: BFxSEQ3: BOOT FLASH 'x' SEQUENCE WORD 3 REGISTER ('x' = 1 AND 2)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/P	R/P	R/P	R/P	R/P	R/P	R/P	R/P
	CSEQ<15:8>							
23:16	R/P	R/P	R/P	R/P	R/P	R/P	R/P	R/P
	CSEQ<7:0>							
15:8	R/P	R/P	R/P	R/P	R/P	R/P	R/P	R/P
	TSEQ<15:8>							
7:0	R/P	R/P	R/P	R/P	R/P	R/P	R/P	R/P
	TSEQ<7:0>							

Legend:		P = Programmable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **CSEQ<15:0>:** Boot Flash Complement Sequence Number bits

bit 15-0 **TSEQ<15:0>:** Boot Flash True Sequence Number bits

Note: The BFxSEQ0, BFxSEQ1, and BFxSEQ2 registers are used for Quad Word programming operation when programming the BFxSEQ3 registers, and do not contain any valid information.

TABLE 7-1: MIPS32® M-CLASS MICROPROCESSOR CORE EXCEPTION TYPES (CONTINUED)

Exception Type (In Order of Priority)	Description	Branches to	Status Bits Set	Debug Bits Set	EXCCODE	XC32 Function Name
Instruction Validity Exceptions	An instruction could not be completed because it was not allowed to access the required resources (Coprocessor Unusable) or was illegal (Reserved Instruction). If both exceptions occur on the same instruction, the Coprocessor Unusable Exception takes priority over the Reserved Instruction Exception.	EBASE+0x180	EXL	—	0x0A or 0x0B	_general_exception_handler
Execute Exception	An instruction-based exception occurred: Integer overflow, trap, system call, breakpoint, floating point, or DSP ASE state disabled exception.	EBASE+0x180	EXL	—	0x08-0x0C	_general_exception_handler
Tr	Execution of a trap (when trap condition is true).	EBASE+0x180	EXL	—	0x0D	_general_exception_handler
DDBL/DDBS	EJTAG Data Address Break (address only) or EJTAG data value break on store (address + value).	0xBFC0_0480	—	DDBL or DDBS	—	—
WATCH	A reference to an address that is in one of the Watch registers (data).	EBASE+0x180	EXL	—	0x17	_general_exception_handler
AdEL	Load address alignment error. User mode load reference to kernel address.	EBASE+0x180	EXL	—	0x04	_general_exception_handler
AdES	Store address alignment error. User mode store to kernel address.	EBASE+0x180	EXL	—	0x05	_general_exception_handler
TLBL	Load TLB miss or load TLB hit to page with V = 0.	EBASE+0x180	EXL	—	0x02	_general_exception_handler
TLBS	Store TLB miss or store TLB hit to page with V = 0.	EBASE+0x180	EXL	—	0x03	_general_exception_handler
DBE	Load or store bus error.	EBASE+0x180	EXL	—	0x07	_general_exception_handler
DDBL	EJTAG data hardware breakpoint matched in load data compare.	0xBFC0_0480	—	DDBL	—	—
CBrk	EJTAG complex breakpoint.	0xBFC0_0480	—	DIBIMPR, DDBLIMPR, and/or DDBSIMPR	—	—
Lowest Priority						

TABLE 10-3: DMA CHANNEL 0 THROUGH CHANNEL 7 REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
1390	DCH4SSA	31:16	CHSSA<31:0>																0000
		15:0																	0000
13A0	DCH4DSA	31:16	CHDSA<31:0>																0000
		15:0																	0000
13B0	DCH4SSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSSIZ<15:0>																0000
13C0	DCH4DSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDSIZ<15:0>																0000
13D0	DCH4SPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSPTR<15:0>																0000
13E0	DCH4DPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDPTR<15:0>																0000
13F0	DCH4CSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCSIZ<15:0>																0000
1400	DCH4CPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCPTR<15:0>																0000
1410	DCH4DAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHPDAT<15:0>																0000
1420	DCH5CON	31:16	CHPIGN<7:0>								—	—	—	—	—	—	—	—	0000
		15:0	CHBUSY	—	CHPIGNEN	—	CHPATLEN	—	—	CHCHNS	CHEN	CHAED	CHCHN	CHAEN	—	CHEDET	CHPRI<1:0>		0000
1430	DCH5ECON	31:16	—	—	—	—	—	—	—	—	CHAIRQ<7:0>								00FF
		15:0	CHSIRQ<7:0>								CFORCE	CABORT	PATEN	SIRQEN	AIRQEN	—	—	—	FF00
1440	DCH5INT	31:16	—	—	—	—	—	—	—	—	CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE	CHERIE	0000
		15:0	—	—	—	—	—	—	—	—	CHSDIF	CHSHIF	CHDDIF	CHDHIF	CHBCIF	CHCCIF	CHTAIF	CHERIF	0000
1450	DCH5SSA	31:16	CHSSA<31:0>																0000
		15:0																	0000
1460	DCH5DSA	31:16	CHDSA<31:0>																0000
		15:0																	0000
1470	DCH5SSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSSIZ<15:0>																0000
1480	DCH5DSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDSIZ<15:0>																0000
1490	DCH5SPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSPTR<15:0>																0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 "CLR, SET, and INV Registers"** for more information.

REGISTER 11-1: USBCSR0: USB CONTROL STATUS REGISTER 0 (CONTINUED)

bit 10 **RESUME:** Resume from Suspend control bit
1 = Generate Resume signaling when the device is in Suspend mode
0 = Stop Resume signaling

In *Device mode*, the software should clear this bit after 10 ms (a maximum of 15 ms) to end Resume signaling. In *Host mode*, the software should clear this bit after 20 ms.

bit 9 **SUSPMODE:** Suspend Mode status bit
1 = The USB module is in Suspend mode
0 = The USB module is in Normal operations

This bit is read-only in Device mode. In Host mode, it can be set by software, and is cleared by hardware.

bit 8 **SUSPEN:** Suspend Mode Enable bit
1 = Suspend mode is enabled
0 = Suspend mode is not enabled

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **FUNC<6:0>:** Device Function Address bits

These bits are only available in *Device mode*. This field is written with the address received through a SET_ADDRESS command, which will then be used for decoding the function address in subsequent token packets.

REGISTER 11-16: USBINFO: USB INFORMATION REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0
	VPLEN<7:0>							
23:16	R/W-0	R/W-1	R/W-0	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0
	WTCON<3:0>				WTID<3:0>			
15:8	R-1	R-0	R-0	R-0	R-1	R-1	R-0	R-0
	DMACHANS<3:0>				RAMBITS<3:0>			
7:0	R-0	R-1	R-1	R-1	R-0	R-1	R-1	R-1
	RXENDPTS<3:0>				TXENDPTS<3:0>			

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-24 **VPLEN<7:0>:** VBUS pulsing charge length bits

Sets the duration of the VBUS pulsing charge in units of 546.1 µs. (The default setting corresponds to 32.77 ms.)

bit 23-20 **WTCON<3:0>:** Connect/Disconnect filter control bits

Sets the wait to be applied to allow for the connect/disconnect filter in units of 533.3 ns. The default setting corresponds to 2.667 µs.

bit 19-6 **WTID<3:0>:** ID delay valid control bits

Sets the delay to be applied from IDPULLUP being asserted to IDDIG being considered valid in units of 4.369ms. The default setting corresponds to 52.43ms.

bit 15-12 **DMACHANS<3:0>:** DMA Channels bits

These read-only bits provide the number of DMA channels in the USB module. For the PIC32MZ EF family, this number is 8.

bit 11-8 **RAMBITS<3:0>:** RAM address bus width bits

These read-only bits provide the width of the RAM address bus. For the PIC32MZ EF family, this number is 12.

bit 7-4 **RXENDPTS<3:0>:** Included RX Endpoints bits

This read-only register gives the number of RX endpoints in the design. For the PIC32MZ EF family, this number is 7.

bit 3-0 **TXENDPTS<3:0>:** Included TX Endpoints bits

These read-only bits provide the number of TX endpoints in the design. For the PIC32MZ EF family, this number is 7.

TABLE 20-1: SERIAL QUADRATURE INTERFACE (SQI) REGISTER MAP (CONTINUED)

Virtual Address (BF8E_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
2044	SQI1BD STAT	31:16	—	—	—	—	—	—	—	—	—	—	BDSTATE<3:0>				DMA START	DMAACTV	0000
		15:0	BDCON<15:0>																0000
2048	SQI1BD POLLCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	POLLCON<15:0>																0000
204C	SQI1BD TXDSTAT	31:16	—	—	—	TXSTATE<3:0>				—	—	—	—	TXBUFCNT<4:0>					0000
		15:0	—	—	—	—	—	—	—	—	TXCURBUFLEN<7:0>								0000
2050	SQI1BD RXDSTAT	31:16	—	—	—	RXSTATE<3:0>				—	—	—	—	RXBUFCNT<4:0>					0000
		15:0	—	—	—	—	—	—	—	—	RXCURBUFLEN<7:0>								0000
2054	SQI1THR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	THRES<4:0>					0000
2058	SQI1INT SIGEN	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	DMAEISE	PKT DONEISE	BD DONEISE	CON THRISE	CON EMPTYISE	CON FULLISE	RX THRISE	RX FULLISE	RX EMPTYISE	TX THRISE	TX FULLISE	TX EMPTYISE	0000
205C	SQI1 TAPCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	CLKINDLY<5:0>						DATAOUTDLY<3:0>				CLKOUTDLY<3:0>				0000
2060	SQI1 MEMSTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	STATPOS	TYPESTAT<1:0>		STATBYTES<1:0>		0000
		15:0	STATDATA<15:0>																0000
2064	SQI1 XCON3	31:16	—	—	—	INIT1 SCHECK	INIT1COUNT<1:0>		INIT1TYPE<1:0>		INIT1CMD3<7:0>								0000
		15:0	INIT1CMD2<7:0>								INIT1CMD1<7:0>								0000
2068	SQI1 XCON4	31:16	—	—	—	INIT2 SCHECK	INIT2COUNT<1:0>		INIT2TYPE<1:0>		INIT2CMD3<7:0>								0000
		15:0	INIT2CMD2<7:0>								INIT2CMD1<7:0>								0000

REGISTER 20-26: SQI1XCON4: SQI XIP CONTROL REGISTER 4

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	INIT2SCHECK	INIT2COUNT<1:0>		INIT2TYPE<1:0>	
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	INIT2CMD3<7:0>(1)							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	INIT2CMD2<7:0>(1)							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	INIT2CMD1<7:0>(1)							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-29 **Unimplemented:** Read as '0'

bit 28 **INIT2SCHECK:** Flash Initialization 2 Command Status Check bit
1 = Check the status after executing the INIT2 command
0 = Do not check the status

bit 27-26 **INIT2COUNT<1:0>:** Flash Initialization 2 Command Count bits
11 = INIT2CMD1, INIT2CMD2, and INIT2CMD3 are sent
10 = INIT2CMD1 and INIT2CMD2 are sent, but INIT2CMD3 is still pending
01 = INIT2CMD1 is sent, but INIT2CMD2 and INIT2CMD3 are still pending
00 = No commands are sent

bit 25-24 **INIT2TYPE<1:0>:** Flash Initialization 2 Command Type bits
11 = Reserved
10 = INIT2 commands are sent in Quad Lane mode
01 = INIT2 commands are sent in Dual Lane mode
00 = INIT2 commands are sent in Single Lane mode

bit 24-16 **INIT2CMD3<7:0>:** Flash Initialization Command 3 bits(1)
Third command of the Flash initialization.

bit 15-8 **INIT2CMD2<7:0>:** Flash Initialization Command 2 bits(1)
Second command of the Flash initialization.

bit 7-0 **INIT2CMD1<7:0>:** Flash Initialization Command 1 bits(1)
First command of the Flash initialization.

Note 1: INIT2CMD1 can be WEN and INIT2CMD2 can be SECTOR UNPROTECT.

Note: Some Flash devices require Write Enable and Sector Unprotect commands before read/write operations and this register is useful in working with those Flash types (XIP mode only)

22.0 UNIVERSAL ASYNCHRONOUS RECEIVER TRANSMITTER (UART)

Note: This data sheet summarizes the features of the PIC32MZ EF family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 21. "Universal Asynchronous Receiver Transmitter (UART)"** (DS60001107) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

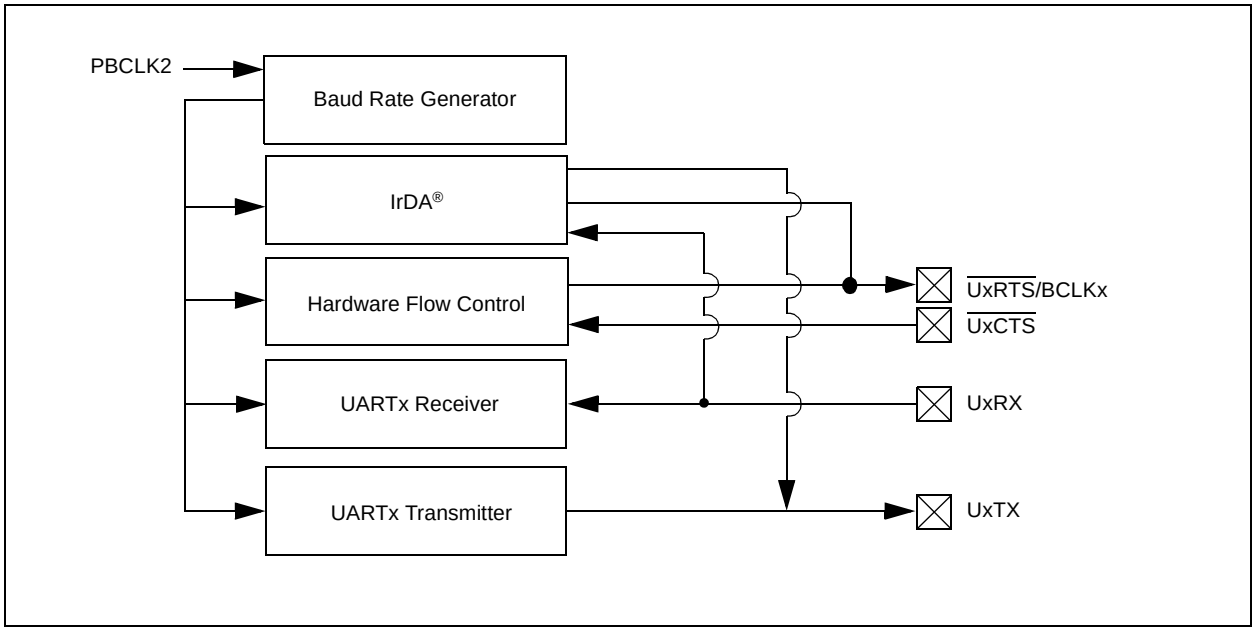
The UART module is one of the serial I/O modules available in the PIC32MZ EF family of devices. The UART is a full-duplex, asynchronous communication channel that communicates with peripheral devices and personal computers through protocols, such as RS-232, RS-485, LIN, and IrDA®. The module also supports the hardware flow control option, with $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$ pins, and also includes an IrDA encoder and decoder.

The primary features of the UART module are:

- Full-duplex, 8-bit or 9-bit data transmission
- Even, Odd or No Parity options (for 8-bit data)
- One or two Stop bits
- Hardware auto-baud feature
- Hardware flow control option
- Fully integrated Baud Rate Generator (BRG) with 16-bit prescaler
- Baud rates ranging from 76 bps to 25 Mbps at 100 MHz (PBCLK2)
- 8-level deep First-In-First-Out (FIFO) transmit data buffer
- 8-level deep FIFO receive data buffer
- Parity, framing and buffer overrun error detection
- Support for interrupt-only on address detect (9th bit = 1)
- Separate transmit and receive interrupts
- Loopback mode for diagnostic support
- LIN Protocol support
- IrDA encoder and decoder with 16x baud clock output for external IrDA encoder/decoder support

Figure 22-1 illustrates a simplified block diagram of the UART module.

FIGURE 22-1: UART SIMPLIFIED BLOCK DIAGRAM



REGISTER 22-1: UxMODE: UARTx MODE REGISTER (CONTINUED)

bit 5 **ABAUD:** Auto-Baud Enable bit
1 = Enable baud rate measurement on the next character – requires reception of Sync character (0x55); cleared by hardware upon completion
0 = Baud rate measurement is disabled or completed

bit 4 **RXINV:** Receive Polarity Inversion bit
1 = UxRX Idle state is '0'
0 = UxRX Idle state is '1'

bit 3 **BRGH:** High Baud Rate Enable bit
1 = High-Speed mode – 4x baud clock enabled
0 = Standard Speed mode – 16x baud clock enabled

bit 2-1 **PDSEL<1:0>:** Parity and Data Selection bits
11 = 9-bit data, no parity
10 = 8-bit data, odd parity
01 = 8-bit data, even parity
00 = 8-bit data, no parity

bit 0 **STSEL:** Stop Selection bit
1 = 2 Stop bits
0 = 1 Stop bit

Note 1: These bits are present for legacy compatibility, and are superseded by PPS functionality on these devices. For additional information, see **Section 12.4 "Peripheral Pin Select (PPS)"**.

25.0 REAL-TIME CLOCK AND CALENDAR (RTCC)

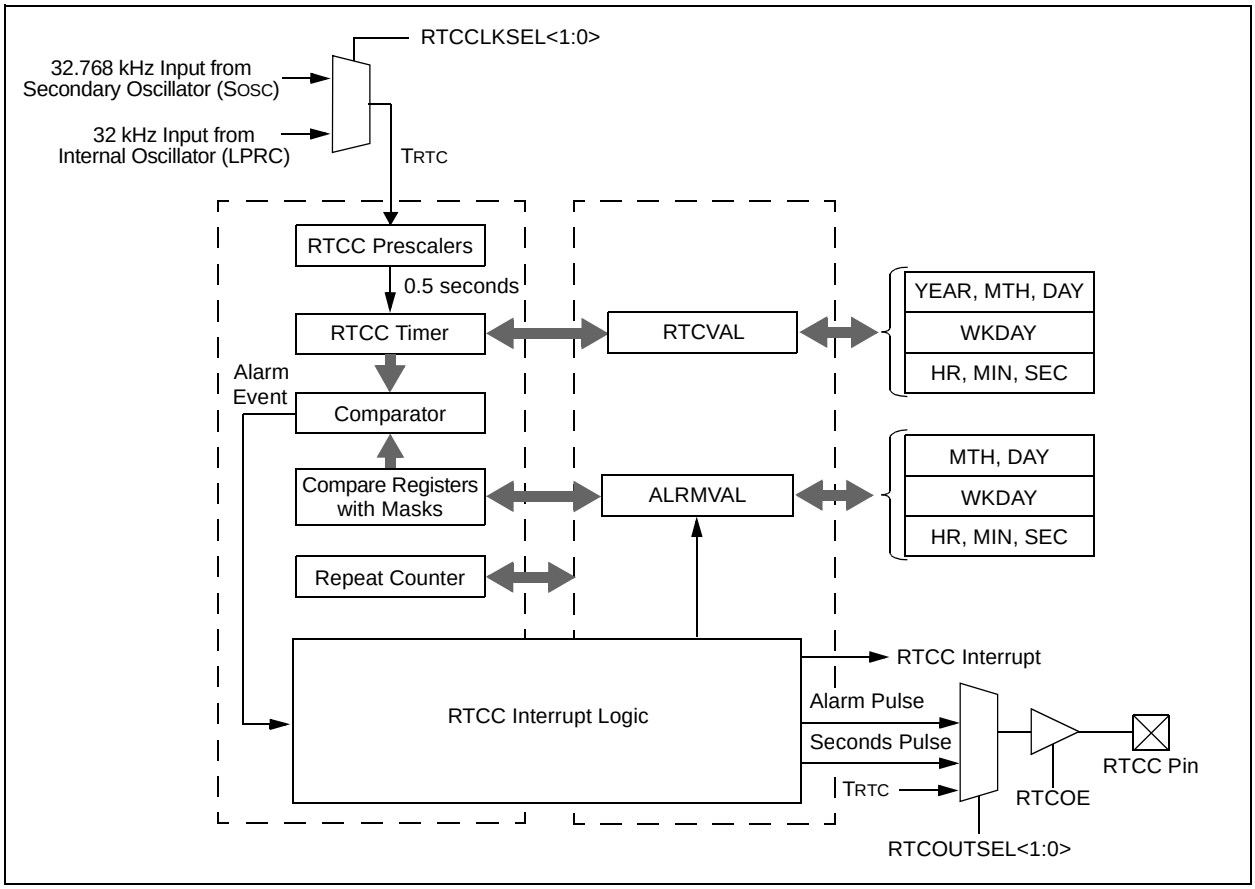
Note: This data sheet summarizes the features of the PIC32MZ EF family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 29. "Real-Time Clock and Calendar (RTCC)"** (DS60001125) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

The RTCC module is intended for applications in which accurate time must be maintained for extended periods of time with minimal or no CPU intervention. Low-power optimization provides extended battery lifetime while keeping track of time.

The following are key features of the RTCC module:

- Time: hours, minutes, and seconds
- 24-hour format (military time)
- Visibility of one-half second period
- Provides calendar: Weekday, date, month and year
- Alarm intervals are configurable for half of a second, one second, 10 seconds, one minute, 10 minutes, one hour, one day, one week, one month, and one year
- Alarm repeat with decrementing counter
- Alarm with indefinite repeat: Chime
- Year range: 2000 to 2099
- Leap year correction
- BCD format for smaller firmware overhead
- Optimized for long-term battery operation
- Fractional second synchronization
- User calibration of the clock crystal frequency with auto-adjust
- Calibration range: ±0.66 seconds error per month
- Calibrates up to 260 ppm of crystal error
- Uses external 32.768 kHz crystal or 32 kHz internal oscillator
- Alarm pulse, seconds clock, or internal clock output on RTCC pin

FIGURE 25-1: RTCC BLOCK DIAGRAM



26.1 Crypto Engine Control Registers

TABLE 26-2: CRYPTO ENGINE REGISTER MAP

Virtual Address (BF8E_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
5000	CEVER	31:16	REVISION<7:0>								VERSION<7:0>								0000
		15:0	ID<15:0>																0000
5004	CECON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	SWAPOEN	SWRST	SWAPEN	—	—	BDPCHST	BDPPLEN	DMAEN	0000
5008	CEBDADDR	31:16	BDPADDR<31:0>																0000
		15:0																	0000
500C	CEBDPADDR	31:16	BASEADDR<31:0>																0000
		15:0																	0000
5010	CESTAT	31:16	ERRMODE<2:0>			ERROP<2:0>			ERRPHASE<1:0>		—	—	BDSTATE<3:0>				START	ACTIVE	0000
		15:0	BDCTRL<15:0>																0000
5014	CEINTSRC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	AREIF	PKTIF	CBDIF	PENDIF	0000
5018	CEINTEN	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	AREIE	PKTIE	CBDIE	PENDIE	0000
501C	CEPOLLCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	BDPPLCON<15:0>																0000
5020	CEHDLEN	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	HDRLEN<7:0>								0000
5024	CETRLLEN	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	TRLRLEN<7:0>								0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

FIGURE 40-5: VOH – 12x DRIVER PINS

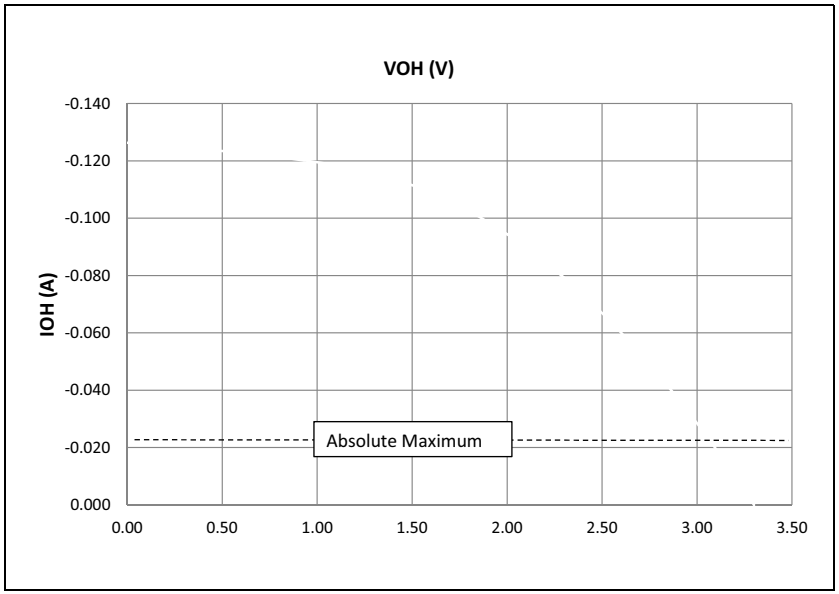


FIGURE 40-6: VOL – 12x DRIVER PINS

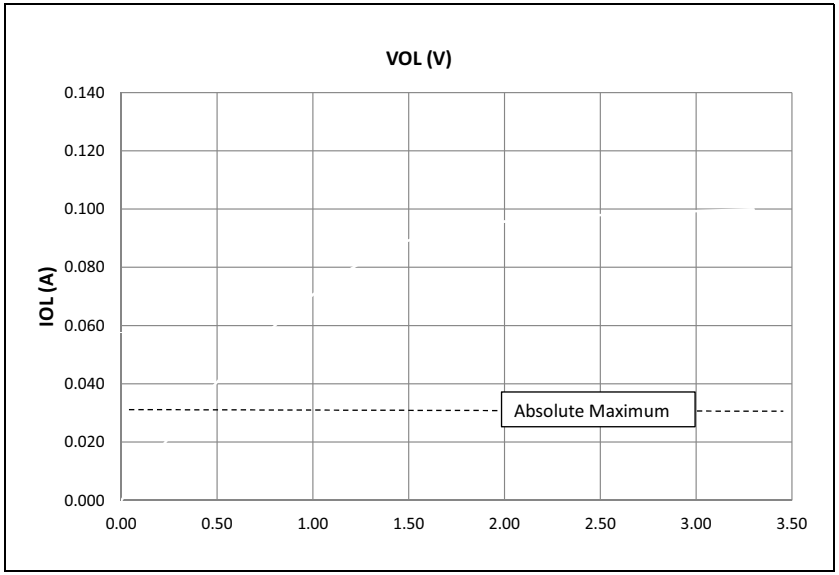
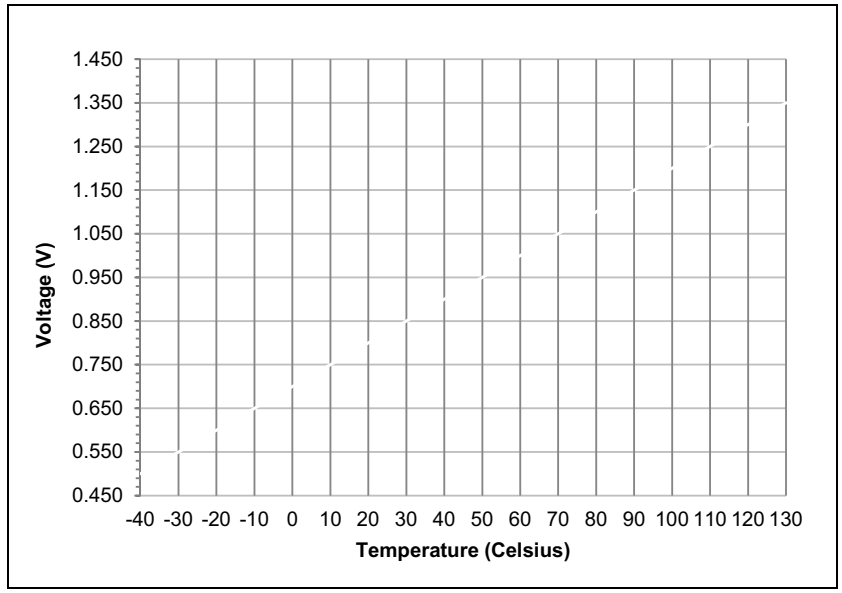


FIGURE 40-7: TYPICAL TEMPERATURE SENSOR VOLTAGE



A.4 Resets

The PIC32MZ EF family of devices has updated the resets modules to incorporate the new handling of NMI resets from the WDT, DMT, and the FSCM. In addition, some bits have been moved, as summarized in Table A-5.

TABLE A-5: RESET DIFFERENCES

PIC32MX5XX/6XX/7XX Feature	PIC32MZ EF Feature
Power Reset	
	The VREGS bit, which controls whether the internal regulator is enabled in Sleep mode, has been moved from RCON in PIC32MX5XX/6XX/7XX devices to a new PWRCON register in PIC32MZ EF devices.
VREGS (**RCON<8>**) 1 = Regulator is enabled and is on during Sleep mode 0 = Regulator is disabled and is off during Sleep mode	VREGS (**PWRCON<0>**) 1 = Voltage regulator will remain active during Sleep 0 = Voltage regulator will go to Stand-by mode during Sleep
Watchdog Timer Reset	
On PIC32MX devices, a WDT expiration immediately triggers a device reset.	On PIC32MZ EF devices, the WDT expiration now causes a NMI. The WDTO bit in RNMICON indicates that the WDT caused the NMI. A new timer, NMICNT, runs when the WDT NMI is triggered, and if it expires, the device is reset.
WDT expiration immediately causes a device reset.	**WDT expiration causes a NMI, which can then trigger the device reset.** **WDTO (RNMICON<24>)** **1 = WDT time-out has occurred and caused a NMI** **0 = WDT time-out has not occurred** **NMICNT<7:0> (RNMICON<7:0>)**

A.5 USB

The PIC32MZ EF family of devices has a new Hi-Speed USB module, which requires the updated USB stack from Microchip. In addition, the USB PLL was also updated. See **A.1 "Oscillator and PLL Configuration"** for more information and Table A-6 for a list of additional differences.

TABLE A-6: USB DIFFERENCES

PIC32MX5XX/6XX/7XX Feature	PIC32MZ EF Feature
Debug Mode	
On PIC32MX devices, when stopping on a breakpoint during debugging, the USB module can be configured to stop or continue execution from the Freeze Peripherals dialog in MPLAB X IDE.	On PIC32MZ EF devices, the USB module continues operating when stopping on a breakpoint during debugging.
VBUSON Pin	
PIC32MX devices feature a VBUSON pin for controlling the external transceiver power supply.	On PIC32MZ EF devices, the VBUSON pin is not available. A port pin can be used to achieve the same functionality.

TABLE A-10: PERIPHERAL DIFFERENCES (CONTINUED)

PIC32MX5XX/6XX/7XX Feature	PIC32MZ EF Feature
Ethernet	
	On PIC32MZ EF devices, the input clock divider for the Ethernet module has expanded options to accommodate the faster peripheral bus clock.
CLKSEL<3:0> (EMAC1MCFG<5:2>) 1000 = SYSCLK divided by 40 0111 = SYSCLK divided by 28 0110 = SYSCLK divided by 20 0101 = SYSCLK divided by 14 0100 = SYSCLK divided by 10 0011 = SYSCLK divided by 8 0010 = SYSCLK divided by 6 000x = SYSCLK divided by 4	CLKSEL<3:0> (EMAC1MCFG<5:2>) **1010 = PBCLK5 divided by 50** **1001 = PBCLK5 divided by 48** 1000 = PBCLK5 divided by 40 0111 = PBCLK5 divided by 28 0110 = PBCLK5 divided by 20 0101 = PBCLK5 divided by 14 0100 = PBCLK5 divided by 10 0011 = PBCLK5 divided by 8 0010 = PBCLK5 divided by 6 000x = PBCLK5 divided by 4
Comparator/Comparator Voltage Reference	
On PIC32MX devices, it was possible to select the VREF+ pin as the output to the CVREFOUT pin. VREFSEL (CVRCON<10>) 1 = CVREF = VREF+ 0 = CVREF is generated by the resistor network	On PIC32MZ EF devices, the CVREFOUT pin must come from the resistor network. This bit is not available.
On PIC32MX devices, the internal voltage reference (IVREF) could be chosen by the BGSEL<1:0> bits. BGSEL<1:0> (CVRCON<9:8>) 11 = IVREF = VREF+ 10 = Reserved 01 = IVREF = 0.6V (nominal, default) 00 = IVREF = 1.2V (nominal)	On PIC32MZ EF devices, IVREF is fixed and cannot be changed. These bits are not available.
Change Notification	
On PIC32MX devices, Change Notification is controlled by the **CNCON, CNEN, and CNPUE** registers.	On PIC32MZ EF devices, Change Notification functionality has been relocated into each I/O port and is controlled by the **CNPUx, CNPDx, CNCONx, CNENx, and CNSTATx** registers.
System Bus	
On PIC32MX devices, the System Bus registers can be used to configure RAM memory for data and program memory partitions, cacheability of Flash memory, and RAM Wait states. These registers are: **BMXCON, BMXDKPBA, BMXDUDBA, BMXDUPBA, BMXPUPBA, BMXDRMSZ, BMXPFMSZ, and BMXBOOTSZ.**	On PIC32MZ EF devices, a new System Bus is utilized that supports using RAM memory for program or data without the need for special configuration. Therefore, no special registers are associated with the System Bus to configure these features.
On PIC32MX devices, various arbitration modes are used as initiators on the System Bus. These modes can be selected by the **BMXARB<2:0> (BMXCON<2:0>)** bits.	On PIC32MZ EF devices, a new arbitration scheme has been implemented on the System Bus. All initiators use the Least Recently Serviced (LRS) scheme, with the exception of the DMA, CPU, and the Flash Controller. The Flash Controller always has High priority over LRS initiators. The DMA and CPU (when servicing an interrupt) can be selected to have LRS or High priority using the **DMAPRI (CFGCON<25>)** and **CPUPRI (CFGCON<24>)** bits.

B.6 Resets

On PIC32MZ EF devices, the Reset module adds eight bits to the NMICNT field to make the time-out period before device Reset longer, as described in Table B-5.

TABLE B-5: RESETS DIFFERENCES

PIC32MZ EC Feature	PIC32MZ EF Feature
Countdown to Reset During NMIs	
On PIC32MZ EC devices, the NMICNT<7:0> field is eight bits long, giving a maximum of 256 instructions before the device Reset.	On PIC32MZ EF devices, the NMICNT<15:0> field is now 16 bits long, giving a longer period of time (up to 65,536 instructions) prior to a device Reset.

B.7 USB

On PIC32MZ EF devices, a new USBCRCON register has been added to assist in controlling the reset of the USB module, and triggering interrupts based on VBUS voltage levels. This register also overcomes an errata on PIC32MZ EC devices that requires a three second start-up on the USB module.

B.8 I/O Ports

On PIC32MZ EF devices, many of the I/O pins now feature slew rate control bits to control how fast the pin makes a low-to-high or high-to-low transition. The Change Notification feature has also been enhanced to allow detection of level events in addition to edge detection. However, the SIDL bit is not present in the CNCONx registers on PIC32MZ EF devices, as it is on PIC32MZ EC devices.

B.9 Watchdog Timer

PIC32MZ EF devices use a new Watchdog Timer, although the overall control through the DEVCFGx words remains identical to that of PIC32MZ EC devices. Table B-6 lists two more changes, as well.

TABLE B-6: WATCHDOG TIMER DIFFERENCES

PIC32MZ EC Feature	PIC32MZ EF Feature
Watchdog Timer Postscaler	
On PIC32MZ EC devices, the SWDTPS<4:0> bits (WDTCON<6:2>) reflect the postscaler setting for the Watchdog Timer.	On PIC32MZ EF devices, the field has been changed to the RUNDIV<4:0> bits (WDTCON<12:8>).
Watchdog Windowed Mode	
On PIC32MZ EC devices, WDTWINEN is at bit position 1 (WDTCON<1>).	On PIC32MZ EF devices, WDTWINEN is now at bit position 0 (WDTCON<0>).

B.10 Serial Quad Interface (SQI)

On PIC32MZ EF devices, the SQI module has been updated with the following features:

- FIFOs can be reset through the CONFIFORST (SQI1CFG<19>), RXFIFORST (SQI1CFG<18>), and TXFIFORST (SQI1CFG<17>) bits in Register 20-3
- A new Flash Status check is available, which will allow the SQI to automatically query the status of the external device during write/erase operations without software intervention. See the SCHECK bit (SQI1CON<24>) and the SQI1MEMSTAT register (Register 20-4 and Register 20-24, respectively).
- The SQI clock divider bits have been expanded, and can use an undivided clock. See the CLKDIV<10:0> bits (SQI1CLKCON<18:8>) in Register 20-5.
- A new DMA Bus Error Interrupt is available through the DMAEIE (SQI1INTEN<11>), DMAEIF (SQI1INTSTAT<11>), and DMAEISE (SQI1INTSIGEN<11>) bits in Register 20-8, Register 20-9, and Register 20-22, respectively
- The SQI1STAT2 register (see Register 20-13) has two new fields:
  - CMDSTAT<1:0> (SQI1STAT2<17:16>) indicates the current command status
  - CONAVAIL<4:0> (SQI1STAT<11:8>) indicates how many spaces are available in the Control FIFO.
- The TAP Controller within the SQI can be configured for various timing requirements via the SQI1TAPCON register (Register 20-23)
- Two new XIP mode registers (SQI1XCON3 and SQI1XCON4) have been added for additional command sequencing (see Register 20-25 and Register 20-26, respectively)

Refer to **20.0 “Serial Quad Interface (SQI)”** and **Section 46. “Serial Quad Interface (SQI)”** (DS60001128) for more information.

B.11 PMP

On PIC32MZ EF devices, the PMP features the ability to buffer reads and writes in both directions, and can read and write from different addresses. Refer to **23.0 “Parallel Master Port (PMP)”** and **Section 43. “Parallel Master Port”** (DS60001346) for information.

NOTES:

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