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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	MIPS32® M-Class
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, PMP, SPI, SQI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	78
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	2.1V ~ 3.6V
Data Converters	A/D 40x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mz2048efh100t-i-pf

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

TABLE 5: PIN NAMES FOR 144-PIN DEVICES

144-PIN LQFP AND TQFP (TOP VIEW)		144	
PIC32MZ0512EF(E/F/K)144 PIC32MZ1024EF(G/H/M)144 PIC32MZ1024EF(E/F/K)144 PIC32MZ2048EF(G/H/M)144		1	
Pin Number	Full Pin Name	Pin Number	Full Pin Name
1	AN23/RG15	37	PGEC2/AN46/RPB6/RB6
2	EBIA5/AN34/PMA5/RA5	38	PGED2/AN47/RPB7/RB7
3	EBID5/AN17/RPE5/PMD5/RE5	39	VREF-/CVREF-/AN27/RA9
4	EBID6/AN16/PMD6/RE6	40	VREF+/CVREF+/AN28/RA10
5	EBID7/AN15/PMD7/RE7	41	AVDD
6	EBIA6/AN22/RPC1/PMA6/RC1	42	AVSS
7	AN35/ETXD0/RJ8	43	AN38/ETXD2/RH0
8	AN36/ETXD1/RJ9	44	AN39/ETXD3/RH1
9	EBIBS0/RJ12	45	EBIRP/RH2
10	EBIBS1/RJ10	46	RH3
11	EBIA12/AN21/RPC2/PMA12/RC2	47	EBIA10/AN48/RPB8/PMA10/RB8
12	EBIWE/AN20/RPC3/PMWR/RC3	48	EBIA7/AN49/RPB9/PMA7/RB9
13	EBIOE/AN19/RPC4/PMRD/RC4	49	CVREFOUT/AN5/RPB10/RB10
14	AN14/C1IND/RPG6/SCK2/RG6	50	AN6/RB11
15	AN13/C1INC/RPG7/SDA4/RG7	51	EBIA1/PMA1/RK1
16	AN12/C2IND/RPG8/SCL4/RG8	52	EBIA3/PMA3/RK2
17	VSS	53	EBIA17/RK3
18	VDD	54	VSS
19	EBIA16/RK0	55	VDD
20	MCLR	56	TCK/AN29/RA1
21	EBIA2/AN11/C2INC/RPG9/PMA2/RG9	57	TDI/AN30/RPF13/SCK5/RF13
22	TMS/AN24/RA0	58	TDO/AN31/RPF12/RF12
23	AN25/RPE8/RE8	59	AN7/RB12
24	AN26/RPE9/RE9	60	AN8/RB13
25	AN45/C1INA/RPB5/RB5	61	AN9/RPB14/SCK3/RB14
26	AN4/C1INB/RB4	62	AN10/RPB15/OCFB/RB15
27	AN37/ERXCLK/EREFCLK/RJ11	63	VSS
28	EBIA13/PMA13/RJ13	64	VDD
29	EBIA11/PMA11/RJ14	65	AN40/ERXERR/RH4
30	EBIA0/PMA0/RJ15	66	AN41/ERXD1/RH5
31	AN3/C2INA/RPB3/RB3	67	AN42/ERXD2/RH6
32	VSS	68	EBIA4/PMA4/RH7
33	VDD	69	AN32/RPD14/RD14
34	AN2/C2INB/RPB2/RB2	70	AN33/RPD15/SCK6/RD15
35	PGEC1/AN1/RPB1/RB1	71	OSC1/CLKI/RC12
36	PGED1/AN0/RPB0/RB0	72	OSC2/CLKO/RC15

- Note** 1: The RPN pins can be used by remappable peripherals. See Table 1 for the available peripherals and **Section 12.4 “Peripheral Pin Select (PPS)”** for restrictions.
- 2: Every I/O port pin (RAX-RKx) can be used as a change notification pin (CNAx-CNKx). See **Section 12.0 “I/O Ports”** for more information.
- 3: Shaded pins are 5V tolerant.

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

REGISTER 3-3: CONFIG3: CONFIGURATION REGISTER 3; CP0 REGISTER 16, SELECT 3

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	r-1	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	R-0	R-1	R-0	R-0	R-0	R-1	R/W-y
	—	IPLW<1:0>			MMAR<2:0>		MCU	ISAONEXC ⁽¹⁾
15:8	R-y	R-y	R-1	R-1	R-1	R-1	U-0	R-1
	ISA<1:0> ⁽¹⁾		ULRI	RXI	DSP2P	DSPP	—	ITL
7:0	U-0	R-1	R-1	R-0	R-1	U-0	U-0	R-0
	—	VEIC	VINT	SP	CDMM	—	—	TL

Legend:	r = Reserved bit	y = Value set from Configuration bits on POR
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

- bit 31 **Reserved:** This bit is hardwired as '1' to indicate the presence of the Config4 register
- bit 30-23 **Unimplemented:** Read as '0'
- bit 22-21 **IPLW<1:0>:** Width of the Status IPL and Cause RIPL bits
01 = IPL and RIPL bits are 8-bits in width
- bit 20-18 **MMAR<2:0>:** microMIPS Architecture Revision Level bits
000 = Release 1
- bit 17 **MCU:** MIPS® MCU™ ASE Implemented bit
1 = MCU ASE is implemented
- bit 16 **ISAONEXC:** ISA on Exception bit⁽¹⁾
1 = microMIPS is used on entrance to an exception vector
0 = MIPS32 ISA is used on entrance to an exception vector
- bit 15-14 **ISA<1:0>:** Instruction Set Availability bits⁽¹⁾
11 = Both MIPS32 and microMIPS are implemented; microMIPS is used when coming out of reset
10 = Both MIPS32 and microMIPS are implemented; MIPS32 ISA used when coming out of reset
- bit 13 **ULRI:** UserLocal Register Implemented bit
1 = UserLocal Coprocessor 0 register is implemented
- bit 12 **RXI:** RIE and XIE Implemented in PageGrain bit
1 = RIE and XIE bits are implemented
- bit 11 **DSP2P:** MIPS DSP ASE Revision 2 Presence bit
1 = DSP Revision 2 is present
- bit 10 **DSPP:** MIPS DSP ASE Presence bit
1 = DSP is present
- bit 9 **Unimplemented:** Read as '0'
- bit 8 **ITL:** Indicates that iFlowtrace® hardware is present
1 = The iFlowtrace® is implemented in the core
- bit 7 **Unimplemented:** Read as '0'
- bit 6 **VEIC:** External Vector Interrupt Controller bit
1 = Support for an external interrupt controller is implemented
- bit 5 **VINT:** Vector Interrupt bit
1 = Vector interrupts are implemented
- bit 4 **SP:** Small Page bit
0 = 4 KB page size
- bit 3 **CDMM:** Common Device Memory Map bit
1 = CDMM is implemented
- bit 2-1 **Unimplemented:** Read as '0'
- bit 0 **TL:** Trace Logic bit
0 = Trace logic is not implemented

Note 1: These bits are set based on the value of the BOOTISA Configuration bit (DEVCFG0<6>).

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

REGISTER 4-4: SBTxELOG2: SYSTEM BUS TARGET 'x' ERROR LOG REGISTER 2 ('x' = 0-13)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	R-0	R-0
	—	—	—	—	—	—	GROUP<1:0>	

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

bit 31-3 **Unimplemented:** Read as '0'

bit 1-0 **GROUP<1:0>:** Requested Permissions Group bits

11 = Group 3

10 = Group 2

01 = Group 1

00 = Group 0

Note: Refer to Table 4-6 for the list of available targets and their descriptions.

REGISTER 4-5: SBTxECON: SYSTEM BUS TARGET 'x' ERROR CONTROL REGISTER ('x' = 0-13)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
	—	—	—	—	—	—	—	ERRP
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

bit 31-25 **Unimplemented:** Read as '0'

bit 24 **ERRP:** Error Control bit

1 = Report protection group violation errors

0 = Do not report protection group violation errors

bit 23-0 **Unimplemented:** Read as '0'

Note: Refer to Table 4-6 for the list of available targets and their descriptions.

6.0 RESETS

Note: This data sheet summarizes the features of the PIC32MZ EF family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 7. “Resets”** (DS60001118) in the *“PIC32 Family Reference Manual”*, which is available from the Microchip web site (www.microchip.com/PIC32).

The Reset module combines all Reset sources and controls the device Master Reset signal, SYSRST. The device Reset sources are as follows:

- Power-on Reset (POR)
- Master Clear Reset pin ($\overline{\text{MCLR}}$)
- Software Reset (SWR)
- Watchdog Timer Reset (WDTR)
- Brown-out Reset (BOR)
- Configuration Mismatch Reset (CMR)
- Deadman Timer Reset (DMTR)

A simplified block diagram of the Reset module is illustrated in Figure 6-1.

FIGURE 6-1: SYSTEM RESET BLOCK DIAGRAM

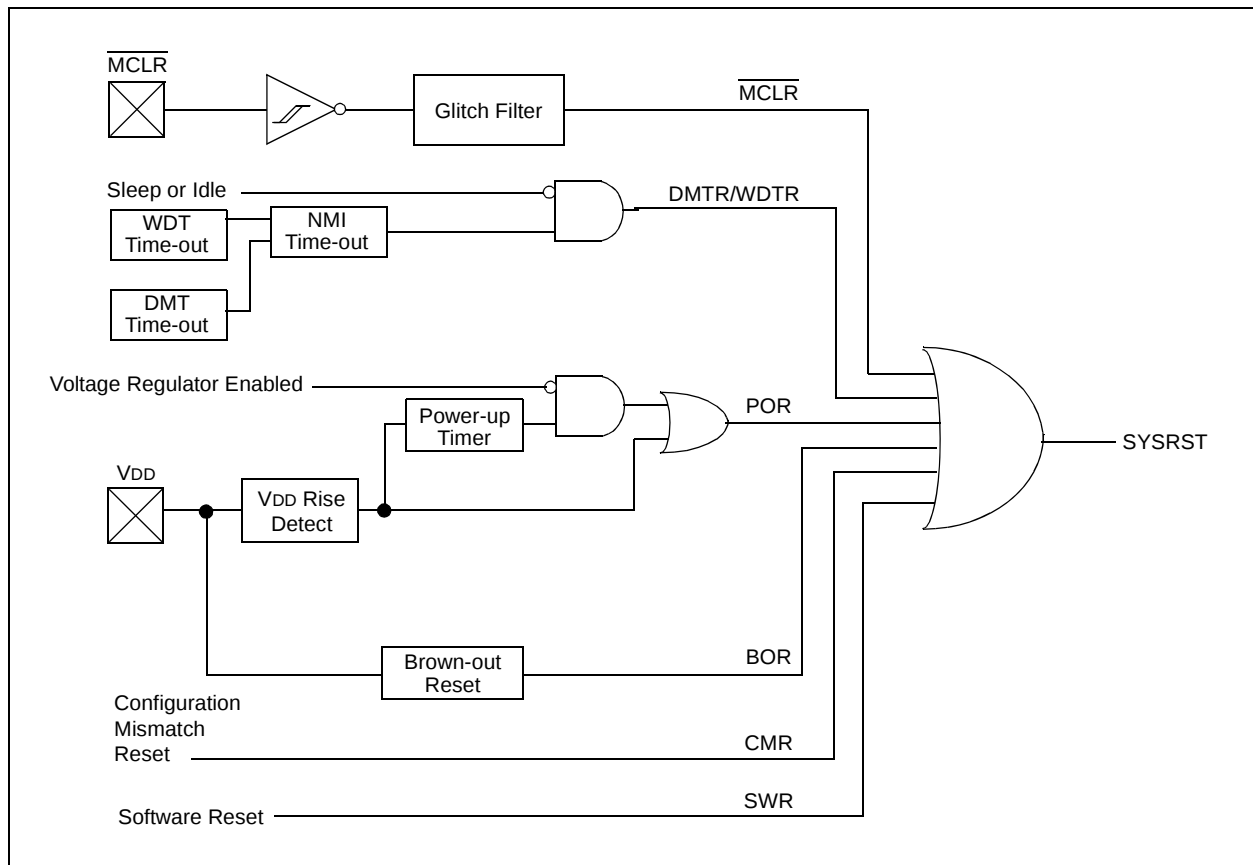


TABLE 7-3: INTERRUPT REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name ⁽¹⁾	Bit Range	Bits															All Resets	
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1		16/0
05C0	OFF032	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
05C4	OFF033	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
05C8	OFF034	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
05CC	OFF035	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
05D0	OFF036	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
05D4	OFF037	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
05D8	OFF038	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
05DC	OFF039	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
05E0	OFF040	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
05E4	OFF041	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
05E8	OFF042	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
05EC	OFF043	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
05F0	OFF044	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
05F4	OFF045	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
05F8	OFF046	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

- Note**
- 1: All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 “CLR, SET, and INV Registers”** for more information.
 - 2: This bit or register is not available on 64-pin devices.
 - 3: This bit or register is not available on devices without a CAN module.
 - 4: This bit or register is not available on 100-pin devices.
 - 5: Bits 31 and 30 are not available on 64-pin and 100-pin devices; bits 29 through 14 are not available on 64-pin devices.
 - 6: Bits 31, 30, 29, and bits 5 through 0 are not available on 64-pin and 100-pin devices; bit 31 is not available on 124-pin devices; bit 22 is not available on 64-pin devices.
 - 7: This bit or register is not available on devices without a Crypto module.
 - 8: This bit or register is not available on 124-pin devices.

11.1 USB OTG Control Registers

TABLE 11-1: USB REGISTER MAP 1

Virtual Address (BF8E_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
3000	USBCSR0	31:16	—	—	—	—	—	—	—	—	EP7TXIF	EP6TXIF	EP5TXIF	EP4TXIF	EP3TXIF	EP2TXIF	EP1TXIF	EP0IF	0000
		15:0	ISOUPD ⁽¹⁾	SOFT CONN ⁽¹⁾	HSEN	HSMODE	RESET	RESUME	SUSP MODE	SUSPEN	—	FUNC<6:0> ⁽¹⁾							2000
			— ⁽²⁾	— ⁽²⁾								— ⁽²⁾	— ⁽²⁾	— ⁽²⁾	— ⁽²⁾	— ⁽²⁾	— ⁽²⁾		
3004	USBCSR1	31:16	—	—	—	—	—	—	—	—	EP7TXIE	EP6TXIE	EP5TXIE	EP4TXIE	EP3TXIE	EP2TXIE	EP1TXIE	EP0IE	00FF
		15:0	—	—	—	—	—	—	—	—	EP7RXIF	EP6RXIF	EP5RXIF	EP4RXIF	EP3RXIF	EP2RXIF	EP1RXIF	—	0000
3008	USBCSR2	31:16	VBUSERRIE	SESSRQIE	DISCONIE	CONNIE	SOFIE	RESETIE	RESUMEIE	SUSPIE	VBUSERRIF	SESSREQIF	DISCONIF	CONNIF	SOFIF	RESETIF	RESUMEIF	SUSPIF	0000
		15:0	—	—	—	—	—	—	—	—	EP7RXIE	EP6RXIE	EP5RXIE	EP4RXIE	EP3RXIE	EP2RXIE	EP1RXIE	—	00FE
300C	USBCSR3	31:16	FORCEHST	FIFOACC	FORCEFS	FORCEHS	PACKET	TESTK	TESTJ	NAK	—	—	—	—	ENDPOINT<3:0>				0000
		15:0	—	—	—	—	—	RFRMNUM<10:0>											
3010	USB IE0CSR0 ⁽³⁾	31:16	—	—	—	—	— ⁽¹⁾	— ⁽¹⁾	— ⁽¹⁾	FLSHFIFO	SVC SETEND ⁽¹⁾	SVCPRP ⁽¹⁾	SEND STALL ⁽¹⁾	SETUP END ⁽¹⁾	DATAEND ⁽¹⁾	SENT STALL ⁽¹⁾	TXPKT RDY	RXPKT RDY	0000
							DISPING ⁽²⁾	DTWREN ⁽²⁾	DATA TGGL ⁽²⁾		NAK TMOUT ⁽²⁾	STATPKT ⁽²⁾	REQPKT ⁽²⁾	ERROR ⁽²⁾	SETUP PKT ⁽²⁾	RXSTALL ⁽²⁾			0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
3018	USB IE0CSR2 ⁽³⁾	31:16	—	—	—	NAKLIM<4:0> ⁽²⁾					SPEED<1:0> ⁽²⁾		—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	RXCNT<6:0>							
301C	USB IE0CSR3 ⁽³⁾	31:16	MPRXEN	MPTXEN	BIGEND	HBRXEN	HBTXEN	DYNFIFOS	SOFTCONE	UTMIDWID	—	—	—	—	—	—	—	—	xx00
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
3010	USB IENCSR0 ⁽⁴⁾	31:16	AUTOSSET	ISO ⁽¹⁾	MODE	DMA REQEN	FRC DATTG	DMA REQMD	— ⁽¹⁾	— ⁽¹⁾	INCOMP TX ⁽¹⁾	CLRDT	SENT STALL ⁽¹⁾	SEND STALL ⁽¹⁾	FLUSH	UNDER RUN ⁽¹⁾	FIFONE	TXPKT RDY	0000
				DTWREN ⁽²⁾					DATA TGGL ⁽²⁾	NAK TMOUT ⁽²⁾	RXSTALL ⁽²⁾		SETUPPKT ⁽²⁾	ERROR ⁽²⁾		0000			
		15:0	MULT<4:0>					TXMAXP<10:0>											
3014	USB IENCSR1 ⁽⁴⁾	31:16	AUTOCLR	ISO ⁽¹⁾	DMA REQEN	DISNYET ⁽¹⁾	DMA REQMD	— ⁽¹⁾	— ⁽¹⁾	INCOM PRX	CLRDT	SENTSTALL ⁽¹⁾	SENDSTALL ⁽¹⁾	FLUSH	DATAERR ⁽¹⁾	OVERRUN ⁽¹⁾	FIFOFULL	RXPKT RDY	0000
				AUTORQ ⁽²⁾		PIDERR ⁽²⁾		DATA TWEN ⁽²⁾	DATA TGGL ⁽²⁾			RXSTALL ⁽²⁾	REQPKT ⁽²⁾		DERR- NAKT ⁽¹⁾	ERROR ⁽²⁾			0000
		15:0	MULT<4:0>					RXMAXP<10:0>											
3018	USB IENCSR2 ⁽⁴⁾	31:16	TXINTERV<7:0> ⁽²⁾								SPEED<1:0> ⁽²⁾		PROTOCOL<1:0>		TEP<3:0>				0000
		15:0	—	—	RXCNT<13:0>												0000		
301C	USB IENCSR3 ^(1,3)	31:16	RXFIFOSZ<3:0>				TXFIFOSZ<3:0>				—	—	—	—	—	—	—	—	0000
		15:0	RXINTERV<7:0>								SPEED<1:0>		PROTOCOL<1:0>		TEP<3:0>				0000
3020	USB FIFO0	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
3024	USB FIFO1	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

- Note**
- 1: Device mode.
 - 2: Host mode.
 - 3: Definition for Endpoint 0 (ENDPOINT<3:0> (USBCSR<19:16>) = 0).
 - 4: Definition for Endpoints 1-7 (ENDPOINT<3:0> (USBCSR<19:16>) = 1 through 7).

TABLE 12-5: PORTB REGISTER MAP

Virtual Address (BF86_#)	Register Name(s)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0100	ANSELB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ANSB15	ANSB14	ANSB13	ANSB12	ANSB11	ANSB10	ANSB9	ANSB8	ANSB7	ANSB6	ANSB5	ANSB4	ANSB3	ANSB2	ANSB1	ANSB0	FFFF
0110	TRISB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRISB15	TRISB14	TRISB13	TRISB12	TRISB11	TRISB10	TRISB9	TRISB8	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	FFFF
0120	PORTB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx
0130	LATB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	LATB15	LATB14	LATB13	LATB12	LATB11	LATB10	LATB9	LATB8	LATB7	LATB6	LATB5	LATB4	LATB3	LATB2	LATB1	LATB0	xxxx
0140	ODCB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ODCB15	ODCB14	ODCB13	ODCB12	ODCB11	ODCB10	ODCB9	ODCB8	ODCB7	ODCB6	ODCB5	ODCB4	ODCB3	ODCB2	ODCB1	ODCB0	0000
0150	CNPUB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPUB15	CNPUB14	CNPUB13	CNPUB12	CNPUB11	CNPUB10	CNPUB9	CNPUB8	CNPUB7	CNPUB6	CNPUB5	CNPUB4	CNPUB3	CNPUB2	CNPUB1	CNPUB0	0000
0160	CNPDB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPDB15	CNPDB14	CNPDB13	CNPDB12	CNPDB11	CNPDB10	CNPDB9	CNPDB8	CNPDB7	CNPDB6	CNPDB5	CNPDB4	CNPDB3	CNPDB2	CNPDB1	CNPDB0	0000
0170	CNCONB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	EDGE DETECT	—	—	—	—	—	—	—	—	—	—	—	0000
0180	CNENB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNENB15	CNENB14	CNENB13	CNENB12	CNENB11	CNENB10	CNENB9	CNENB8	CNENB7	CNENB6	CNENB5	CNENB4	CNENB3	CNENB2	CNENB1	CNENB0	0000
0190	CNSTATB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CN STATB15	CN STATB14	CN STATB13	CN STATB12	CN STATB11	CN STATB10	CN STATB9	CN STATB8	CN STATB7	CN STATB6	CN STATB5	CN STATB4	CN STATB3	CN STATB2	CN STATB1	CN STATB0	0000
01A0	CNNEB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNNEB15	CNNEB14	CNNEB13	CNNEB12	CNNEB11	CNNEB10	CNNEB9	CNNEB8	CNNEB7	CNNEB6	CNNEB5	CNNEB4	CNNEB3	CNNEB2	CNNEB1	CNNEB0	0000
01B0	CNFB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNFB15	CNFB14	CNFB13	CNFB12	CNFB11	CNFB10	CNFB9	CNFB8	CNFB7	CNFB6	CNFB5	CNFB4	CNFB3	CNFB2	CNFB1	CNFB0	0000
01C0	SRCON0B	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	SR0B14	—	—	—	SR0B10	SR0B9	SR0B8	—	—	SR0B5	—	SR0B3	—	—	—	0000
01D0	SRCON1B	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	SR1B14	—	—	—	SR1B10	SR1B9	SR1B8	—	—	SR1B5	—	SR1B3	—	—	—	0000

Legend: x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 “CLR, SET, and INV Registers”** for more information.

NOTES:

- Prescaler capture event modes:
 - Capture timer value on every 4th rising edge of input at ICx pin
 - Capture timer value on every 16th rising edge of input at ICx pin

- Device wake-up from capture pin during Sleep and Idle modes
- Interrupt on input capture event
- 4-word FIFO buffer for capture values; Interrupt optionally generated after 1, 2, 3, or 4 buffer locations are filled
- Input capture can also be used to provide additional sources of external interrupts

- Capture timer value on every edge (rising and falling), specified edge first

Note 1: An 'x' in a signal, register or bit name denotes the number of the capture channel.

Note 2: See Table 17-1 for Timerx and Timery selections.

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

REGISTER 21-1: I2CxCON: I²C CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	PCIE	SCIE	BOEN	SDAHT	SBCDE	AHEN	DHEN
15:8	R/W-0	U-0	R/W-0	R/W-1, HC	R/W-0	R/W-0	R/W-0	R/W-0
	ON	—	SIDL	SCKREL	STRICT	A10M	DISSLW	SMEN
7:0	R/W-0	R/W-0	R/W-0	R/W-0, HC	R/W-0, HC	R/W-0, HC	R/W-0, HC	R/W-0, HC
	GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN

Legend:

R = Readable bit

-n = Value at POR

HC = Cleared in Hardware

W = Writable bit

'1' = Bit is set

U = Unimplemented bit, read as '0'

'0' = Bit is cleared

x = Bit is unknown

bit 31-23 **Unimplemented:** Read as '0'

bit 22 **PCIE:** Stop Condition Interrupt Enable bit (I²C Slave mode only)

1 = Enable interrupt on detection of Stop condition

0 = Stop detection interrupts are disabled

bit 21 **SCIE:** Start Condition Interrupt Enable bit (I²C Slave mode only)

1 = Enable interrupt on detection of Start or Restart conditions

0 = Start detection interrupts are disabled

bit 20 **BOEN:** Buffer Overwrite Enable bit (I²C Slave mode only)

1 = I2CxRCV is updated and $\overline{ACK}$ is generated for a received address/data byte, ignoring the state of the I2COV bit (I2CxSTAT<6>) only if the RBF bit (I2CxSTAT<2>) = 0

0 = I2CxRCV is only updated when the I2COV bit (I2CxSTAT<6>) is clear

bit 19 **SDAHT:** SDA Hold Time Selection bit

1 = Minimum of 300 ns hold time on SDA after the falling edge of SCL

0 = Minimum of 100 ns hold time on SDA after the falling edge of SCL

bit 18 **SBCDE:** Slave Mode Bus Collision Detect Enable bit (I²C Slave mode only)

1 = Enable slave bus collision interrupts

0 = Slave bus collision interrupts are disabled

bit 18 **AHEN:** Address Hold Enable bit (Slave mode only)

1 = Following the 8th falling edge of SCL for a matching received address byte; SCKREL bit will be cleared and the SCL will be held low.

0 = Address holding is disabled

bit 16 **DHEN:** Data Hold Enable bit (I²C Slave mode only)

1 = Following the 8th falling edge of SCL for a received data byte; slave hardware clears the SCKREL bit and SCL is held low

0 = Data holding is disabled

bit 15 **ON:** I²C Enable bit

1 = Enables the I²C module and configures the SDA and SCL pins as serial port pins

0 = Disables the I²C module; all I²C pins are controlled by PORT functions

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit

1 = Discontinue module operation when device enters Idle mode

0 = Continue module operation in Idle mode

28.0 12-BIT HIGH-SPEED SUCCESSIVE APPROXIMATION REGISTER (SAR) ANALOG-TO-DIGITAL CONVERTER (ADC)

Note: This data sheet summarizes the features of the PIC32MZ EF family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 22. “12-bit High-Speed Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC)”** (DS60001344) in the “PIC32 Family Reference Manual”, which is available from the Microchip web site (www.microchip.com/PIC32).

The 12-bit High-Speed Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC) includes the following key features:

- 12-bit resolution
- Six ADC modules with dedicated Sample and Hold (S&H) circuits
- Two dedicated ADC modules can be combined in Turbo mode to provide double conversion rate (clock sources for combined ADC modules must be synchronous)
- Single-ended and/or differential inputs
- Can operate during Sleep mode
- Supports touch sense applications
- Six digital comparators
- Six digital filters supporting two modes:
 - Oversampling mode
 - Averaging mode
- Early interrupt generation resulting in faster processing of converted data
- Designed for motor control, power conversion, and general purpose applications

A simplified block diagram of the ADC module is illustrated in Figure 28-1.

The 12-bit HS SAR ADC has up to five dedicated ADC modules (ADC0-ADC4) and one shared ADC module (ADC7). The dedicated ADC modules use a single input (or its alternate) and are intended for high-speed and precise sampling of time-sensitive or transient inputs. The the shared ADC module incorporates a multiplexer on the input to facilitate a larger group of inputs, with slower sampling, and provides flexible automated scanning option through the input scan logic.

For each ADC module, the analog inputs are connected to the S&H capacitor. The clock, sampling time, and output data resolution for each ADC module can be set independently. The ADC module performs the conversion of the input analog signal based on the configurations set in the registers. When conversion is complete, the final result is stored in the result buffer for the specific analog input and is passed to the digital filter and digital comparator if configured to use data from this particular sample. Input to ADCx mapping is illustrated in Figure 28-2.

The throughput rate (see Table 37-39 in **37.0 “Electrical Characteristics”**) is calculated, as shown in Equation 28-1.

EQUATION 28-1: ADC THROUGHPUT RATE

$$FTP = \frac{T_{AD}}{(T_{SAMP} + T_{CONV})}$$

Where,

T_{AD} = the frequency of the individual ADC module

Note 1: Prior to enabling the ADC module, the user application must copy the ADC calibration data (DEVADC0-DEVADC4, DEVADC7; see Register 34-13) from the Configuration memory into the ADC Configuration registers (ADC0CFG-ADC4CFG, ADC7CFG).

2: Configure the AICMPEN (ADC-CON1<12>) and IOANCPEN (CFG-CON<7>) bits to '0' if VDD >= 2.5V. Set the AICMPEN and IOANCPEN bits to '1' if VDD < 2.5V.

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

**REGISTER 28-14: ADCCMPENx: ADC DIGITAL COMPARATOR 'x' ENABLE REGISTER
(‘x’ = 1 THROUGH 6)**

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0 CMPE31 ⁽¹⁾	R/W-0 CMPE30 ⁽¹⁾	R/W-0 CMPE29 ⁽¹⁾	R/W-0 CMPE28 ⁽¹⁾	R/W-0 CMPE27 ⁽¹⁾	R/W-0 CMPE26 ⁽¹⁾	R/W-0 CMPE25 ⁽¹⁾	R/W-0 CMPE24 ⁽¹⁾
23:16	R/W-0 CMPE23 ⁽¹⁾	R/W-0 CMPE22 ⁽¹⁾	R/W-0 CMPE21 ⁽¹⁾	R/W-0 CMPE20 ⁽¹⁾	R/W-0 CMPE19 ⁽¹⁾	R/W-0 CMPE18	R/W-0 CMPE17	R/W-0 CMPE16
15:8	R/W-0 CMPE15	R/W-0 CMPE14	R/W-0 CMPE13	R/W-0 CMPE12	R/W-0 CMPE11	R/W-0 CMPE10	R/W-0 CMPE9	R/W-0 CMPE8
7:0	R/W-0 CMPE7	R/W-0 CMPE6	R/W-0 CMPE5	R/W-0 CMPE4	R/W-0 CMPE3	R/W-0 CMPE2	R/W-0 CMPE1	R/W-0 CMPE0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-0 **CMPE31:CMPE0**: ADC Digital Comparator 'x' Enable bits^(2,3)

These bits enable conversion results corresponding to the Analog Input to be processed by the Digital Comparator. CMPE0 enables AN0, CMPE1 enables AN1, and so on.

Note 1: This bit is not available on 64-pin devices.

2: CMPE_x = AN_x, where 'x' = 0-31 (Digital Comparator inputs are limited to AN0 through AN31).

3: Changing the bits in this register while the Digital Comparator is enabled (ENDCMP = 1) can result in unpredictable behavior.

TABLE 29-1: CAN1 REGISTER SUMMARY FOR PIC32MZXXXECF AND PIC32MZXXXECH DEVICES (CONTINUED)

Virtual Address (BF88_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
00F0	C1FLTCON3	31:16	FLTEN15	MSEL15<1:0>	FSEL15<4:0>					FLTEN14	MSEL14<1:0>	FSEL14<4:0>					0000		
		15:0	FLTEN13	MSEL13<1:0>	FSEL13<4:0>					FLTEN12	MSEL12<1:0>	FSEL12<4:0>					0000		
0100	C1FLTCON4	31:16	FLTEN19	MSEL19<1:0>	FSEL19<4:0>					FLTEN18	MSEL18<1:0>	FSEL18<4:0>					0000		
		15:0	FLTEN17	MSEL17<1:0>	FSEL17<4:0>					FLTEN16	MSEL16<1:0>	FSEL16<4:0>					0000		
0110	C1FLTCON5	31:16	FLTEN23	MSEL23<1:0>	FSEL23<4:0>					FLTEN22	MSEL22<1:0>	FSEL22<4:0>					0000		
		15:0	FLTEN21	MSEL21<1:0>	FSEL21<4:0>					FLTEN20	MSEL20<1:0>	FSEL20<4:0>					0000		
0120	C1FLTCON6	31:16	FLTEN27	MSEL27<1:0>	FSEL27<4:0>					FLTEN26	MSEL26<1:0>	FSEL26<4:0>					0000		
		15:0	FLTEN25	MSEL25<1:0>	FSEL25<4:0>					FLTEN24	MSEL24<1:0>	FSEL24<4:0>					0000		
0130	C1FLTCON7	31:16	FLTEN31	MSEL31<1:0>	FSEL31<4:0>					FLTEN30	MSEL30<1:0>	FSEL30<4:0>					0000		
		15:0	FLTEN29	MSEL29<1:0>	FSEL29<4:0>					FLTEN28	MSEL28<1:0>	FSEL28<4:0>					0000		
0140-0330	C1RXFn (n = 0-31)	31:16	SID<10:0>										---		EXID	---		EID<17:16>	xxxx
		15:0	EID<15:0>																xxxx
0340	C1FIFOBA	31:16	C1FIFOBA<31:0>																0000
		15:0																	0000
0350	C1FIFOCONn (n = 0)	31:16	---	---	---	---	---	---	---	---	---	---	FSIZE<4:0>					0000	
		15:0	---	FRESET	UINC	DONLY	---	---	---	---	TXEN	TXABAT	TXLARB	TXERR	TXREQ	RTREN	TXPRI<1:0>	0000	
0360	C1FIFOINTn (n = 0)	31:16	---	---	---	---	---	TXNFULLIE	TXHALFIE	TXEMPTYIE	---	---	---	---	RXOVFLIE	RXFULLIE	RXHALFIE	RXN EMPTYIE	0000
		15:0	---	---	---	---	---	TXNFULLIF	TXHALFIF	TXEMPTYIF	---	---	---	---	RXOVFLIF	RXFULLIF	RXHALFIF	RXN EMPTYIF	0000
0370	C1FIFOUAn (n = 0)	31:16	C1FIFOUA<31:0>																0000
		15:0																	0000
0380	C1FIFOCIn (n = 0)	31:16	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	0000
		15:0	---	---	---	---	---	---	---	---	---	---	C1FIFOCI<4:0>					0000	
0390-0B40	C1FIFOCONn C1FIFOINTn C1FIFOUAn C1FIFOCIn (n = 1-31)	31:16	---	---	---	---	---	---	---	---	---	---	FSIZE<4:0>					0000	
		15:0	---	FRESET	UINC	DONLY	---	---	---	---	TXEN	TXABAT	TXLARB	TXERR	TXREQ	RTREN	TXPRI<1:0>	0000	
		31:16	---	---	---	---	---	TXNFULLIE	TXHALFIE	TXEMPTYIE	---	---	---	---	RXOVFLIE	RXFULLIE	RXHALFIE	RXN EMPTYIE	0000
		15:0	---	---	---	---	---	TXNFULLIF	TXHALFIF	TXEMPTYIF	---	---	---	---	RXOVFLIF	RXFULLIF	RXHALFIF	RXN EMPTYIF	0000
		31:16	C1FIFOUA<31:0>																0000
		15:0																	0000
		31:16	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 "CLR, SET, and INV Registers"** for more information.

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

REGISTER 30-15: ETHSTAT: ETHERNET CONTROLLER STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BUFCNT<7:0> ⁽¹⁾							
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0
	ETHBUSY ⁽⁵⁾	TxBUSY ^(2,6)	RxBUSY ^(3,6)	—	—	—	—	—

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-24 **Unimplemented:** Read as '0'

bit 23-16 **BUFCNT<7:0>:** Packet Buffer Count bits⁽¹⁾

Number of packet buffers received in memory. Once a packet has been successfully received, this register is incremented by hardware based on the number of descriptors used by the packet. Software decrements the counter (by writing to the BUFCDEC bit (ETHCON1<0>)) for each descriptor used) after a packet has been read out of the buffer. The register does not roll over (0xFF to 0x00) when hardware tries to increment the register and the register is already at 0xFF. Conversely, the register does not roll under (0x00 to 0xFF) when software tries to decrement the register and the register is already at 0x0000. When software attempts to decrement the counter at the same time that the hardware attempts to increment the counter, the counter value will remain unchanged.

When this register value reaches 0xFF, the RX logic will halt (only if automatic Flow Control is enabled) awaiting software to write the BUFCDEC bit in order to decrement the register below 0xFF.

If automatic Flow Control is disabled, the RxDMA will continue processing and the BUFCNT will saturate at a value of 0xFF.

When this register is non-zero, the PKTPEND status bit will be set and an interrupt may be generated, depending on the value of the ETHIEN bit <PKTPENDIE> register.

When the ETHRXST register is written, the BUFCNT counter is automatically cleared to 0x00.

Note: BUFCNT will not be cleared when ON is set to '0'. This enables software to continue to utilize and decrement this count.

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **ETHBUSY:** Ethernet Module busy bit⁽⁵⁾

1 = Ethernet logic has been turned on (ON (ETHCON1<15>) = 1) or is completing a transaction

0 = Ethernet logic is idle

This bit indicates that the module has been turned on or is completing a transaction after being turned off.

Note 1: This bit is only used for RX operations.

2: This bit is only affected by TX operations.

3: This bit is only affected by RX operations.

4: This bit is affected by TX and RX operations.

5: This bit will be *set* when the ON bit (ETHCON1<15>) = 1.

6: This bit will be *cleared* when the ON bit (ETHCON1<15>) = 0.

REGISTER 34-5: DEVCFG2/ADEVCFG2: DEVICE CONFIGURATION WORD 2 (CONTINUED)

bit 3 **Reserved:** Write as '1'

bit 2-0 **FPLLIDIV<2:0>:** PLL Input Divider bits

111 = Divide by 8

110 = Divide by 7

101 = Divide by 6

100 = Divide by 5

011 = Divide by 4

010 = Divide by 3

001 = Divide by 2

000 = Divide by 1

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

REGISTER 34-9: CFGEBIC: EXTERNAL BUS INTERFACE CONTROL PIN CONFIGURATION REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	U-0
	EBI RDYINV3	EBI RDYINV2	EBI RDYIN1	—	EBI RDYEN3	EBI RDYEN2	EBI RDYEN1	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
	—	—	—	—	—	—	EBIRDYLVL	EBIRPEN
15:8	U-0	U-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0
	—	—	EBIWEEN	EBIOEEN	—	—	EBIBSEN1	EBIBSEN0
7:0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0
	EBICSEN3	EBICSEN2	EBICSEN1	EBICSEN0	—	—	EBIDEN1	EBIDEN0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 31 **EBIRDYINV3:** EBIRDY3 Inversion Control bit
1 = Invert EBIRDY3 pin before use
0 = Do not invert EBIRDY3 pin before use
- bit 30 **EBIRDYINV2:** EBIRDY2 Inversion Control bit
1 = Invert EBIRDY2 pin before use
0 = Do not invert EBIRDY2 pin before use
- bit 29 **EBIRDYINV1:** EBIRDY1 Inversion Control bit
1 = Invert EBIRDY1 pin before use
0 = Do not invert EBIRDY1 pin before use
- bit 28 **Unimplemented:** Read as '0'
- bit 27 **EBIRDYEN3:** EBIRDY3 Pin Enable bit
1 = EBIRDY3 pin is enabled for use by the EBI module
0 = EBIRDY3 pin is available for general use
- bit 26 **EBIRDYEN2:** EBIRDY2 Pin Enable bit
1 = EBIRDY2 pin is enabled for use by the EBI module
0 = EBIRDY2 pin is available for general use
- bit 25 **EBIRDYEN1:** EBIRDY1 Pin Enable bit
1 = EBIRDY1 pin is enabled for use by the EBI module
0 = EBIRDY1 pin is available for general use
- bit 24-18 **Unimplemented:** Read as '0'
- bit 17 **EBIRDYLVL:** EBIRDYx Pin Sensitivity Control bit
1 = Use level detect for EBIRDYx pins
0 = Use edge detect for EBIRDYx pins
- bit 16 **EBIRPEN:** EBIRP Pin Sensitivity Control bit
1 = EBIRP pin is enabled for use by the EBI module
0 = EBIRP pin is available for general use
- bit 15-14 **Unimplemented:** Read as '0'
- bit 13 **EBIWEEN:** EBIWE Pin Enable bit
1 = EBIWE pin is enabled for use by the EBI module
0 = EBIWE pin is available for general use

Note: When EBIMD = 1, the bits in this register are ignored and the pins are available for general use.

FIGURE 37-6: TIMER1-TIMER9 EXTERNAL CLOCK TIMING CHARACTERISTICS

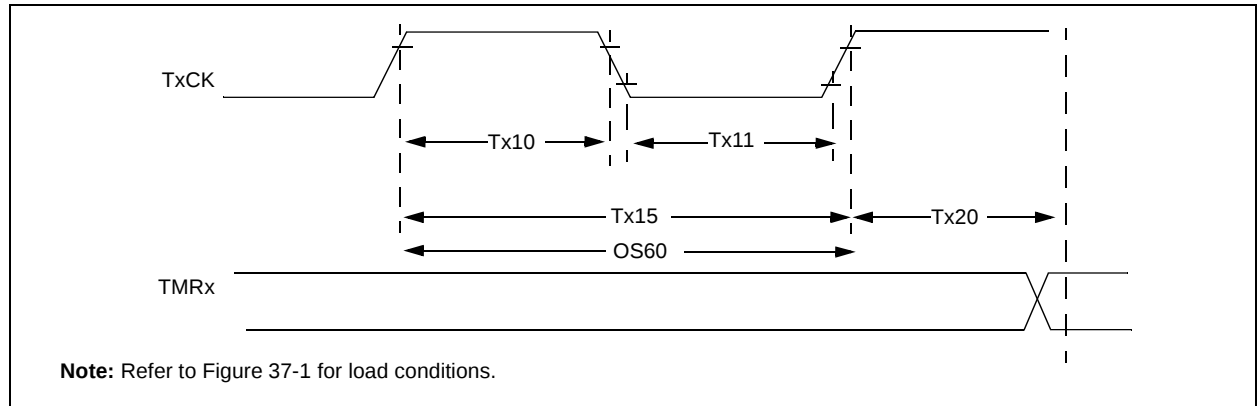


TABLE 37-25: TIMER1 EXTERNAL CLOCK TIMING REQUIREMENTS⁽¹⁾

AC CHARACTERISTICS				Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	Symbol	Characteristics ⁽²⁾		Min.	Typ.	Max.	Units	Conditions
TA10	TtxH	TxCK High Time	Synchronous, with prescaler	$[(12.5 \text{ ns or } 1 \text{ TPBCLK3}) / N] + 20 \text{ ns}$	—	—	ns	Must also meet parameter TA15 (Note 3)
			Asynchronous, with prescaler	10	—	—	ns	—
TA11	TtxL	TxCK Low Time	Synchronous, with prescaler	$[(12.5 \text{ ns or } 1 \text{ TPBCLK3}) / N] + 20 \text{ ns}$	—	—	ns	Must also meet parameter TA15 (Note 3)
			Asynchronous, with prescaler	10	—	—	ns	—
TA15	TtxP	TxCK Input Period	Synchronous, with prescaler	$[(\text{Greater of } 20 \text{ ns or } 2 \text{ TPBCLK3}) / N] + 30 \text{ ns}$	—	—	ns	VDD > 2.7V (Note 3)
				$[(\text{Greater of } 20 \text{ ns or } 2 \text{ TPBCLK3}) / N] + 50 \text{ ns}$	—	—	ns	VDD < 2.7V (Note 3)
			Asynchronous, with prescaler	20	—	—	ns	VDD > 2.7V
				50	—	—	ns	VDD < 2.7V
OS60	Ft1	SOSC1/T1CK Oscillator Input Frequency Range (oscillator enabled by setting TCS bit (T1CON<1>))		32	—	50	kHz	—
TA20	TCKEXTMRL	Delay from External TxCK Clock Edge to Timer Increment		—		1	TPBCLK3	—

Note 1: Timer1 is a Type A timer.

2: This parameter is characterized, but not tested in manufacturing.

3: N = Prescale Value (1, 8, 64, 256).

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

TABLE 37-38: ADC MODULE SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	Symbol	Characteristics	Min.	Typ.	Max.	Units	Conditions
Device Supply							
AD01	AVDD	Module VDD Supply	Greater of VDD – 0.3 or 2.1	—	Lesser of VDD + 0.3 or 3.6	V	—
AD02	AVSS	Module Vss Supply	VSS	—	VSS + 0.3	V	—
Reference Inputs							
AD05	VREFH	Reference Voltage High	VREFL + 1.8	—	AVDD	V	(Note 1)
AD06	VREFL	Reference Voltage Low	AVSS	—	VREFH – 1.8	V	(Note 1)
AD07	VREF	Absolute Reference Voltage (VREFH – VREFL)	1.8	—	AVDD	V	(Note 2)
AD08	IREF	Current Drain	—	102	—	μA	Per ADCx ('x' = 0-4, 7)
Analog Input							
AD12	VINH-VINL	Full-Scale Input Span	VREFL	—	VREFH	V	—
AD13	VINL	Absolute VINL Input Voltage	AVSS	—	VREFL	V	—
AD14	VINH	Absolute VINH Input Voltage	AVSS	—	VREFH	V	—
ADC Accuracy – Measurements with External VREF+/VREF-							
AD20c	Nr	Resolution	6	—	12	bits	Selectable 6, 8, 10, 12 Resolution Ranges
AD21c	INL	Integral Nonlinearity	—	±3	—	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.3V
AD22c	DNL	Differential Nonlinearity	—	±1	—	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.3V
AD23c	GERR	Gain Error	—	±8	—	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.3V
AD24c	EOFF	Offset Error	—	±2	—	LSb	VINL = AVSS = 0V, AVDD = 3.3V
Dynamic Performance							
AD31b	SINAD	Signal to Noise and Distortion	—	67	—	dB	Single-ended (Notes 2,3)
AD34b	ENOB	Effective Number of bits	—	10.5	—	bits	(Notes 2,3)

Note 1: These parameters are not characterized or tested in manufacturing.

2: These parameters are characterized, but not tested in manufacturing.

3: Characterized with a 1 kHz sine wave.

4: The ADC module is functional at VBORMIN < VDD < VDDMIN, but with degraded performance. Unless otherwise stated, module functionality is guaranteed, but not characterized.

**64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body [QFN]
With 7.70 x 7.70 Exposed Pad [QFN]**

TOP VIEW

NOTE 1

(DATUM B)

(DATUM A)

2X

2X

SIDE VIEW

SEATING PLANE

A

A1

A3

64X

BOTTOM VIEW

NOTE 1

D2

E2

L

N

K

64X b

Feature Control Frames:

- TOP VIEW: $\text{2X} \left[\text{Surface Symbol} \right] 0.25 \text{ C}$
- SIDE VIEW: $\left[\text{Surface Symbol} \right] 0.10 \text{ C}$, $\left[\text{Surface Symbol} \right] 0.08 \text{ C}$
- BOTTOM VIEW: $\left[\text{Feature Control Frame} \right] 0.10 \text{ (M) C A B}$, $\left[\text{Feature Control Frame} \right] 0.10 \text{ (M) C A B}$, $\left[\text{Feature Control Frame} \right] 0.05 \text{ (M) C}$

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PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

B.6 Resets

On PIC32MZ EF devices, the Reset module adds eight bits to the NMICNT field to make the time-out period before device Reset longer, as described in Table B-5.

TABLE B-5: RESETS DIFFERENCES

PIC32MZ EC Feature	PIC32MZ EF Feature
Countdown to Reset During NMIs	
On PIC32MZ EC devices, the NMICNT<7:0> field is eight bits long, giving a maximum of 256 instructions before the device Reset.	On PIC32MZ EF devices, the NMICNT<15:0> field is now 16 bits long, giving a longer period of time (up to 65,536 instructions) prior to a device Reset.

B.7 USB

On PIC32MZ EF devices, a new USBCRCON register has been added to assist in controlling the reset of the USB module, and triggering interrupts based on VBUS voltage levels. This register also overcomes an errata on PIC32MZ EC devices that requires a three second start-up on the USB module.

B.8 I/O Ports

On PIC32MZ EF devices, many of the I/O pins now feature slew rate control bits to control how fast the pin makes a low-to-high or high-to-low transition. The Change Notification feature has also been enhanced to allow detection of level events in addition to edge detection. However, the SIDL bit is not present in the CNCONx registers on PIC32MZ EF devices, as it is on PIC32MZ EC devices.

B.9 Watchdog Timer

PIC32MZ EF devices use a new Watchdog Timer, although the overall control through the DEVCFGx words remains identical to that of PIC32MZ EC devices. Table B-6 lists two more changes, as well.

TABLE B-6: WATCHDOG TIMER DIFFERENCES

PIC32MZ EC Feature	PIC32MZ EF Feature
Watchdog Timer Postscaler	
On PIC32MZ EC devices, the SWDTPS<4:0> bits (WDTCON<6:2>) reflect the postscaler setting for the Watchdog Timer.	On PIC32MZ EF devices, the field has been changed to the RUNDIV<4:0> bits (WDTCON<12:8>).
Watchdog Windowed Mode	
On PIC32MZ EC devices, WDTWINEN is at bit position 1 (WDTCON<1>).	On PIC32MZ EF devices, WDTWINEN is now at bit position 0 (WDTCON<0>).