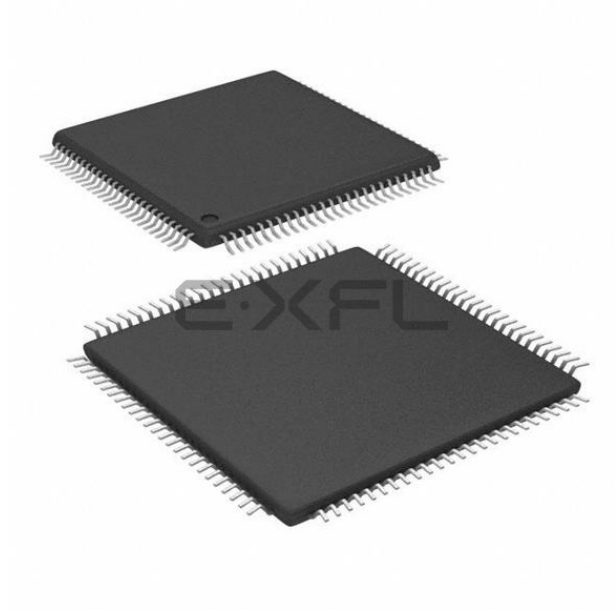
Microchip Technology - PIC32MZ2048EFH100T-I/PT Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® M-Class
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, PMP, SPI, SQI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	78
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	2.1V ~ 3.6V
Data Converters	A/D 40x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mz2048efh100t-i-pt

TABLE 3-3: COPROCESSOR 0 REGISTERS (CONTINUED)

Register Number	Register Name	Function
12	Status	Processor status and control.
	IntCtl	Interrupt control of vector spacing.
	SRSCtl	Shadow register set control.
	SRSMap	Shadow register mapping control.
	View_IPL	Allows the Priority Level to be read/written without extracting or inserting that bit from/to the Status register.
	SRSMAP2	Contains two 4-bit fields that provide the mapping from a vector number to the shadow set number to use when servicing such an interrupt.
13	Cause	Describes the cause of the last exception.
	NestedExc	Contains the error and exception level status bit values that existed prior to the current exception.
	View_RIPL	Enables read access to the RIPL bit that is available in the Cause register.
14	EPC	Program counter at last exception.
	NestedEPC	Contains the exception program counter that existed prior to the current exception.
15	PRID	Processor identification and revision
	Ebase	Exception base address of exception vectors.
	CDMMBase	Common device memory map base.
16	Config	Configuration register.
	Config1	Configuration register 1.
	Config2	Configuration register 2.
	Config3	Configuration register 3.
	Config4	Configuration register 4.
	Config5	Configuration register 5.
	Config7	Configuration register 7.
17	LLAddr	Load link address (MPU only).
18	WatchLo	Low-order watchpoint address (MPU only).
19	WatchHi	High-order watchpoint address (MPU only).
20-22	Reserved	Reserved in the PIC32 core.
23	Debug	EJTAG debug register.
	TraceControl	EJTAG trace control.
	TraceControl2	EJTAG trace control 2.
	UserTraceData1	EJTAG user trace data 1 register.
	TraceBPC	EJTAG trace breakpoint register.
	Debug2	Debug control/exception status 1.
24	DEPC	Program counter at last debug exception.
	UserTraceData2	EJTAG user trace data 2 register.
25	PerfCtl0	Performance counter 0 control.
	PerfCnt0	Performance counter 0.
	PerfCtl1	Performance counter 1 control.
	PerfCnt1	Performance counter 1.
26	ErrCtl	Software test enable of way-select and data RAM arrays for I-Cache and D-Cache (MPU only).
27	Reserved	Reserved in the PIC32 core.
28	TagLo/DataLo	Low-order portion of cache tag interface (MPU only).
29	Reserved	Reserved in the PIC32 core.
30	ErrorEPC	Program counter at last error exception.
31	DeSave	Debug exception save.

4.2 System Bus Arbitration

Note: The System Bus interconnect implements one or more instantiations of the SonicsSX® interconnect from Sonics, Inc. This document contains materials that are (c) 2003-2015 Sonics, Inc., and that constitute proprietary information of Sonics, Inc. SonicsSX is a registered trademark of Sonics, Inc. All such materials and trademarks are used under license from Sonics, Inc.

As shown in the PIC32MZ EF Family Block Diagram (see Figure 1-1), there are multiple initiator modules (I1 through I14) in the system that can access various target modules (T1 through T13). Table 4-4 illustrates which initiator can access which target. The System Bus supports simultaneous access to targets by initiators, so long as the initiators are accessing different targets. The System Bus will perform arbitration, if multiple initiators attempt to access the same target.

TABLE 7-2: INTERRUPT IRQ, VECTOR, AND BIT LOCATION (CONTINUED)

Interrupt Source[1]	XC32 Vector Name	IRQ #	Vector #	Interrupt Bit Location				Persistent Interrupt
				Flag	Enable	Priority	Sub-priority	
ADC Data 19[2]	_ADC_DATA19_VECTOR	78	OFF078<17:1>	IFS2<14>	IEC2<14>	IPC19<20:18>	IPC19<17:16>	Yes
ADC Data 20[2]	_ADC_DATA20_VECTOR	79	OFF079<17:1>	IFS2<15>	IEC2<15>	IPC19<28:26>	IPC19<25:24>	Yes
ADC Data 21[2]	_ADC_DATA21_VECTOR	80	OFF080<17:1>	IFS2<16>	IEC2<16>	IPC20<4:2>	IPC20<1:0>	Yes
ADC Data 22[2]	_ADC_DATA22_VECTOR	81	OFF081<17:1>	IFS2<17>	IEC2<17>	IPC20<12:10>	IPC20<9:8>	Yes
ADC Data 23[2]	_ADC_DATA23_VECTOR	82	OFF082<17:1>	IFS2<18>	IEC2<18>	IPC20<20:18>	IPC20<17:16>	Yes
ADC Data 24[2]	_ADC_DATA24_VECTOR	83	OFF083<17:1>	IFS2<19>	IEC2<19>	IPC20<28:26>	IPC20<25:24>	Yes
ADC Data 25[2]	_ADC_DATA25_VECTOR	84	OFF084<17:1>	IFS2<20>	IEC2<20>	IPC21<4:2>	IPC21<1:0>	Yes
ADC Data 26[2]	_ADC_DATA26_VECTOR	85	OFF085<17:1>	IFS2<21>	IEC2<21>	IPC21<12:10>	IPC21<9:8>	Yes
ADC Data 27[2]	_ADC_DATA27_VECTOR	86	OFF086<17:1>	IFS2<22>	IEC2<22>	IPC21<20:18>	IPC21<17:16>	Yes
ADC Data 28[2]	_ADC_DATA28_VECTOR	87	OFF087<17:1>	IFS2<23>	IEC2<23>	IPC21<28:26>	IPC21<25:24>	Yes
ADC Data 29[2]	_ADC_DATA29_VECTOR	88	OFF088<17:1>	IFS2<24>	IEC2<24>	IPC22<4:2>	IPC22<1:0>	Yes
ADC Data 30[2]	_ADC_DATA30_VECTOR	89	OFF089<17:1>	IFS2<25>	IEC2<25>	IPC22<12:10>	IPC22<9:8>	Yes
ADC Data 31[2]	_ADC_DATA31_VECTOR	90	OFF090<17:1>	IFS2<26>	IEC2<26>	IPC22<20:18>	IPC22<17:16>	Yes
ADC Data 32[2]	_ADC_DATA32_VECTOR	91	OFF091<17:1>	IFS2<27>	IEC2<27>	IPC22<28:26>	IPC22<25:24>	Yes
ADC Data 33[2]	_ADC_DATA33_VECTOR	92	OFF092<17:1>	IFS2<28>	IEC2<28>	IPC23<4:2>	IPC23<1:0>	Yes
ADC Data 34[2]	_ADC_DATA34_VECTOR	93	OFF093<17:1>	IFS2<29>	IEC2<29>	IPC23<12:10>	IPC23<9:8>	Yes
ADC Data 35[2,3]	_ADC_DATA35_VECTOR	94	OFF094<17:1>	IFS2<30>	IEC2<30>	IPC23<20:18>	IPC23<17:16>	Yes
ADC Data 36[2,3]	_ADC_DATA36_VECTOR	95	OFF095<17:1>	IFS2<31>	IEC2<31>	IPC23<28:26>	IPC23<25:24>	Yes
ADC Data 37[2,3]	_ADC_DATA37_VECTOR	96	OFF096<17:1>	IFS3<0>	IEC3<0>	IPC24<4:2>	IPC24<1:0>	Yes
ADC Data 38[2,3]	_ADC_DATA38_VECTOR	97	OFF097<17:1>	IFS3<1>	IEC3<1>	IPC24<12:10>	IPC24<9:8>	Yes
ADC Data 39[2,3]	_ADC_DATA39_VECTOR	98	OFF098<17:1>	IFS3<2>	IEC3<2>	IPC24<20:18>	IPC24<17:16>	Yes
ADC Data 40[2,3]	_ADC_DATA40_VECTOR	99	OFF099<17:1>	IFS3<3>	IEC3<3>	IPC24<28:26>	IPC24<25:24>	Yes
ADC Data 41[2,3]	_ADC_DATA41_VECTOR	100	OFF100<17:1>	IFS3<4>	IEC3<4>	IPC25<4:2>	IPC25<1:0>	Yes
ADC Data 42[2,3]	_ADC_DATA42_VECTOR	101	OFF101<17:1>	IFS3<5>	IEC3<5>	IPC25<12:10>	IPC25<9:8>	Yes
ADC Data 43	_ADC_DATA43_VECTOR	102	OFF102<17:1>	IFS3<6>	IEC3<6>	IPC25<20:18>	IPC25<17:16>	Yes
ADC Data 44	_ADC_DATA44_VECTOR	103	OFF103<17:1>	IFS3<7>	IEC3<7>	IPC25<28:26>	IPC25<25:24>	Yes
Core Performance Counter Interrupt	_CORE_PERF_COUNT_VECTOR	104	OFF104<17:1>	IFS3<8>	IEC3<8>	IPC26<4:2>	IPC26<1:0>	No
Core Fast Debug Channel Interrupt	_CORE_FAST_DEBUG_CHAN_VECTOR	105	OFF105<17:1>	IFS3<9>	IEC3<9>	IPC26<12:10>	IPC26<9:8>	Yes

Note 1: Not all interrupt sources are available on all devices. See **TABLE 1: "PIC32MZ EF Family Features"** for the list of available peripherals.

2: This interrupt source is not available on 64-pin devices.

3: This interrupt source is not available on 100-pin devices.

4: This interrupt source is not available on 124-pin devices.

TABLE 7-3: INTERRUPT REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
07E0	OFF168	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07E4	OFF169	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07E8	OFF170	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07EC	OFF171	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07F0	OFF172	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07F4	OFF173	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07F8	OFF174	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07FC	OFF175	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0800	OFF176(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0804	OFF177(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0808	OFF178(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
080C	OFF179	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0810	OFF180	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0814	OFF181	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0818	OFF182	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 "CLR, SET, and INV Registers"** for more information.
2: This bit or register is not available on 64-pin devices.
3: This bit or register is not available on devices without a CAN module.
4: This bit or register is not available on 100-pin devices.
5: Bits 31 and 30 are not available on 64-pin and 100-pin devices; bits 29 through 14 are not available on 64-pin devices.
6: Bits 31, 30, 29, and bits 5 through 0 are not available on 64-pin and 100-pin devices; bit 31 is not available on 124-pin devices; bit 22 is not available on 64-pin devices.
7: This bit or register is not available on devices without a Crypto module.
8: This bit or register is not available on 124-pin devices.

REGISTER 8-4: REFOxCON: REFERENCE OSCILLATOR CONTROL REGISTER ('x' = 1-4)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	RODIV<14:8>						
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RODIV<7:0>							
15:8	R/W-0	U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0, HC	R-0, HS, HC
	ON(1)	—	SIDL	OE	RSLP(2)	—	DIVSWEN	ACTIVE(1)
7:0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	ROSEL<3:0>(3)			

Legend:	HC = Hardware Cleared	HS = Hardware Set	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **Unimplemented:** Read as '0'

bit 30-16 **RODIV<14:0>** Reference Clock Divider bits
The value selects the reference clock divider bits (see Figure 8-1 for details). A value of '0' selects no divider.

bit 15 **ON:** Output Enable bit(1)
1 = Reference Oscillator module is enabled
0 = Reference Oscillator module is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Peripheral Stop in Idle Mode bit
1 = Discontinue module operation when device enters Idle mode
0 = Continue module operation in Idle mode

bit 12 **OE:** Reference Clock Output Enable bit
1 = Reference clock is driven out on REFCLKOx pin
0 = Reference clock is not driven out on REFCLKOx pin

bit 11 **RSLP:** Reference Oscillator Module Run in Sleep bit(2)
1 = Reference Oscillator module output continues to run in Sleep
0 = Reference Oscillator module output is disabled in Sleep

bit 10 **Unimplemented:** Read as '0'

bit 9 **DIVSWEN:** Divider Switch Enable bit
1 = Divider switch is in progress
0 = Divider switch is complete

bit 8 **ACTIVE:** Reference Clock Request Status bit(1)
1 = Reference clock request is active
0 = Reference clock request is not active

bit 7-4 **Unimplemented:** Read as '0'

bit 3-0 **ROSEL<3:0>:** Reference Clock Source Select bits(3)
1111 = Reserved
•
•
•
1001 = BFRC
1000 = REFCLKIx
0111 = System PLL output
0110 = Reserved
0101 = SOSC
0100 = LPRC
0011 = FRC
0010 = POSC
0001 = PBCLK1
0000 = SYSCLK

Note 1: Do not write to this register when the ON bit is not equal to the ACTIVE bit.
2: This bit is ignored when the ROSEL<3:0> bits = 0000 or 0001.
3: The ROSEL<3:0> bits should not be written while the ACTIVE bit is '1', as undefined behavior may result.

REGISTER 11-12: USBFIFOx: USB FIFO DATA REGISTER 'x' ('x' = 0-7)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DATA<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DATA<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DATA<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DATA<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **DATA<31:0>:** USB Transmit/Receive FIFO Data bits

Writes to this register loads data into the TxFIFO for the corresponding endpoint. Reading from this register unloads data from the RxFIFO for the corresponding endpoint.

Transfers may be 8-bit, 16-bit or 32-bit as required, and any combination of access is allowed provided the data accessed is contiguous. However, all transfers associated with one packet must be of the same width so that data is consistently byte-, word- or double-word aligned. The last transfer may contain fewer bytes than the previous transfers in order to complete an odd-byte or odd-word transfer.

REGISTER 14-1: TxCON: TYPE B TIMER CONTROL REGISTER ('x' = 2-9)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
	ON(1)	—	SIDL(2)	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	U-0
	TGATE(1)	TCKPS<2:0>(1)			T32(3)	—	TCS(1)	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Timer On bit(1)
- 1 = Module is enabled
- 0 = Module is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit(2)
- 1 = Discontinue operation when device enters Idle mode
- 0 = Continue operation even in Idle mode

bit 12-8 **Unimplemented:** Read as '0'

bit 7 **TGATE:** Timer Gated Time Accumulation Enable bit(1)

When TCS = 1:
This bit is ignored and is read as '0'.

When TCS = 0:
- 1 = Gated time accumulation is enabled
- 0 = Gated time accumulation is disabled

bit 6-4 **TCKPS<2:0>:** Timer Input Clock Prescale Select bits(1)
- 111 = 1:256 prescale value
- 110 = 1:64 prescale value
- 101 = 1:32 prescale value
- 100 = 1:16 prescale value
- 011 = 1:8 prescale value
- 010 = 1:4 prescale value
- 001 = 1:2 prescale value
- 000 = 1:1 prescale value

bit 3 **T32:** 32-Bit Timer Mode Select bit(3)
- 1 = Odd numbered and even numbered timers form a 32-bit timer
- 0 = Odd numbered and even numbered timers form separate 16-bit timers

Note 1: While operating in 32-bit mode, this bit has no effect for odd numbered timers (Timer1, Timer3, Timer5, Timer7, and Timer9). All timer functions are set through the even numbered timers.

2: While operating in 32-bit mode, this bit must be cleared on odd numbered timers to enable the 32-bit timer in Idle mode.

3: This bit is available only on even numbered timers (Timer2, Timer4, Timer6, and Timer8).

REGISTER 15-7: DMTPSINTV: POST STATUS CONFIGURE DMT INTERVAL STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	PSINTV<31:24>							
23:16	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	PSINTV<23:16>							
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	PSINTV<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-y	R-y	R-y
	PSINTV<7:0>							

Legend:		y = Value set from Configuration bits on POR	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **PSINTV<31:0>:** DMT Window Interval Configuration Status bits
This is always the value of the DMTINTV<2:0> bits in the DEVCFG1 Configuration register.

25.0 REAL-TIME CLOCK AND CALENDAR (RTCC)

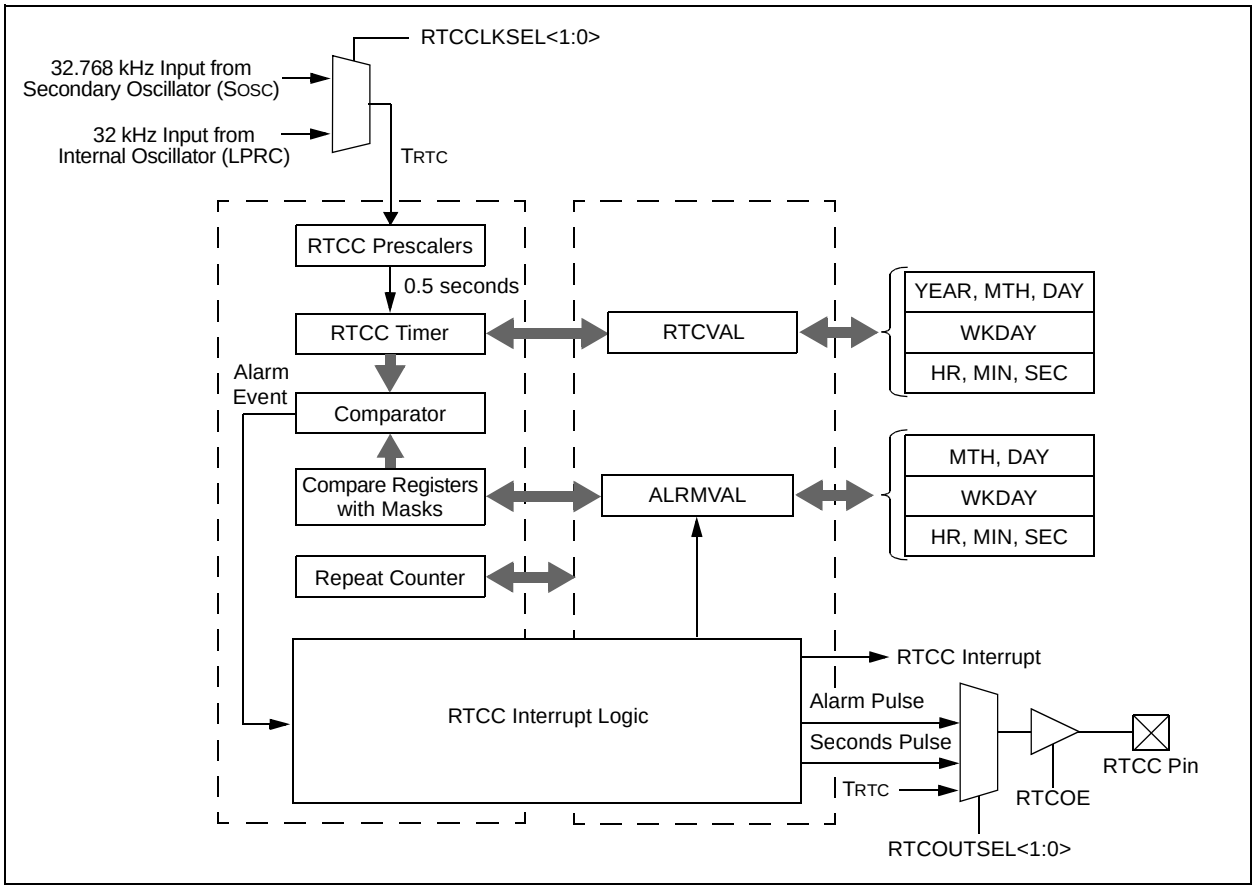
Note: This data sheet summarizes the features of the PIC32MZ EF family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 29. "Real-Time Clock and Calendar (RTCC)"** (DS60001125) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

The RTCC module is intended for applications in which accurate time must be maintained for extended periods of time with minimal or no CPU intervention. Low-power optimization provides extended battery lifetime while keeping track of time.

The following are key features of the RTCC module:

- Time: hours, minutes, and seconds
- 24-hour format (military time)
- Visibility of one-half second period
- Provides calendar: Weekday, date, month and year
- Alarm intervals are configurable for half of a second, one second, 10 seconds, one minute, 10 minutes, one hour, one day, one week, one month, and one year
- Alarm repeat with decrementing counter
- Alarm with indefinite repeat: Chime
- Year range: 2000 to 2099
- Leap year correction
- BCD format for smaller firmware overhead
- Optimized for long-term battery operation
- Fractional second synchronization
- User calibration of the clock crystal frequency with auto-adjust
- Calibration range: ±0.66 seconds error per month
- Calibrates up to 260 ppm of crystal error
- Uses external 32.768 kHz crystal or 32 kHz internal oscillator
- Alarm pulse, seconds clock, or internal clock output on RTCC pin

FIGURE 25-1: RTCC BLOCK DIAGRAM



REGISTER 26-1: CEVER: CRYPTO ENGINE REVISION, VERSION, AND ID REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	REVISION<7:0>							
23:16	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	VERSION<7:0>							
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	ID<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	ID<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-24 **REVISION<7:0>:** Crypto Engine Revision bits

bit 23-16 **VERSION<7:0>:** Crypto Engine Version bits

bit 15-0 **ID<15:0>:** Crypto Engine Identification bits

TABLE 28-1: ADC REGISTER MAP (CONTINUED)

Virtual Address (BF84_#)	Register Name	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
B280	ADCDATA32(1)	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
B284	ADCDATA33(1)	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
B288	ADCDATA34(1)	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
B28C	ADCDATA35(2)	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
B290	ADCDATA36(2)	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
B294	ADCDATA37(2)	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
B298	ADCDATA38(2)	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
B29C	ADCDATA39(2)	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
B2A0	ADCDATA40(2)	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
B2A4	ADCDATA41(2)	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
B2A8	ADCDATA42(2)	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
B2AC	ADCDATA43	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
B2B0	ADCDATA44	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000

Note 1: This bit or register is not available on 64-pin devices.
2: This bit or register is not available on 64-pin and 100-pin devices.
3: Before enabling the ADC, the user application must initialize the ADC calibration values by copying them from the factory-programmed DEVADCx Flash registers into the corresponding ADCxCFG registers.

REGISTER 28-3: ADCCON3: ADC CONTROL REGISTER 3

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ADCSEL<1:0>		CONCLKDIV<5:0>					
23:16	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DIGEN7	—	—	DIGEN4	DIGEN3	DIGEN2	DIGEN1	DIGEN0
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0, HS, HC	R/W-0	R-0, HS, HC
	VREFSEL<2:0>			TRGSUSP	UPDIEN	UPDRDY	SAMP(1,2,3,4)	RQCNVRT
7:0	R/W-0	R/W-0, HC	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	GLSWTRG	GSWTRG	ADINSEL<5:0>					

Legend:	HC = Hardware Set	HS = Hardware Cleared	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-30 **ADCSEL<1:0>:** Analog-to-Digital Clock Source (TCLK) bits
11 = FRC
10 = REFCLK3
01 = System Clock (Tcy)
00 = PBCLK3

bit 29-24 **CONCLKDIV<5:0>:** Analog-to-Digital Control Clock (TQ) Divider bits
111111 = 64 * TCLK = TQ
•
•
•
000011 = 4 * TCLK = TQ
000010 = 3 * TCLK = TQ
000001 = 2 * TCLK = TQ
000000 = TCLK = TQ

bit 23 **DIGEN7:** Shared ADC (ADC7) Digital Enable bit
1 = ADC7 is digital enabled
0 = ADC7 is digital disabled

bit 22-21 **Unimplemented:** Read as '0'

bit 20 **DIGEN4:** ADC4 Digital Enable bit
1 = ADC4 is digital enabled
0 = ADC4 is digital disabled

bit 19 **DIGEN3:** ADC3 Digital Enable bit
1 = ADC3 is digital enabled
0 = ADC3 is digital disabled

Note 1: The SAMP bit has the highest priority and setting this bit will keep the S&H circuit in Sample mode until the bit is cleared. Also, usage of the SAMP bit will cause settings of SAMC<9:0> bits (ADCCON2<25:16>) to be ignored.

2: The SAMP bit only connects Class 2 and Class 3 analog inputs to the shared ADC, ADC7. All Class 1 analog inputs are not affected by the SAMP bit.

3: The SAMP bit is not a self-clearing bit and it is the responsibility of application software to first clear this bit and only after setting the RQCNVRT bit to start the analog-to-digital conversion.

4: Normally, when the SAMP and RQCNVRT bits are used by software routines, all TRGSRCx<4:0> bits and STRGSRC<4:0> bits should be set to '00000' to disable all external hardware triggers and prevent them from interfering with the software-controlled sampling command signal SAMP and with the software-controlled trigger RQCNVRT.

REGISTER 28-23: ADCFIFO: ADC FIFO DATA REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	DATA<31:24>							
23:16	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	DATA<23:16>							
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	DATA<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	DATA<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **DATA<31:0>:** FIFO Data Output Value bits

Note: When an alternate input is used as the input source for a dedicated ADC module, the data output is still read from the Primary input Data Output Register.

REGISTER 29-10: CiFLTCON0: CAN FILTER CONTROL REGISTER 0 (CONTINUED)

bit 15 **FLTEN1:** Filter 1 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 14-13 **MSEL1<1:0>:** Filter 1 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 12-8 **FSEL1<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

bit 7 **FLTEN0:** Filter 0 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 6-5 **MSEL0<1:0>:** Filter 0 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 4-0 **FSEL0<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

Note: The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

REGISTER 29-22: CiFIFOUAn: CAN FIFO USER ADDRESS REGISTER 'n' ('n' = 0-31)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
	CiFIFOUAn<31:24>							
23:16	R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
	CiFIFOUAn<23:16>							
15:8	R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
	CiFIFOUAn<15:8>							
7:0	R-x	R-x	R-x	R-x	R-x	R-x	R-0(1)	R-0(1)
	CiFIFOUAn<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **CiFIFOUAn<31:0>:** CAN FIFO User Address bits

TXEN = 1: (FIFO configured as a Transmit Buffer)

A read of this register will return the address where the next message is to be written (FIFO head).

TXEN = 0: (FIFO configured as a Receive Buffer)

A read of this register will return the address where the next message is to be read (FIFO tail).

Note 1: This bit will always read '0', which forces byte-alignment of messages.

Note: This register is not guaranteed to read correctly in Configuration mode, and should only be accessed when the module is not in Configuration mode.

REGISTER 29-23: CiFIFOCIn: CAN MODULE MESSAGE INDEX REGISTER 'n' ('n' = 0-31)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	R-0	R-0	R-0	R-0	R-0
	—	—	—	CiFIFOCIn<4:0>				

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-5 **Unimplemented:** Read as '0'

bit 4-0 **CiFIFOCIn<4:0>:** CAN Side FIFO Message Index bits

TXEN = 1: (FIFO configured as a Transmit Buffer)

A read of this register will return an index to the message that the FIFO will next attempt to transmit.

TXEN = 0: (FIFO configured as a Receive Buffer)

A read of this register will return an index to the message that the FIFO will use to save the next message.

33.3.1 CONTROLLING CONFIGURATION CHANGES

Because peripherals can be disabled during run time, some restrictions on disabling peripherals are needed to prevent accidental configuration changes. PIC32MZ EF devices include two features to prevent alterations to enabled or disabled peripherals:

- Control register lock sequence
- Configuration bit select lock

33.3.1.1 Control Register Lock

Under normal operation, writes to the PMDx registers are not allowed. Attempted writes appear to execute normally, but the contents of the registers remain unchanged. To change these registers, they must be unlocked in hardware. The register lock is controlled by the PMDLOCK Configuration bit (CFGCON<12>). Setting PMDLOCK prevents writes to the control registers; clearing PMDLOCK allows writes.

To set or clear PMDLOCK, an unlock sequence must be executed. Refer to **Section 42. "Oscillators with Enhanced PLL"** (DS60001250) in the *"PIC32 Family Reference Manual"* for details.

33.3.1.2 Configuration Bit Select Lock

As an additional level of safety, the device can be configured to prevent more than one write session to the PMDx registers. The PMDL1WAY Configuration bit (DEVCFG3<28>) blocks the PMDLOCK bit from being cleared after it has been set once. If PMDLOCK remains set, the register unlock procedure does not execute, and the PPS control registers cannot be written to. The only way to clear the bit and re-enable PMD functionality is to perform a device Reset.

REGISTER 34-9: CFGEBIC: EXTERNAL BUS INTERFACE CONTROL PIN CONFIGURATION REGISTER (CONTINUED)

bit 12 **EBIOEEN:** $\overline{\text{EBIOE}}$ Pin Enable bit
1 = $\overline{\text{EBIOE}}$ pin is enabled for use by the EBI module
0 = $\overline{\text{EBIOE}}$ pin is available for general use

bit 11-10 **Unimplemented:** Read as '0'

bit 9 **EBIBSEN1:** $\overline{\text{EBIBS1}}$ Pin Enable bit
1 = $\overline{\text{EBIBS1}}$ pin is enabled for use by the EBI module
0 = $\overline{\text{EBIBS1}}$ pin is available for general use

bit 8 **EBIBSEN1:** $\overline{\text{EBIBS0}}$ Pin Enable bit
1 = $\overline{\text{EBIBS0}}$ pin is enabled for use by the EBI module
0 = $\overline{\text{EBIBS0}}$ pin is available for general use

bit 7 **EBICSEN3:** $\overline{\text{EBICS3}}$ Pin Enable bit
1 = $\overline{\text{EBICS3}}$ pin is enabled for use by the EBI module
0 = $\overline{\text{EBICS3}}$ pin is available for general use

bit 6 **EBICSEN2:** $\overline{\text{EBICS2}}$ Pin Enable bit
1 = $\overline{\text{EBICS2}}$ pin is enabled for use by the EBI module
0 = $\overline{\text{EBICS2}}$ pin is available for general use

bit 5 **EBICSEN1:** $\overline{\text{EBICS1}}$ Pin Enable bit
1 = $\overline{\text{EBICS1}}$ pin is enabled for use by the EBI module
0 = $\overline{\text{EBICS1}}$ pin is available for general use

bit 4 **EBICSEN0:** $\overline{\text{EBICS0}}$ Pin Enable bit
1 = $\overline{\text{EBICS0}}$ pin is enabled for use by the EBI module
0 = $\overline{\text{EBICS0}}$ pin is available for general use

bit 3-2 **Unimplemented:** Read as '0'

bit 1 **EBIDEN1:** EBI Data Upper Byte Pin Enable bit
1 = EBID<15:8> pins are enabled for use by the EBI module
0 = EBID<15:8> pins have reverted to general use

bit 0 **EBIDEN0:** EBI Data Lower Byte Pin Enable bit
1 = EBID<7:0> pins are enabled for use by the EBI module
0 = EBID<7:0> pins have reverted to general use

Note: When EBIMD = 1, the bits in this register are ignored and the pins are available for general use.

36.6 MPLAB X SIM Software Simulator

The MPLAB X SIM Software Simulator allows code development in a PC-hosted environment by simulating the PIC MCUs and dsPIC DSCs on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a comprehensive stimulus controller. Registers can be logged to files for further run-time analysis. The trace buffer and logic analyzer display extend the power of the simulator to record and track program execution, actions on I/O, most peripherals and internal registers.

The MPLAB X SIM Software Simulator fully supports symbolic debugging using the MPLAB XC Compilers, and the MPASM and MPLAB Assemblers. The software simulator offers the flexibility to develop and debug code outside of the hardware laboratory environment, making it an excellent, economical software development tool.

36.7 MPLAB REAL ICE In-Circuit Emulator System

The MPLAB REAL ICE In-Circuit Emulator System is Microchip's next generation high-speed emulator for Microchip Flash DSC and MCU devices. It debugs and programs all 8, 16 and 32-bit MCU, and DSC devices with the easy-to-use, powerful graphical user interface of the MPLAB X IDE.

The emulator is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with either a connector compatible with in-circuit debugger systems (RJ-11) or with the new high-speed, noise tolerant, Low-Voltage Differential Signal (LVDS) interconnection (CAT5).

The emulator is field upgradable through future firmware downloads in MPLAB X IDE. MPLAB REAL ICE offers significant advantages over competitive emulators including full-speed emulation, run-time variable watches, trace analysis, complex breakpoints, logic probes, a ruggedized probe interface and long (up to three meters) interconnection cables.

36.8 MPLAB ICD 3 In-Circuit Debugger System

The MPLAB ICD 3 In-Circuit Debugger System is Microchip's most cost-effective, high-speed hardware debugger/programmer for Microchip Flash DSC and MCU devices. It debugs and programs PIC Flash microcontrollers and dsPIC DSCs with the powerful, yet easy-to-use graphical user interface of the MPLAB IDE.

The MPLAB ICD 3 In-Circuit Debugger probe is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with a connector compatible with the MPLAB ICD 2 or MPLAB REAL ICE systems (RJ-11). MPLAB ICD 3 supports all MPLAB ICD 2 headers.

36.9 PICkit 3 In-Circuit Debugger/ Programmer

The MPLAB PICkit 3 allows debugging and programming of PIC and dsPIC Flash microcontrollers at a most affordable price point using the powerful graphical user interface of the MPLAB IDE. The MPLAB PICkit 3 is connected to the design engineer's PC using a full-speed USB interface and can be connected to the target via a Microchip debug (RJ-11) connector (compatible with MPLAB ICD 3 and MPLAB REAL ICE). The connector uses two device I/O pins and the Reset line to implement in-circuit debugging and In-Circuit Serial Programming™ (ICSP™).

36.10 MPLAB PM3 Device Programmer

The MPLAB PM3 Device Programmer is a universal, CE compliant device programmer with programmable voltage verification at V_{DDMIN} and V_{DDMAX} for maximum reliability. It features a large LCD display (128 x 64) for menus and error messages, and a modular, detachable socket assembly to support various package types. The ICSP cable assembly is included as a standard item. In Stand-Alone mode, the MPLAB PM3 Device Programmer can read, verify and program PIC devices without a PC connection. It can also set code protection in this mode. The MPLAB PM3 connects to the host PC via an RS-232 or USB cable. The MPLAB PM3 has high-speed communications and optimized algorithms for quick programming of large memory devices, and incorporates an MMC card for file storage and data applications.

TABLE 37-20: INTERNAL FRC ACCURACY

AC CHARACTERISTICS		Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Characteristics**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Internal FRC Accuracy @ 8.00 MHz(1)						
F20	FRC	-5	—	+5	%	0°C ≤ TA ≤ +85°C
		-8	—	+8	%	-40°C ≤ TA ≤ +85°C
		-10	—	+10	%	-40°C ≤ TA ≤ +125°C

Note 1: Frequency calibrated at +25°C and 3.3V. The TUN bits (OSCTUN<5:0>) can be used to compensate for temperature drift.

TABLE 37-21: INTERNAL LPRC ACCURACY

AC CHARACTERISTICS		Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Characteristics**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Internal LPRC @ 32.768 kHz(1)						
F21	LPRC	-8	—	+8	%	0°C ≤ TA ≤ +85°C
		-25	—	+25	%	-40°C ≤ TA ≤ +125°C

Note 1: Change of LPRC frequency as VDD changes.

TABLE 37-22: INTERNAL BACKUP FRC (BFRC) ACCURACY

AC CHARACTERISTICS		Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Characteristics**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Internal BFRC Accuracy @ 8 MHz						
F22	BFRC	—	±30	—	%	—

40.0 AC AND DC CHARACTERISTICS GRAPHS

Note: The graphs provided are a statistical summary based on a limited number of samples and are provided for design guidance purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore, outside the warranted range.

FIGURE 40-1: VOH – 4x DRIVER PINS

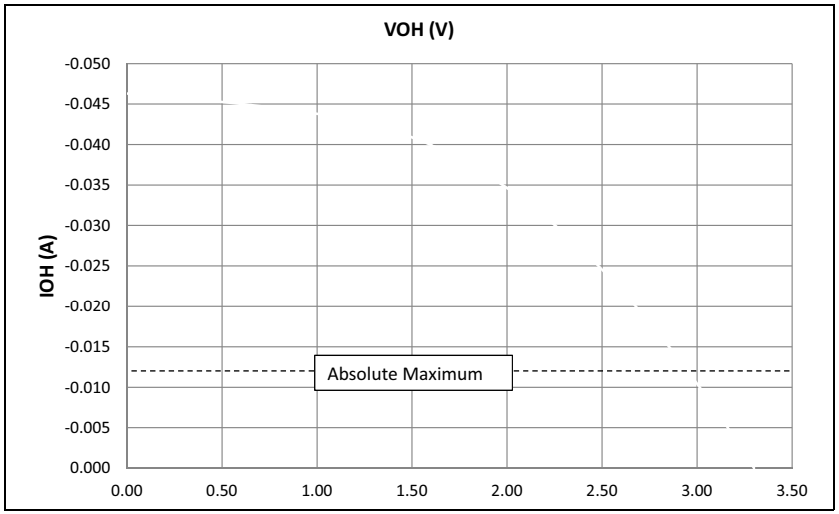


FIGURE 40-2: VOL – 4x DRIVER PINS

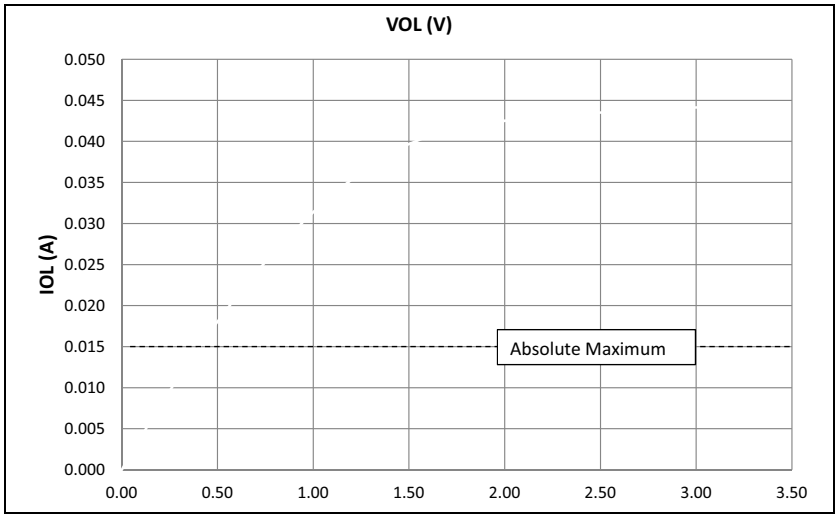


FIGURE 40-3: VOH – 8x DRIVER PINS

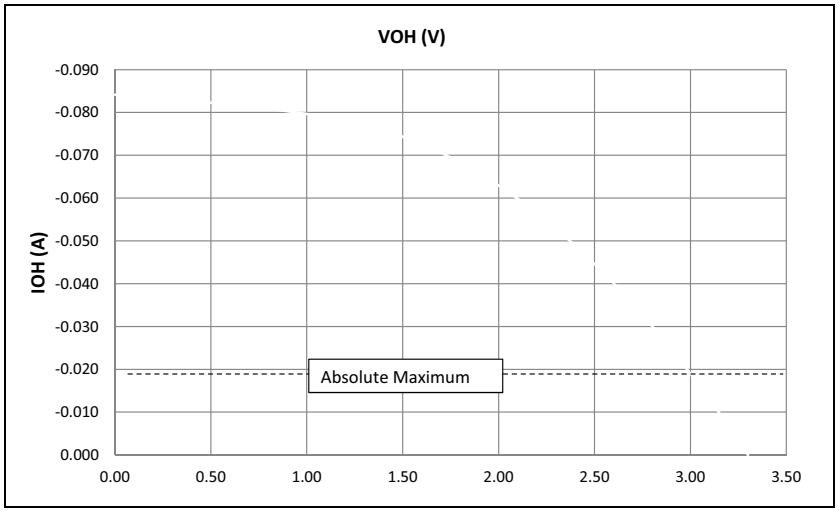


FIGURE 40-4: VOL – 8x DRIVER PINS