Microchip Technology - PIC32MZ2048EFH144-250I/PH Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® M-Class
Core Size	32-Bit Single-Core
Speed	252MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, PMP, SPI, SQI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	120
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	2.1V ~ 3.6V
Data Converters	A/D 48x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-TQFP
Supplier Device Package	144-TQFP (16x16)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mz2048efh144-250i-ph

3.0 CPU

Note 1: This data sheet summarizes the features of the PIC32MZ EF family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 50. "CPU for Devices with MIPS32® microAptiv™ and M-Class Cores"** (DS60001192) of the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

2: The Series 5 Warrior M-class CPU core resources are available at: www.imgtec.com.

The MIPS32® M-Class Core is the heart of the PIC32MZ EF family device processor. The CPU fetches instructions, decodes each instruction, fetches source operands, executes each instruction and writes the results of instruction execution to the proper destinations.

Key features include:

- 5-stage pipeline
- 32-bit address and data paths
- MIPS32 Enhanced Architecture (Release 5):
  - Multiply-accumulate and multiply-subtract instructions
  - Targeted multiply instruction
  - Zero/One detect instructions
  - `WAIT` instruction
  - Conditional move instructions (`MOVN`, `MOVZ`)
  - Vectored interrupts
  - Programmable exception vector base
  - Atomic interrupt enable/disable
  - GPR shadow registers to minimize latency for interrupt handlers
  - Bit field manipulation instructions
  - Virtual memory support
- microMIPS™ compatible instruction set:
  - Improves code size density over MIPS32, while maintaining MIPS32 performance.
  - Supports all MIPS32 instructions (except branch-likely instructions)
  - Fifteen additional 32-bit instructions and 39 16-bit instructions corresponding to commonly-used MIPS32 instructions
  - Stack pointer implicit in instruction
  - MIPS32 assembly and ABI compatible
- MMU with Translation Lookaside Buffer (TLB) mechanism:
  - 16 dual-entry fully associative Joint TLB
  - 4-entry fully associative Instruction and Data TLB
  - 4 KB pages
- Separate L1 data and instruction caches:
  - 16 KB 4-way Instruction Cache (I-Cache)
  - 4 KB 4-way Data Cache (D-Cache)
- Autonomous Multiply/Divide Unit (MDU):
  - Maximum issue rate of one 32x32 multiply per clock
  - Early-in iterative divide. Minimum 12 and maximum 38 clock latency (dividend (*rs*) sign extension-dependent)
- Power Control:
  - Minimum frequency: 0 MHz
  - Low-Power mode (triggered by `WAIT` instruction)
  - Extensive use of local gated clocks
- EJTAG Debug and Instruction Trace:
  - Support for single stepping
  - Virtual instruction and data address/value breakpoints
  - Hardware breakpoint supports both address match and address range triggering.
  - Eight instruction and four data complex breakpoints
- iFlowtrace® version 2.0 support:
  - Real-time instruction program counter
  - Special events trace capability
  - Two performance counters with 34 user-selectable countable events
  - Disabled if the processor enters Debug mode
  - Program Counter sampling
- Four Watch registers:
  - Instruction, Data Read, Data Write options
  - Address match masking options
- DSP ASE Extension:
  - Native fractional format data type operations
  - Register Single Instruction Multiple Data (SIMD) operations (add, subtract, multiply, shift)
  - GPR-based shift
  - Bit manipulation
  - Compare-Pick
  - DSP Control Access
  - Indexed-Load
  - Branch
  - Multiplication of complex operands
  - Variable bit insertion and extraction
  - Virtual circular buffers
  - Arithmetic saturation and overflow handling
  - Zero-cycle overhead saturation and rounding operations
- Floating Point Unit (FPU):
  - 1985 IEEE-754 compliant Floating Point Unit
  - Supports single and double precision datatypes
  - 2008 IEEE-754 compatibility control of NaN handling and Abs/Neg instructions
  - Runs at 1:1 core/FPU clock ratio

TABLE 7-1: MIPS32® M-CLASS MICROPROCESSOR CORE EXCEPTION TYPES (CONTINUED)

Exception Type (In Order of Priority)	Description	Branches to	Status Bits Set	Debug Bits Set	EXCCODE	XC32 Function Name
Instruction Validity Exceptions	An instruction could not be completed because it was not allowed to access the required resources (Coprocessor Unusable) or was illegal (Reserved Instruction). If both exceptions occur on the same instruction, the Coprocessor Unusable Exception takes priority over the Reserved Instruction Exception.	EBASE+0x180	EXL	—	0x0A or 0x0B	_general_exception_handler
Execute Exception	An instruction-based exception occurred: Integer overflow, trap, system call, breakpoint, floating point, or DSP ASE state disabled exception.	EBASE+0x180	EXL	—	0x08-0x0C	_general_exception_handler
Tr	Execution of a trap (when trap condition is true).	EBASE+0x180	EXL	—	0x0D	_general_exception_handler
DDBL/DDBS	EJTAG Data Address Break (address only) or EJTAG data value break on store (address + value).	0xBFC0_0480	—	DDBL or DDBS	—	—
WATCH	A reference to an address that is in one of the Watch registers (data).	EBASE+0x180	EXL	—	0x17	_general_exception_handler
AdEL	Load address alignment error. User mode load reference to kernel address.	EBASE+0x180	EXL	—	0x04	_general_exception_handler
AdES	Store address alignment error. User mode store to kernel address.	EBASE+0x180	EXL	—	0x05	_general_exception_handler
TLBL	Load TLB miss or load TLB hit to page with V = 0.	EBASE+0x180	EXL	—	0x02	_general_exception_handler
TLBS	Store TLB miss or store TLB hit to page with V = 0.	EBASE+0x180	EXL	—	0x03	_general_exception_handler
DBE	Load or store bus error.	EBASE+0x180	EXL	—	0x07	_general_exception_handler
DDBL	EJTAG data hardware breakpoint matched in load data compare.	0xBFC0_0480	—	DDBL	—	—
CBrk	EJTAG complex breakpoint.	0xBFC0_0480	—	DIBIMPR, DDBLIMPR, and/or DDBSIMPR	—	—
Lowest Priority						

TABLE 7-3: INTERRUPT REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0674	OFF077(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0678	OFF078(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
067C	OFF079(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0680	OFF080(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0684	OFF081(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0688	OFF082(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
068C	OFF083(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0690	OFF084(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0694	OFF085(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0698	OFF086(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
069C	OFF087(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
06A0	OFF088(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
06A4	OFF089(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
06A8	OFF090(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
06AC	OFF091(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 "CLR, SET, and INV Registers"** for more information.
2: This bit or register is not available on 64-pin devices.
3: This bit or register is not available on devices without a CAN module.
4: This bit or register is not available on 100-pin devices.
5: Bits 31 and 30 are not available on 64-pin and 100-pin devices; bits 29 through 14 are not available on 64-pin devices.
6: Bits 31, 30, 29, and bits 5 through 0 are not available on 64-pin and 100-pin devices; bit 31 is not available on 124-pin devices; bit 22 is not available on 64-pin devices.
7: This bit or register is not available on devices without a Crypto module.
8: This bit or register is not available on 124-pin devices.

REGISTER 8-8: CLKSTAT: OSCILLATOR CLOCK STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	R-0	R-0	U-0	R-0	R-0	R-0
	—	—	LPRCRDY	SOSCRDY	—	POSCRDY	DIVSPLLRDY	FRCRDY

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-6 **Unimplemented:** Read as '0'

bit 5 **LPRCRDY**: Low-Power RC (LPRC) Oscillator Ready Status bit
1 = LPRC is stable and ready
0 = LPRC is disabled or not operating

bit 4 **SOSCRDY:** Secondary Oscillator (SOSC) Ready Status bit
1 = SOSC is stable and ready
0 = SOSC is disabled or not operating

bit 3 **Unimplemented:** Read as '0'

bit 2 **POSCRDY:** Primary Oscillator (POSC) Ready Status bit
1 = POSC is stable and ready
0 = POSC is disabled or not operating

bit 1 **DIVSPLLRDY:** Divided System PLL Ready Status bit
1 = Divided System PLL is ready
0 = Divided System PLL is not ready

bit 0 **FRCRDY:** Fast RC (FRC) Oscillator Ready Status bit
1 = FRC is stable and ready
0 = FRC is disabled for not operating

REGISTER 11-5: USBIE0CSR0: USB INDEXED ENDPOINT CONTROL STATUS REGISTER 0 (ENDPOINT 0)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	R/W-0	R/W-0, HC	R/W-0	R/W-0, HC
	—	—	—	—	—	—	—	FLSHFIFO
					DISPING	DTWREN	DATATGGL	
23:16	R/W-0, HC	R/W-0, HC	R/W-0, HC	R/C-0, HS	R/W-0, HS	R-0, HS	R-0	R-0
	SVCSETEND	SVCRPR	SENDSTALL	SETUPEND	DATAEND	SENTSTALL	TXPKTRDY	RXPKTRDY
	NAKTMOUT	STATPKT	REQPKT	ERROR	SETUPPKT	RXSTALL		
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

Legend:	HC = Hardware Cleared	HS = Hardware Set	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-28 **Unimplemented:** Read as '0'

bit 27 **DISPING:** Disable Ping tokens control bit (*Host mode*)
1 = USB Module will not issue PING tokens in data and status phases of a Hi-Speed Control transfer
0 = Ping tokens are issued

bit 26 **DTWREN:** Data Toggle Write Enable bit (*Host mode*)
1 = Enable the current state of the Endpoint 0 data toggle to be written. Automatically cleared.
0 = Disable data toggle write

bit 25 **DATATGGL:** Data Toggle bit (*Host mode*)
When read, this bit indicates the current state of the Endpoint 0 data toggle.
If DTWREN = 1, this bit is writable with the desired setting.
If DTWREN = 0, this bit is read-only.

bit 24 **FLSHFIFO:** Flush FIFO Control bit
1 = Flush the next packet to be transmitted/read from the Endpoint 0 FIFO. The FIFO pointer is reset and the TXPKTRDY/RXPKTRDY bit is cleared. Automatically cleared when the operation completes. Should only be used when TXPKTRDY/RXPKTRDY = 1.
0 = No Flush operation

bit 23 **SVCSETEND:** Clear SETUPEND Control bit (*Device mode*)
1 = Clear the SETUPEND bit in this register. This bit is automatically cleared.
0 = Do not clear

NAKTMOUT: NAK Time-out Control bit (*Host mode*)
1 = Endpoint 0 is halted following the receipt of NAK responses for longer than the time set by the NAKLIM<4:0> bits (USBICSR<28:24>)
0 = Allow the endpoint to continue

bit 22 **SVCRPR:** Serviced RXPKTRDY Clear Control bit (*Device mode*)
1 = Clear the RXPKTRDY bit in this register. This bit is automatically cleared.
0 = Do not clear

STATPKT: Status Stage Transaction Control bit (*Host mode*)
1 = When set at the same time as the TXPKTRDY or REQPKT bit is set, performs a status stage transaction
0 = Do not perform a status stage transaction

REGISTER 15-7: DMTPSINTV: POST STATUS CONFIGURE DMT INTERVAL STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	PSINTV<31:24>							
23:16	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	PSINTV<23:16>							
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	PSINTV<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-y	R-y	R-y
	PSINTV<7:0>							

Legend:		y = Value set from Configuration bits on POR	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **PSINTV<31:0>:** DMT Window Interval Configuration Status bits
This is always the value of the DMTINTV<2:0> bits in the DEVCFG1 Configuration register.

REGISTER 16-1: WDTCON: WATCHDOG TIMER CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
	WDTCLRKEY<15:8>							
23:16	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
	WDTCLRKEY<7:0>							
15:8	R/W-y	U-0	U-0	R-y	R-y	R-y	R-y	R-y
	ON(1)	—	—	RUNDIV<4:0>				
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
	—	—	—	—	—	—	—	WDTWINEN

Legend:	y = Values set from Configuration bits on POR		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **WDTCLRKEY:** Watchdog Timer Clear Key bits
To clear the Watchdog Timer to prevent a time-out, software must write the value 0x5743 to this location using a single 16-bit write.

bit 15 **ON:** Watchdog Timer Enable bit(1)
1 = The WDT is enabled
0 = The WDT is disabled

bit 14-13 **Unimplemented:** Read as '0'

bit 12-8 **RUNDIV<4:0>:** Watchdog Timer Postscaler Value bits
On reset, these bits are set to the values of the WDTPS<4:0> Configuration bits in DEVCFG1.

bit 7-1 **Unimplemented:** Read as '0'

bit 0 **WDTWINEN:** Watchdog Timer Window Enable bit
1 = Enable windowed Watchdog Timer
0 = Disable windowed Watchdog Timer

Note 1: This bit only has control when the FWDTEN bit (DEVCFG1<23>) = 0.

NOTES:

REGISTER 20-1: SQI1XCON1: SQI XIP CONTROL REGISTER 1 (CONTINUED)

bit 5-4 **TYPEMODE<1:0>:** SQI Type Mode Enable bits

The boot controller will send the mode in Single Lane, Dual Lane, or Quad Lane.

11 = Reserved
10 = Quad Lane mode is enabled
01 = Dual Lane mode is enabled
00 = Single Lane mode is enabled

bit 3-2 **TYPEADDR<1:0>:** SQI Type Address Enable bits

The boot controller will send the address in Single Lane, Dual Lane, or Quad Lane.

11 = Reserved
10 = Quad Lane mode address is enabled
01 = Dual Lane mode address is enabled
00 = Single Lane mode address is enabled

bit 1-0 **TYPECMD<1:0>:** SQI Type Command Enable bits

The boot controller will send the command in Single Lane, Dual Lane, or Quad Lane.

11 = Reserved
10 = Quad Lane mode command is enabled
01 = Dual Lane mode command is enabled
00 = Single Lane mode command is enabled

NOTES:

FIGURE 26-2: FORMAT OF BD_CTRL

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31-24	DESC_EN	—	CRY_MODE<2:0>			—	—	—
23-16	—	SA_ FETCH_EN	—	—	LAST_BD	LIFM	PKT_ INT_EN	CBD_ INT_EN
15-8	BD_BUFLEN<15:8>							
7-0	BD_BUFLEN<7:0>							

bit 31 **DESC_EN**: Descriptor Enable
1 = The descriptor is owned by hardware. After processing the BD, hardware resets this bit to '0'.
0 = The descriptor is owned by software

bit 30 **Unimplemented:** Must be written as '0'

bit 29-27 **CRY_MODE<2:0>:** Crypto Mode
111 = Reserved
110 = Reserved
101 = Reserved
100 = Reserved
011 = CEK operation
010 = KEK operation
001 = Preboot authentication
000 = Normal operation

bit 22 **SA_FETCH_EN:** Fetch Security Association From External Memory
1 = Fetch SA from the SA pointer. This bit needs to be set to '1' for every new packet.
0 = Use current fetched SA or the internal SA

bit 21-20 **Unimplemented:** Must be written as '0'

bit 19 **LAST_BD:** Last Buffer Descriptors
1 = Last Buffer Descriptor in the chain
0 = More Buffer Descriptors in the chain
After the last BD, the CEBDADDR goes to the base address in CEBDPADDR.

bit 18 **LIFM:** Last In Frame
In case of Receive Packets (from H/W-> Host), this field is filled by the Hardware to indicate whether the packet goes across multiple buffer descriptors. In case of transmit packets (from Host -> H/W), this field indicates whether this BD is the last in the frame.

bit 17 **PKT_INT_EN:** Packet Interrupt Enable
Generate an interrupt after processing the current buffer descriptor, if it is the end of the packet.

bit 16 **CBD_INT_EN:** CBD Interrupt Enable
Generate an interrupt after processing the current buffer descriptor.

bit 15-0 **BD_BUFLEN<15:0>:** Buffer Descriptor Length
This field contains the length of the buffer and is updated with the actual length filled by the receiver.

FIGURE 26-3: FORMAT OF BD_SADDR

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31-24	BD_SAADDR<31:24>							
23-16	BD_SAADDR<23:16>							
15-8	BD_SAADDR<15:8>							
7-0	BD_SAADDR<7:0>							

bit 31-0 **BD_SAADDR<31:0>:** Security Association IP Session Address
The sessions' SA pointer has the keys and IV values.

REGISTER 28-17: ADCTRG1: ADC TRIGGER SOURCE 1 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	TRGSRC3<4:0>				
23:16	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	TRGSRC2<4:0>				
15:8	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	TRGSRC1<4:0>				
7:0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	TRGSRC0<4:0>				

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-29 **Unimplemented:** Read as '0'

bit 28-24 **TRGSRC3<4:0>:** Trigger Source for Conversion of Analog Input AN3 Select bits
11111 = Reserved
•
•
•
01101 = Reserved
01100 = Comparator 2 (COUT)
01011 = Comparator 1 (COUT)
01010 = OCMP5
01001 = OCMP3
01000 = OCMP1
00111 = TMR5 match
00110 = TMR3 match
00101 = TMR1 match
00100 = INT0 External interrupt
00011 = STRIG
00010 = Global level software trigger (GLSWTRG)
00001 = Global software edge Trigger (GSWTRG)
00000 = No Trigger

For STRIG, in addition to setting the trigger, it also requires programming of the STRGSRC<4:0> bits (ADCCON1<20:16>) to select the trigger source, and requires the appropriate CSS bits to be set in the ADCCSS*x* registers.

bit 23-21 **Unimplemented:** Read as '0'

bit 20-16 **TRGSRC2<4:0>:** Trigger Source for Conversion of Analog Input AN2 Select bits
See bits 28-24 for bit value definitions.

bit 15-13 **Unimplemented:** Read as '0'

bit 12-8 **TRGSRC1<4:0>:** Trigger Source for Conversion of Analog Input AN1 Select bits
See bits 28-24 for bit value definitions.

bit 7-5 **Unimplemented:** Read as '0'

bit 4-0 **TRGSRC0<4:0>:** Trigger Source for Conversion of Analog Input AN0 Select bits
See bits 28-24 for bit value definitions.

REGISTER 29-3: CiINT: CAN INTERRUPT REGISTER (CONTINUED)

bit 14 **WAKIF:** CAN Bus Activity Wake-up Interrupt Flag bit
1 = A bus wake-up activity interrupt has occurred
0 = A bus wake-up activity interrupt has not occurred

bit 13 **CERRIF:** CAN Bus Error Interrupt Flag bit
1 = A CAN bus error has occurred
0 = A CAN bus error has not occurred

bit 12 **SERRIF:** System Error Interrupt Flag bit
1 = A system error occurred (typically an illegal address was presented to the System Bus)
0 = A system error has not occurred

bit 11 **RBOVIF:** Receive Buffer Overflow Interrupt Flag bit
1 = A receive buffer overflow has occurred
0 = A receive buffer overflow has not occurred

bit 10-4 **Unimplemented:** Read as '0'

bit 3 **MODIF:** CAN Mode Change Interrupt Flag bit
1 = A CAN module mode change has occurred (OPMOD<2:0> has changed to reflect REQOP)
0 = A CAN module mode change has not occurred

bit 2 **CTMRIF:** CAN Timer Overflow Interrupt Flag bit
1 = A CAN timer (CANTMR) overflow has occurred
0 = A CAN timer (CANTMR) overflow has not occurred

bit 1 **RBIF:** Receive Buffer Interrupt Flag bit
1 = A receive buffer interrupt is pending
0 = A receive buffer interrupt is not pending

bit 0 **TBIF:** Transmit Buffer Interrupt Flag bit
1 = A transmit buffer interrupt is pending
0 = A transmit buffer interrupt is not pending

Note 1: This bit can only be cleared by turning the CAN module off and on by clearing or setting the ON bit (CiCON<15>).

REGISTER 30-13: ETHIEN: ETHERNET CONTROLLER INTERRUPT ENABLE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	R/W-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0
	—	TXBUSEIE(1)	RXBUSEIE(2)	—	—	—	EWMARKIE(2)	FWMARKIE(2)
7:0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	RXDONEIE(2)	PKTPENDIE(2)	RXACTIE(2)	—	TXDONEIE(1)	TXABORTIE(1)	RXBUFNAIE(2)	RXOVFLWIE(2)

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-15 **Unimplemented:** Read as '0'

bit 14 **TXBUSEIE:** Transmit BVCI Bus Error Interrupt Enable bit(1)
1 = Enable TXBUS Error Interrupt
0 = Disable TXBUS Error Interrupt

bit 13 **RXBUSEIE:** Receive BVCI Bus Error Interrupt Enable bit(2)
1 = Enable RXBUS Error Interrupt
0 = Disable RXBUS Error Interrupt

bit 12-10 **Unimplemented:** Read as '0'

bit 9 **EWMARKIE:** Empty Watermark Interrupt Enable bit(2)
1 = Enable EWMARK Interrupt
0 = Disable EWMARK Interrupt

bit 8 **FWMARKIE:** Full Watermark Interrupt Enable bit(2)
1 = Enable FWMARK Interrupt
0 = Disable FWMARK Interrupt

bit 7 **RXDONEIE:** Receiver Done Interrupt Enable bit(2)
1 = Enable RXDONE Interrupt
0 = Disable RXDONE Interrupt

bit 6 **PKTPENDIE:** Packet Pending Interrupt Enable bit(2)
1 = Enable PKTPEND Interrupt
0 = Disable PKTPEND Interrupt

bit 5 **RXACTIE:** RX Activity Interrupt Enable bit
1 = Enable RXACT Interrupt
0 = Disable RXACT Interrupt

bit 4 **Unimplemented:** Read as '0'

bit 3 **TXDONEIE:** Transmitter Done Interrupt Enable bit(1)
1 = Enable TXDONE Interrupt
0 = Disable TXDONE Interrupt

bit 2 **TXABORTIE:** Transmitter Abort Interrupt Enable bit(1)
1 = Enable TXABORT Interrupt
0 = Disable TXABORT Interrupt

bit 1 **RXBUFNAIE:** Receive Buffer Not Available Interrupt Enable bit(2)
1 = Enable RXBUFNA Interrupt
0 = Disable RXBUFNA Interrupt

bit 0 **RXOVFLWIE:** Receive FIFO Overflow Interrupt Enable bit(2)
1 = Enable RXOVFLW Interrupt
0 = Disable RXOVFLW Interrupt

Note 1: This bit is only used for TX operations.
2: This bit is only used for RX operations.

REGISTER 34-1: DEVSIGN0/ADEVSIGN0: DEVICE SIGNATURE WORD 0 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	r-0	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—
23:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—
15:8	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—
7:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—

Legend:	r = Reserved bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **Reserved:** Write as '0'

bit 30-0 **Reserved:** Write as '1'

Note: The DEVSIGN1 through DEVSIGN3 and ADEVSIGN1 through ADEVSIGN3 registers are used for Quad Word programming operation when programming the DEVSIGN0/ADESIGN0 registers, and do not contain any valid information.

REGISTER 34-2: DEVCP0/ADEVCP0: DEVICE CODE-PROTECT 0 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	r-1	r-1	r-1	R/P	r-1	r-1	r-1	r-1
	—	—	—	CP	—	—	—	—
23:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—
15:8	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—
7:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—

Legend:	r = Reserved bit	P = Programmable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-29 **Reserved:** Write as '1'

bit 28 **CP:** Code-Protect bit

Prevents boot and program Flash memory from being read or modified by an external programming device.
1 = Protection is disabled
0 = Protection is enabled

bit 27-0 **Reserved:** Write as '1'

Note: The DEVCP1 through DEVCP3 and ADEVCP1 through ADEVCP3 registers are used for Quad Word programming operation when programming the DEVCP0/ADEVCP0 registers, and do not contain any valid information.

REGISTER 34-4: DEVCFG1/ADEVCFG1: DEVICE CONFIGURATION WORD 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/P	R/P	R/P	R/P	R/P	R/P	R/P	R/P
	FDMTEN	DMTCNT<4:0>					FWDTWINSZ<1:0>	
23:16	R/P	R/P	R/P	R/P	R/P	R/P	R/P	R/P
	FWDTEN	WINDIS	WDTSPGM	WDTPS<4:0>				
15:8	R/P	R/P	r-1	r-1	r-1	R/P	R/P	R/P
	FCKSM<1:0>		—	—	—	OSCIOFNC	POSCMOD<1:0>	
7:0	R/P	R/P	R/P	R/P	R/P	R/P	R/P	R/P
	IESO	FSOSCEN	DMTINTV<2:0>			FNOSC<2:0>		

Legend:	r = Reserved bit	P = Programmable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **FDMTEN:** Deadman Timer enable bit
1 = Deadman Timer is enabled and *cannot* be disabled by software
0 = Deadman Timer is disabled and *can* be enabled by software

bit 30-26 **DMTCNT<4:0>:** Deadman Timer Count Select bits
11111 = Reserved
•
•
•
11000 = Reserved
10111 = 2^{31} (2147483648)
10110 = 2^{30} (1073741824)
10101 = 2^{29} (536870912)
10100 = 2^{28} (268435456)
•
•
•
00001 = 2^{9} (512)
00000 = 2^{8} (256)

bit 25-24 **FWDTWINSZ<1:0>:** Watchdog Timer Window Size bits
11 = Window size is 25%
10 = Window size is 37.5%
01 = Window size is 50%
00 = Window size is 75%

bit 23 **FWDTEN:** Watchdog Timer Enable bit
1 = Watchdog Timer is enabled and cannot be disabled by software
0 = Watchdog Timer is not enabled; it can be enabled in software

bit 22 **WINDIS:** Watchdog Timer Window Enable bit
1 = Watchdog Timer is in non-Window mode
0 = Watchdog Timer is in Window mode

bit 21 **WDTSPGM:** Watchdog Timer Stop During Flash Programming bit
1 = Watchdog Timer stops during Flash programming
0 = Watchdog Timer runs during Flash programming (for read/execute while programming Flash applications)

TABLE 37-20: INTERNAL FRC ACCURACY

AC CHARACTERISTICS		Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Characteristics**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Internal FRC Accuracy @ 8.00 MHz(1)						
F20	FRC	-5	—	+5	%	0°C ≤ TA ≤ +85°C
		-8	—	+8	%	-40°C ≤ TA ≤ +85°C
		-10	—	+10	%	-40°C ≤ TA ≤ +125°C

Note 1: Frequency calibrated at +25°C and 3.3V. The TUN bits (OSCTUN<5:0>) can be used to compensate for temperature drift.

TABLE 37-21: INTERNAL LPRC ACCURACY

AC CHARACTERISTICS		Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Characteristics**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Internal LPRC @ 32.768 kHz(1)						
F21	LPRC	-8	—	+8	%	0°C ≤ TA ≤ +85°C
		-25	—	+25	%	-40°C ≤ TA ≤ +125°C

Note 1: Change of LPRC frequency as VDD changes.

TABLE 37-22: INTERNAL BACKUP FRC (BFRC) ACCURACY

AC CHARACTERISTICS		Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Characteristics**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Internal BFRC Accuracy @ 8 MHz						
F22	BFRC	—	±30	—	%	—

TABLE 37-40: ADC SAMPLE TIMES WITH CVD ENABLED

AC CHARACTERISTICS[2]			Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Symbol**	**Characteristics**	**Min.**	**Typ.[1]**	**Max.**	**Units**	**Conditions**
AD60a	TSAMP	Sample Time for ADC7 (Class 2 and Class 3 Inputs) with the CVDEN bit (ADCCON1<11>) = 1	8 9 11 12 14 16 17	—	—	TAD	Source Impedance ≤ 200Ω CVDCPL<2:0> (ADCCON2<28:26>) = 001 CVDCPL<2:0> (ADCCON2<28:26>) = 010 CVDCPL<2:0> (ADCCON2<28:26>) = 011 CVDCPL<2:0> (ADCCON2<28:26>) = 100 CVDCPL<2:0> (ADCCON2<28:26>) = 101 CVDCPL<2:0> (ADCCON2<28:26>) = 110 CVDCPL<2:0> (ADCCON2<28:26>) = 111
			10 12 14 16 18 19 21	—	—	TAD	Source Impedance ≤ 500Ω CVDCPL<2:0> (ADCCON2<28:26>) = 001 CVDCPL<2:0> (ADCCON2<28:26>) = 010 CVDCPL<2:0> (ADCCON2<28:26>) = 011 CVDCPL<2:0> (ADCCON2<28:26>) = 100 CVDCPL<2:0> (ADCCON2<28:26>) = 101 CVDCPL<2:0> (ADCCON2<28:26>) = 110 CVDCPL<2:0> (ADCCON2<28:26>) = 111
			13 16 18 21 23 26 28	—	—	TAD	Source Impedance ≤ 1 KΩ CVDCPL<2:0> (ADCCON2<28:26>) = 001 CVDCPL<2:0> (ADCCON2<28:26>) = 010 CVDCPL<2:0> (ADCCON2<28:26>) = 011 CVDCPL<2:0> (ADCCON2<28:26>) = 100 CVDCPL<2:0> (ADCCON2<28:26>) = 101 CVDCPL<2:0> (ADCCON2<28:26>) = 110 CVDCPL<2:0> (ADCCON2<28:26>) = 111
			41 48 56 63 70 78 85	—	—	TAD	Source Impedance ≤ 5 KΩ CVDCPL<2:0> (ADCCON2<28:26>) = 001 CVDCPL<2:0> (ADCCON2<28:26>) = 010 CVDCPL<2:0> (ADCCON2<28:26>) = 011 CVDCPL<2:0> (ADCCON2<28:26>) = 100 CVDCPL<2:0> (ADCCON2<28:26>) = 101 CVDCPL<2:0> (ADCCON2<28:26>) = 110 CVDCPL<2:0> (ADCCON2<28:26>) = 111

Note 1: These parameters are characterized, but not tested in manufacturing.

2: The ADC module is functional at VBORMIN < VDD < VDDMIN, but with degraded performance. Unless otherwise stated, module functionality is guaranteed, but not characterized.

39.2 AC Characteristics and Timing Parameters

The information contained in this section defines PIC32MZ EF device AC characteristics and timing parameters.

TABLE 39-5: SYSTEM TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param. No.	**Symbol**	**Characteristics**	**Minimum**	**Typical**	**Maximum**	**Units**	**Conditions**
MOS51	FSYS	System Frequency	DC	—	252	MHz	USB module disabled
			60	—	252	MHz	USB module enabled
MOS55a	FPB	Peripheral Bus Frequency	DC	—	100	MHz	For PBCLKx, 'x' ≠ 4, 7 (see **Note 1**)
MOS55b			DC	—	200	MHz	For PBCLK4
MOS55c			DC	—	252	MHz	For PBCLK7
MOS56	FREF	Reference Clock Frequency	—	—	50	MHz	For REFCLKI1, 3, 4 and REFCLKO1, 3, 4 pins

Note 1: If the DEVCFG registers are configured for a SYSCLK speed greater than 200 MHz, these PBCLKs will be running faster than the maximum rating when the device comes out of Reset. To ensure proper operation, firmware must start the device at a speed less than or equal to 200 MHz, adjust the speed of the PBCLKs, and then raise the SYSCLK speed to the desired speed.

TABLE 39-6: PLL CLOCK TIMING SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typical**	**Max.**	**Units**	**Conditions**
MOS54a	FPLL	PLL Output Frequency Range	10	—	252	MHz	—

Note 1: These parameters are characterized, but not tested in manufacturing.

2: This jitter specification is based on clock-cycle by clock-cycle measurements. To get the effective jitter for individual time-bases on communication clocks, use the following formula:

$$EffectiveJitter = \frac{D_{CLK}}{\sqrt{\frac{PBCLK2}{CommunicationClock}}}$$

For example, if PBCLK2 = 100 MHz and SPI bit rate = 50 MHz, the effective jitter is as follows:

$$EffectiveJitter = \frac{D_{CLK}}{\sqrt{\frac{100}{50}}} = \frac{D_{CLK}}{1.41}$$

B.12 Crypto Engine

Table B-7 lists the changes available for the Crypto Engine.

TABLE B-7: CRYPTO DIFFERENCES

PIC32MZ EC Feature	PIC32MZ EF Feature
Output Data Format	
On PIC32MZ EC devices, the output of the Crypto Engine is always in big-endian format, usually requiring a software (or DMA) solution to put the data into little-endian format, which the core handles natively.	On PIC32MZ EF devices, the SWAPOEN bit (CECON<7>) has been added to control output byte swapping. This bit, when enabled, will byte-swap the output.

B.13 Device Configuration and Control

A number of enhancements have been added to the PIC32MZ EF devices that allow greater control and flexibility on the device. Some bit fields have also changed location. Table B-8 lists these changes.

TABLE B-8: DEVICE CONFIGURATION AND CONTROL DIFFERENCES

PIC32MZ EC Feature	PIC32MZ EF Feature
MCLR Pin Configuration	
On PIC32MZ EC devices, the MCLR pin always generate a system reset.	On PIC32MZ EF devices, the $\overline{\text{MCLR}}$ pin can now be configured to generate either a system Reset or an emulated POR Reset. SMCLR (DEVCFG0<15>) 1 = MCLR pin generates a normal system Reset 0 = MCLR pin generates an emulated POR Reset
I/O Analog Charge Pump	
Low V_{DD} environments cause attenuation of analog inputs.	A new bit enables an I/O charge pump, which improves analog performance when operating at lower V_{DD}. IOANCPEN (CFGCON<7>) 1 = Charge pump is enabled 0 = Charge pump is disabled
EBI Ready Pin Control	
EBIRDYINV<3:1> (CFGEBIC<30:28>) EBIRDYEN<3:1> (CFGEBIC<26:24>)	The EBIRDY control bits have been moved. EBIRDYINV<3:1> (CFGEBIC<31:29>) EBIRDYEN<3:1> (CFGEBIC<27:25>)
Boot Flash Sequence Control	
On PIC32MZ EC devices, the Boot Flash Sequence (specifying which boot memory was mapped to the lower boot alias) was determined with the BFxSEQ0 registers.	On PIC32MZ EF devices, the Boot Flash Sequence has been moved to the BFxSEQ3 register.