Microchip Technology - PIC32MZ2048EFH144T-250I/JWX Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® M-Class
Core Size	32-Bit Single-Core
Speed	252MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, PMP, SPI, SQI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	120
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	2.1V ~ 3.6V
Data Converters	A/D 48x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-TFBGA
Supplier Device Package	144-TFBGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mz2048efh144t-250i-jwx

TABLE 4-10: SYSTEM BUS TARGET 2 REGISTER MAP

Virtual Address (BF8F_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
8820	SBT2ELOG1	31:16	MULTI	—	—	—	CODE<3:0>				—	—	—	—	—	—	—	—	0000
		15:0	INITID<7:0>								REGION<3:0>				—	CMD<2:0>			0000
8824	SBT2ELOG2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	GROUP<1:0>		0000
8828	SBT2ECON	31:16	—	—	—	—	—	—	—	ERRP	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
8830	SBT2ECLRS	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
8838	SBT2ECLRM	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
8840	SBT2REG0	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
8850	SBT2RD0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8858	SBT2WR0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8860	SBT2REG1	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
8870	SBT2RD1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8878	SBT2WR1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8880	SBT2REG2	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
8890	SBT2RD2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8898	SBT2WR2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.
Note: For reset values listed as 'xxxx', please refer to Table 4-6 for the actual reset values.

REGISTER 7-2: PRISS: PRIORITY SHADOW SELECT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PRI7SS<3:0>(1)				PRI6SS<3:0>(1)			
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PRI5SS<3:0>(1)				PRI4SS<3:0>(1)			
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PRI3SS<3:0>				PRI2SS<3:0>(1)			
7:0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	R/W-0
	PRI1SS<3:0>(1)				—	—	—	SS0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-28 **PRI7SS<3:0>:** Interrupt with Priority Level 7 Shadow Set bits(1)
1xxx = Reserved (by default, an interrupt with a priority level of 7 uses Shadow Set 0)
0111 = Interrupt with a priority level of 7 uses Shadow Set 7
0110 = Interrupt with a priority level of 7 uses Shadow Set 6
•
•
•
0001 = Interrupt with a priority level of 7 uses Shadow Set 1
0000 = Interrupt with a priority level of 7 uses Shadow Set 0

bit 27-24 **PRI6SS<3:0>:** Interrupt with Priority Level 6 Shadow Set bits(1)
1xxx = Reserved (by default, an interrupt with a priority level of 6 uses Shadow Set 0)
0111 = Interrupt with a priority level of 6 uses Shadow Set 7
0110 = Interrupt with a priority level of 6 uses Shadow Set 6
•
•
•
0001 = Interrupt with a priority level of 6 uses Shadow Set 1
0000 = Interrupt with a priority level of 6 uses Shadow Set 0

bit 23-20 **PRI5SS<3:0>:** Interrupt with Priority Level 5 Shadow Set bits(1)
1xxx = Reserved (by default, an interrupt with a priority level of 5 uses Shadow Set 0)
0111 = Interrupt with a priority level of 5 uses Shadow Set 7
0110 = Interrupt with a priority level of 5 uses Shadow Set 6
•
•
•
0001 = Interrupt with a priority level of 5 uses Shadow Set 1
0000 = Interrupt with a priority level of 5 uses Shadow Set 0

bit 19-16 **PRI4SS<3:0>:** Interrupt with Priority Level 4 Shadow Set bits(1)
1xxx = Reserved (by default, an interrupt with a priority level of 4 uses Shadow Set 0)
0111 = Interrupt with a priority level of 4 uses Shadow Set 7
0110 = Interrupt with a priority level of 4 uses Shadow Set 6
•
•
•
0001 = Interrupt with a priority level of 4 uses Shadow Set 1
0000 = Interrupt with a priority level of 4 uses Shadow Set 0

Note 1: These bits are ignored if the MVEC bit (INTCON<12>) = 0.

TABLE 10-3: DMA CHANNEL 0 THROUGH CHANNEL 7 REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
15B0	DCH7ECON	31:16	—	—	—	—	—	—	—	—	CHAIRQ<7:0>								00FF
		15:0	CHSIRQ<7:0>								CFORCE	CABORT	PATEN	SIRQEN	AIRQEN	—	—	—	FF00
15C0	DCH7INT	31:16	—	—	—	—	—	—	—	—	CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE	CHERIE	0000
		15:0	—	—	—	—	—	—	—	—	CHSDIF	CHSHIF	CHDDIF	CHDHIF	CHBCIF	CHCCIF	CHTAIF	CHERIF	0000
15D0	DCH7SSA	31:16	CHSSA<31:0>																0000
		15:0																	0000
15E0	DCH7DSA	31:16	CHDSA<31:0>																0000
		15:0																	0000
15F0	DCH7SSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSSIZ<15:0>																0000
1600	DCH7DSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDSIZ<15:0>																0000
1610	DCH7SPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSPTR<15:0>																0000
1620	DCH7DPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDPTR<15:0>																0000
1630	DCH7CSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCSIZ<15:0>																0000
1640	DCH7CPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCPTR<15:0>																0000
1650	DCH7DAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHPDAT<15:0>																0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 "CLR, SET, and INV Registers"** for more information.

REGISTER 21-2: I2CxSTAT: I^{2}C STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R-0, HS, HC	R-0, HS, HC	R/C-0, HS, HC	U-0	U-0	R/C-0, HS	R-0, HS, HC	R-0, HS, HC
	ACKSTAT	TRSTAT	ACKTIM	—	—	BCL	GCSTAT	ADD10
7:0	R/C-0, HS, SC	R/C-0, HS, SC	R-0, HS, HC	R/C-0, HS, HC	R/C-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	IWCOL	I2COV	D_A	P	S	R_W	RBF	TBF

Legend:	HS = Hardware Set	HC = Hardware Cleared	SC = Software Cleared
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	C = Clearable bit

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ACKSTAT:** Acknowledge Status bit
(when operating as I^{2}C master, applicable to master transmit operation)
1 = NACK received from slave
0 = ACK received from slave
Hardware set or clear at end of slave Acknowledge.

bit 14 **TRSTAT:** Transmit Status bit (when operating as I^{2}C master, applicable to master transmit operation)
1 = Master transmit is in progress (8 bits + ACK)
0 = Master transmit is not in progress
Hardware set at beginning of master transmission. Hardware clear at end of slave Acknowledge.

bit 13 **ACKTIM:** Acknowledge Time Status bit (Valid in I^{2}C Slave mode only)
1 = I^{2}C bus is in an Acknowledge sequence, set on the eight falling edge of SCL clock
0 = Not an Acknowledge sequence, cleared on 9th rising edge of SCL clock

bit 12-11 **Unimplemented:** Read as '0'

bit 10 **BCL:** Master Bus Collision Detect bit
1 = A bus collision has been detected during a master operation
0 = No collision
Hardware set at detection of bus collision.

bit 9 **GCSTAT:** General Call Status bit
1 = General call address was received
0 = General call address was not received
Hardware set when address matches general call address. Hardware clear at Stop detection.

bit 8 **ADD10:** 10-bit Address Status bit
1 = 10-bit address was matched
0 = 10-bit address was not matched
Hardware set at match of 2nd byte of matched 10-bit address. Hardware clear at Stop detection.

bit 7 **IWCOL:** Write Collision Detect bit
1 = An attempt to write the I2CxTRN register failed because the I^{2}C module is busy
0 = No collision
Hardware set at occurrence of write to I2CxTRN while busy (cleared by software).

bit 6 **I2COV:** Receive Overflow Flag bit
1 = A byte was received while the I2CxRCV register is still holding the previous byte
0 = No overflow
Hardware set at attempt to transfer I2CxRSR to I2CxRCV (cleared by software).

REGISTER 23-1: PMCON: PARALLEL PORT CONTROL REGISTER (CONTINUED)

bit 7-6 **CSF<1:0>:** Chip Select Function bits(1)
- 11 = Reserved
- 10 = PMCS1 and PMCS2 function as Chip Select
- 01 = PMCS2 functions as Chip Select and PMCS1 functions as address bit 14
- 00 = PMCS1 and PMCS2 function as address bit 14 and address bit 15

bit 5 **ALP:** Address Latch Polarity bit(1)
- 1 = Active-high (PMALL and PMALH)
- 0 = Active-low ($\overline{\text{PMALL}}$ and $\overline{\text{PMALH}}$)

bit 4 **CS2P:** Chip Select 2 Polarity bit(1)
- 1 = Active-high (PMCS2)
- 0 = Active-low ($\overline{\text{PMCS2}}$)

bit 3 **CS1P:** Chip Select 1 Polarity bit(1)
- 1 = Active-high (PMCS1)
- 0 = Active-low ($\overline{\text{PMCS1}}$)

bit 2 **Unimplemented:** Read as '0'

bit 1 **WRSP:** Write Strobe Polarity bit

For Slave Modes and Master mode 2 (MODE<1:0> = 00,01,10):
- 1 = Write strobe active-high (PMWR)
- 0 = Write strobe active-low ($\overline{\text{PMWR}}$)

For Master mode 1 (MODE<1:0> = 11):
- 1 = Enable strobe active-high (PMENB)
- 0 = Enable strobe active-low ($\overline{\text{PMENB}}$)

bit 0 **RDSP:** Read Strobe Polarity bit

For Slave modes and Master mode 2 (MODE<1:0> = 00,01,10):
- 1 = Read Strobe active-high (PMRD)
- 0 = Read Strobe active-low ($\overline{\text{PMRD}}$)

For Master mode 1 (MODE<1:0> = 11):
- 1 = Read/write strobe active-high (PMRD/$\overline{\text{PMWR}}$)
- 0 = Read/write strobe active-low ($\overline{\text{PMRD}}$/PMWR)

Note 1: These bits have no effect when their corresponding pins are used as address lines.

24.1 EBI Control Registers

TABLE 24-2: EBI REGISTER MAP

Virtual Address (BF8E_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
1014	EBICS0	31:16	CSADDR<15:0>																0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
1018	EBICS1(1)	31:16	CSADDR<15:0>																0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
101C	EBICS2(1)	31:16	CSADDR<15:0>																0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
1020	EBICS3(1)	31:16	CSADDR<15:0>																0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
1054	EBIMSK0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	REGSEL<2:0>			MEMTYPE<2:0>			MEMSIZE<4:0>					0020
1058	EBIMSK1(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	REGSEL<2:0>			MEMTYPE<2:0>			MEMSIZE<4:0>					0020
105C	EBIMSK2(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	REGSEL<2:0>			MEMTYPE<2:0>			MEMSIZE<4:0>					0120
1060	EBIMSK3(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	REGSEL<2:0>			MEMTYPE<2:0>			MEMSIZE<4:0>					0120
1094	EBISMT0	31:16	—	—	—	—	—	RDYMODE	PAGESIZE<1:0>		PAGEMODE	TPRC<3:0>				TBTA<2:0>			041C
		15:0	TWP<5:0>						TWR<1:0>		TAS<1:0>	TRC<5:0>							2D4B
1098	EBISMT1	31:16	—	—	—	—	—	RDYMODE	PAGESIZE<1:0>		PAGEMODE	TPRC<3:0>				TBTA<2:0>			041C
		15:0	TWP<5:0>						TWR<1:0>		TAS<1:0>	TRC<5:0>							2D4B
109C	EBISMT2	31:16	—	—	—	—	—	RDYMODE	PAGESIZE<1:0>		PAGEMODE	TPRC<3:0>				TBTA<2:0>			014C
		15:0	TWP<5:0>						TWR<1:0>		TAS<1:0>	TRC<5:0>							2D4B
10A0	EBIFTRPD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	TRPD<11:0>												00C8
10A4	EBISMCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	SMDWIDTH2<2:0>			SMDWIDTH1<2:0>			SMDWIDTH0<2:0>			—	—	—	—	—	—	SMRP	0201

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register is available on 144-pin devices only.

REGISTER 24-1: EBICSx: EXTERNAL BUS INTERFACE CHIP SELECT REGISTER ('x' = 0-3)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CSADDR<15:8>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CSADDR<7:0>							
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **CSADDR<15:0>:** Base Address for Device bits
Address in physical memory, which will select the external device.

bit 15-0 **Unimplemented:** Read as '0'

REGISTER 26-3: CEBDADDR: CRYPTO ENGINE BUFFER DESCRIPTOR REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	BDPADDR<31:24>							
23:16	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	BDPADDR<23:16>							
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	BDPADDR<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	BDPADDR<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **BDPADDR<31:0>:** Current Buffer Descriptor Process Address Status bits

These bits contain the current descriptor address that is being processed by the Buffer Descriptor Processor (BDP).

REGISTER 26-4: CEBDPADDR: CRYPTO ENGINE BUFFER DESCRIPTOR PROCESSOR REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BASEADDR<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BASEADDR<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BASEADDR<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BASEADDR<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **BASEADDR<31:0>:** Buffer Descriptor Base Address bits

These bits contain the physical address of the first Buffer Descriptor in the Buffer Descriptor chain. When enabled, the Crypto DMA begins fetching Buffer Descriptors from this address.

REGISTER 26-5: CESTAT: CRYPTO ENGINE STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	ERRMODE<2:0>			ERROP<2:0>			ERRPHASE<1:0>	
23:16	U-0	U-0	R-0	R-0	R-0	R-0	R-0	R-0
	—	—	BDSTATE<3:0>				START	ACTIVE
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	BDCTRL<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	BDCTRL<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-29 **ERRMODE<2:0>:** Internal Error Mode Status bits
- 111 = Reserved
- 110 = Reserved
- 101 = Reserved
- 100 = Reserved
- 011 = CEK operation
- 010 = KEK operation
- 001 = Preboot authentication
- 000 = Normal operation

bit 28-26 **ERROP<2:0>:** Internal Error Operation Status bits
- 111 = Reserved
- 110 = Reserved
- 101 = Reserved
- 100 = Authentication
- 011 = Reserved
- 010 = Decryption
- 001 = Encryption
- 000 = Reserved

bit 25-24 **ERRPHASE<1:0>:** Internal Error Phase of DMA Status bits
- 11 = Destination data
- 10 = Source data
- 01 = Security Association (SA) access
- 00 = Buffer Descriptor (BD) access

bit 23-22 **Unimplemented:** Read as '0'

bit 21-18 **BDSTATE<3:0>:** Buffer Descriptor Processor State Status bits

The current state of the BDP:
- 1111 = Reserved
- •
- •
- •
- 0111 = Reserved
- 0110 = SA fetch
- 0101 = Fetch BDP is disabled
- 0100 = Descriptor is done
- 0011 = Data phase
- 0010 = BDP is loading
- 0001 = Descriptor fetch request is pending
- 0000 = BDP is idle

bit 17 **START:** DMA Start Status bit
- 1 = DMA start has occurred
- 0 = DMA start has not occurred

26.2 Crypto Engine Buffer Descriptors

Host software creates a linked list of buffer descriptors and the hardware updates them. Table 26-3 provides a list of the Crypto Engine buffer descriptors, followed by format descriptions of each buffer descriptor (see Figure 26-2 through Figure 26-9).

TABLE 26-3: CRYPTO ENGINE BUFFER DESCRIPTORS

Name (see Note 1)		Bit 31/2315/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
BD_CTRL	31:24	DESC_EN	—	CRY_MODE<2:0>			—	—	—
	23:16	—	SA_FETCH_EN	—	—	LAST_BD	LIFM	PKT_INT_EN	CBD_INT_EN
	15:8	BD_BUFLEN<15:8>							
	7:0	BD_BUFLEN<7:0>							
BD_SA_ADDR	31:24	BD_SAADDR<31:24>							
	23:16	BD_SAADDR<23:16>							
	15:8	BD_SAADDR<15:8>							
	7:0	BD_SAADR<7:0>							
BD_SCRADDR	31:24	BD_SRCADDR<31:24>							
	23:16	BD_SRCADDR<23:16>							
	15:8	BD_SRCADDR<15:8>							
	7:0	BD_SRCADDR<7:0>							
BD_DSTADDR	31:24	BD_DSTADDR<31:24>							
	23:16	BD_DSTADDR<23:16>							
	15:8	BD_DSTADDR<15:8>							
	7:0	BD_DSTADDR<7:0>							
BD_NXTPTR	31:24	BD_NXTADDR<31:24>							
	23:16	BD_NXTADDR<23:16>							
	15:8	BD_NXTADDR<15:8>							
	7:0	BD_NXTADDR<7:0>							
BD_UPDPTR	31:24	BD_UPDADDR<31:24>							
	23:16	BD_UPDADDR<23:16>							
	15:8	BD_UPDADDR<15:8>							
	7:0	BD_UPDADDR<7:0>							
BD_MSG_LEN	31:24	MSG_LENGTH<31:24>							
	23:16	MSG_LENGTH<23:16>							
	15:8	MSG_LENGTH<15:8>							
	7:0	MSG_LENGTH<7:0>							
BD_ENC_OFF	31:24	ENCR_OFFSET<31:24>							
	23:16	ENCR_OFFSET<23:16>							
	15:8	ENCR_OFFSET<15:8>							
	7:0	ENCR_OFFSET<7:0>							

Note 1: The buffer descriptor must be allocated in memory on a 64-bit boundary.

REGISTER 28-5: ADCIMCON1: ADC INPUT MODE CONTROL REGISTER 1 (CONTINUED)

bit 4 **SIGN2:** AN2 Signed Data Mode bit
1 = AN2 is using Signed Data mode
0 = AN2 is using Unsigned Data mode

bit 3 **DIFF1:** AN1 Mode bit
1 = AN1 is using Differential mode
0 = AN1 is using Single-ended mode

bit 2 **SIGN1:** AN1 Signed Data Mode bit
1 = AN1 is using Signed Data mode
0 = AN1 is using Unsigned Data mode

bit 1 **DIFF0:** AN0 Mode bit
1 = AN0 is using Differential mode
0 = AN0 is using Single-ended mode

bit 0 **SIGN0:** AN0 Signed Data Mode bit
1 = AN0 is using Signed Data mode
0 = AN0 is using Unsigned Data mode

REGISTER 28-32: ADCANCON: ADC ANALOG WARM-UP CONTROL REGISTER (CONTINUED)

bit 7 **ANEN7:** Shared ADC (ADC7) Analog and Bias Circuitry Enable bit

1 = Analog and bias circuitry enabled. Once the analog and bias circuit is enabled, the ADC module needs a warm-up time, as defined by the WKUPCLKCNT<3:0> bits.

0 = Analog and bias circuitry disabled

bit 5-6 **Unimplemented:** Read as '0'

bit 4-0 **ANEN4:ANEN0:** ADC4-ADC0 Analog and Bias Circuitry Enable bits

1 = Analog and bias circuitry enabled. Once the analog and bias circuit is enabled, the ADC module needs a warm-up time, as defined by the WKUPCLKCNT<3:0> bits.

0 = Analog and bias circuitry disabled

REGISTER 29-12: CiFLTCON2: CAN FILTER CONTROL REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN11	MSEL11<1:0>		FSEL11<4:0>				
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN10	MSEL10<1:0>		FSEL10<4:0>				
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN9	MSEL9<1:0>		FSEL9<4:0>				
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN8	MSEL8<1:0>		FSEL8<4:0>				

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **FLTEN11:** Filter 11 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 30-29 **MSEL11<1:0>:** Filter 11 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 28-24 **FSEL11<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

bit 23 **FLTEN10:** Filter 10 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 22-21 **MSEL10<1:0>:** Filter 10 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 20-16 **FSEL10<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

Note: The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

REGISTER 29-16: CiFLTCON6: CAN FILTER CONTROL REGISTER 6

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN27	MSEL27<1:0>		FSEL27<4:0>				
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN26	MSEL26<1:0>		FSEL26<4:0>				
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN25	MSEL25<1:0>		FSEL25<4:0>				
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN24	MSEL24<1:0>		FSEL24<4:0>				

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **FLTEN27:** Filter 27 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 30-29 **MSEL27<1:0>:** Filter 27 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 28-24 **FSEL27<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

bit 23 **FLTEN26:** Filter 26 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 22-21 **MSEL26<1:0>:** Filter 26 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 20-16 **FSEL26<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

Note: The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

REGISTER 29-20: CiFIFOCONn: CAN FIFO CONTROL REGISTER 'n' ('n' = 0-31) (CONTINUED)

bit 6 **TXABAT:** Message Aborted bit(2)
1 = Message was aborted
0 = Message completed successfully

bit 5 **TXLARB:** Message Lost Arbitration bit(3)
1 = Message lost arbitration while being sent
0 = Message did not lose arbitration while being sent

bit 4 **TXERR:** Error Detected During Transmission bit(3)
1 = A bus error occurred while the message was being sent
0 = A bus error did not occur while the message was being sent

bit 3 **TXREQ:** Message Send Request
TXEN = 1: (FIFO configured as a Transmit FIFO)
Setting this bit to '1' requests sending a message.
The bit will automatically clear when all the messages queued in the FIFO are successfully sent.
Clearing the bit to '0' while set ('1') will request a message abort.
TXEN = 0: (FIFO configured as a Receive FIFO)
This bit has no effect.

bit 2 **RTREN:** Auto RTR Enable bit
1 = When a remote transmit is received, TXREQ will be set
0 = When a remote transmit is received, TXREQ will be unaffected

bit 1-0 **TXPR<1:0>:** Message Transmit Priority bits
11 = Highest Message Priority
10 = High Intermediate Message Priority
01 = Low Intermediate Message Priority
00 = Lowest Message Priority

Note 1: These bits can only be modified when the CAN module is in Configuration mode (OPMOD<2:0> bits (CiCON<23:21>) = 100).
2: This bit is updated when a message completes (or aborts) or when the FIFO is reset.
3: This bit is reset on any read of this register or when the FIFO is reset.

REGISTER 30-37: EMAC1SA0: ETHERNET CONTROLLER MAC STATION ADDRESS 0 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P
	STNADDR6<7:0>							
7:0	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P	R/W-P
	STNADDR5<7:0>							

Legend:		P = Programmable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-8 **STNADDR6<7:0>:** Station Address Octet 6 bits
These bits hold the sixth transmitted octet of the station address.

bit 7-0 **STNADDR5<7:0>:** Station Address Octet 5 bits
These bits hold the fifth transmitted octet of the station address.

Note 1: Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware.

2: This register is loaded at reset from the factory preprogrammed station address.

36.2 MPLAB XC Compilers

The MPLAB XC Compilers are complete ANSI C compilers for all of Microchip's 8, 16, and 32-bit MCU and DSC devices. These compilers provide powerful integration capabilities, superior code optimization and ease of use. MPLAB XC Compilers run on Windows, Linux or MAC OS X.

For easy source level debugging, the compilers provide debug information that is optimized to the MPLAB X IDE.

The free MPLAB XC Compiler editions support all devices and commands, with no time or memory restrictions, and offer sufficient code optimization for most applications.

MPLAB XC Compilers include an assembler, linker and utilities. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. MPLAB XC Compiler uses the assembler to produce its object file. Notable features of the assembler include:

- Support for the entire device instruction set
- Support for fixed-point and floating-point data
- Command-line interface
- Rich directive set
- Flexible macro language
- MPLAB X IDE compatibility

36.3 MPASM Assembler

The MPASM Assembler is a full-featured, universal macro assembler for PIC10/12/16/18 MCUs.

The MPASM Assembler generates relocatable object files for the MPLINK Object Linker, Intel® standard HEX files, MAP files to detail memory usage and symbol reference, absolute LST files that contain source lines and generated machine code, and COFF files for debugging.

The MPASM Assembler features include:

- Integration into MPLAB X IDE projects
- User-defined macros to streamline assembly code
- Conditional assembly for multipurpose source files
- Directives that allow complete control over the assembly process

36.4 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK Object Linker combines relocatable objects created by the MPASM Assembler. It can link relocatable objects from precompiled libraries, using directives from a linker script.

The MPLIB Object Librarian manages the creation and modification of library files of precompiled code. When a routine from a library is called from a source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications.

The object linker/library features include:

- Efficient linking of single libraries instead of many smaller files
- Enhanced code maintainability by grouping related modules together
- Flexible creation of libraries with easy module listing, replacement, deletion and extraction

36.5 MPLAB Assembler, Linker and Librarian for Various Device Families

MPLAB Assembler produces relocatable machine code from symbolic assembly language for PIC24, PIC32 and dsPIC DSC devices. MPLAB XC Compiler uses the assembler to produce its object file. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. Notable features of the assembler include:

- Support for the entire device instruction set
- Support for fixed-point and floating-point data
- Command-line interface
- Rich directive set
- Flexible macro language
- MPLAB X IDE compatibility

TABLE 37-45: USB OTG ELECTRICAL SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
USB313	VUSB3V3	USB Voltage	3.0	—	3.6	V	Voltage on VUSB3V3 must be in this range for proper USB operation
Low-Speed and Full-Speed Modes							
USB315	VILUSB	Input Low Voltage for USB Buffer	—	—	0.8	V	—
USB316	VIHUSB	Input High Voltage for USB Buffer	2.0	—	—	V	—
USB318	VDIFS	Differential Input Sensitivity	0.2	—	—	V	The difference between D+ and D- must exceed this value while VCM is met
USB319	VCM	Differential Common Mode Range	0.8	—	2.5	V	—
USB321	VOL	Voltage Output Low	0.0	—	0.3	V	1.425 kΩ load connected to VUSB3V3
USB322	VOH	Voltage Output High	2.8	—	3.6	V	14.25 kΩ load connected to ground
Hi-Speed Mode							
USB323	VHSDI	Differential input signal level	150	—	—	mV	—
USB324	VHSSQ	SQ detection threshold	100	—	150	mV	—
USB325	VHSCM	Common mode voltage range	-50	—	500	mV	—
USB326	VHSOH	Data signaling high	360	—	440	mV	—
USB327	VHSOL	Data signaling low	-10	—	10	mV	—
USB328	VCHIRPJ	Chirp J level	700	—	1100	mV	—
USB329	VCHIRPK	Chirp K level	-900	—	-500	mV	—
USB330	ZHSDRV	Driver output resistance	—	45	—	Ω	—

Note 1: These parameters are characterized, but not tested in manufacturing.

A.8 Flash Programming

The PIC32MZ EF family of devices incorporates a new Flash memory technology. Applications ported from PIC32MX5XX/6XX/7XX devices that take advantage of Run-time Self Programming will need to adjust the Flash programming steps to incorporate these changes.

Table A-9 lists the differences (indicated by **Bold** type) that will affect software migration.

TABLE A-9: FLASH PROGRAMMING DIFFERENCES

PIC32MX5XX/6XX/7XX Feature	PIC32MZ EF Feature
Program Flash Write Protection	
On PIC32MX devices, the Program Flash write-protect bits are part of the Flash Configuration words (DEVCFG0). PWP<**7**:0> (**DEVCFG0<19:12>**) 11111111 = Disabled 11111110 = 0xBD000FFF 11111101 = 0xBD001FFF 11111100 = 0xBD002FFF 11111011 = 0xBD003FFF 11111010 = 0xBD004FFF 11111001 = 0xBD005FFF 11111000 = 0xBD006FFF 11110111 = 0xBD007FFF 11110110 = 0xBD008FFF 11110101 = 0xBD009FFF 11110100 = 0xBD00AFFF 11110011 = 0xBD00BFFF 11110010 = 0xBD00CFFF 11110001 = 0xBD00DFFF 11110000 = 0xBD00EFFF 11101111 = 0xBD00FFFF • • • 01111111 = 0xBD07FFFF	On PIC32MZ EF devices, the write-protect register is contained separately as the NVMPWP register. It has been expanded to 24 bits, and now represents the address below, which all Flash memory is protected. Note that the lower 14 bits are forced to zero, so that all memory locations in the page are protected. PWP<**23**:0> (**NVMPWP<23:0>**) Physical memory below address 0x1Dxxxxxx is write protected, where 'xxxxxx' is specified by PWP<23:0>. When PWP<23:0> has a value of '0', write protection is disabled for the entire program Flash. If the specified address falls within the page, the entire page and all pages below the current page will be protected.
Code Protection	
On PIC32MX devices, code protection is enabled by the CP (**DEVCFG**<28>) bit.	On PIC32MZ EF devices, code protection is enabled by the CP (**DEVCP0**<28>) bit.
Boot Flash Write Protection	
On PIC32MX devices, Boot Flash write protection is enable by the **BWP (DEVCFG<24>)** bit and protects the entire Boot Flash memory.	On PIC32MZ EF devices, Boot Flash write protection is divided into pages and is enable by the **LBWPx** and **UBWPx** bits in the **NVMBWP** register.
Low-Voltage Detect Status	
LVDSTAT (NVMCON<11>) 1 = Low-voltage event is active 0 = Low-voltage event is not active	The LVDSTAT bit is not available in PIC32MZ EF devices.

TABLE A-9: FLASH PROGRAMMING DIFFERENCES (CONTINUED)

PIC32MX5XX/6XX/7XX Feature	PIC32MZ EF Feature
Flash Programming	
	The op codes for programming the Flash memory have been changed to accommodate the new quad-word programming and dual-panel features. The row size has changed to 2 KB (512 IW) from 128 IW. The page size has changed to 16 KB (4K IW) from 4 KB (1K IW). Note that the NVMOP register is now protected, and requires the WREN bit be set to enable modification.
NVMOP<3:0> (NVMCON<3:0>) 1111 = Reserved • • • **0111 = Reserved** **0110 = No operation** **0101 = Program Flash (PFM) erase operation** 0100 = Page erase operation 0011 = Row program operation **0010 = No operation** 0001 = Word program operation 0000 = No operation	NVMOP<3:0> (NVMCON<3:0>) 1111 = Reserved • • • 1000 = Reserved **0111 = Program erase operation** **0110 = Upper program Flash memory erase operation** **0101 = Lower program Flash memory erase operation** 0100 = Page erase operation 0011 = Row program operation **0010 = Quad Word (128-bit) program operation** 0001 = Word program operation 0000 = No operation
PIC32MX devices feature a single NVMDATA register for word programming. NVMDATA	On PIC32MZ EF devices, to support quad word programming, the NVMDATA register has been expanded to four words. NVMDATA**x**, where 'x' = 0 through 3
Flash Endurance and Retention	
PIC32MX devices support Flash endurance and retention of up to 20K E/W cycles and 20 years.	On PIC32MZ EF devices, ECC must be enabled to support the same endurance and retention as PIC32MX devices.
Configuration Words	
On PIC32MX devices, Configuration Words can be programmed with **Word or Row program** operation.	On PIC32MZ EF devices, all Configuration Words must be programmed with **Quad Word or Row Program** operations.
Configuration Words Reserved Bit	
On PIC32MX devices, the **DEVCFG0<15>** bit is Reserved and must be programmed to '0'.	On PIC32MZ EF devices, this bit is **DEVSIGN0<31>**.