Microchip Technology - PIC32MZ2048EFH144T-250I/PH Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® M-Class
Core Size	32-Bit Single-Core
Speed	252MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, PMP, SPI, SQI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	120
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	2.1V ~ 3.6V
Data Converters	A/D 48x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-TQFP
Supplier Device Package	144-TQFP (16x16)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mz2048efh144t-250i-ph

REGISTER 3-3: CONFIG3: CONFIGURATION REGISTER 3; CP0 REGISTER 16, SELECT 3

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	r-1	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	R-0	R-1	R-0	R-0	R-0	R-1	R/W-y
	—	IPLW<1:0>		MMAR<2:0>			MCU	ISAONEXC(1)
15:8	R-y	R-y	R-1	R-1	R-1	R-1	U-0	R-1
	ISA<1:0>(1)		ULRI	RXI	DSP2P	DSPP	—	ITL
7:0	U-0	R-1	R-1	R-0	R-1	U-0	U-0	R-0
	—	VEIC	VINT	SP	CDMM	—	—	TL

Legend:	r = Reserved bit	y = Value set from Configuration bits on POR
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 31 **Reserved:** This bit is hardwired as '1' to indicate the presence of the Config4 register

bit 30-23 **Unimplemented:** Read as '0'

bit 22-21 **IPLW<1:0>:** Width of the Status IPL and Cause RIPL bits
01 = IPL and RIPL bits are 8-bits in width

bit 20-18 **MMAR<2:0>:** microMIPS Architecture Revision Level bits
000 = Release 1

bit 17 **MCU:** MIPS® MCU™ ASE Implemented bit
1 = MCU ASE is implemented

bit 16 **ISAONEXC:** ISA on Exception bit(1)
1 = microMIPS is used on entrance to an exception vector
0 = MIPS32 ISA is used on entrance to an exception vector

bit 15-14 **ISA<1:0>:** Instruction Set Availability bits(1)
11 = Both MIPS32 and microMIPS are implemented; microMIPS is used when coming out of reset
10 = Both MIPS32 and microMIPS are implemented; MIPS32 ISA used when coming out of reset

bit 13 **ULRI:** UserLocal Register Implemented bit
1 = UserLocal Coprocessor 0 register is implemented

bit 12 **RXI:** RIE and XIE Implemented in PageGrain bit
1 = RIE and XIE bits are implemented

bit 11 **DSP2P:** MIPS DSP ASE Revision 2 Presence bit
1 = DSP Revision 2 is present

bit 10 **DSPP:** MIPS DSP ASE Presence bit
1 = DSP is present

bit 9 **Unimplemented:** Read as '0'

bit 8 **ITL:** Indicates that iFlowtrace® hardware is present
1 = The iFlowtrace® is implemented in the core

bit 7 **Unimplemented:** Read as '0'

bit 6 **VEIC:** External Vector Interrupt Controller bit
1 = Support for an external interrupt controller is implemented

bit 5 **VINT:** Vector Interrupt bit
1 = Vector interrupts are implemented

bit 4 **SP:** Small Page bit
0 = 4 KB page size

bit 3 **CDMM:** Common Device Memory Map bit
1 = CDMM is implemented

bit 2-1 **Unimplemented:** Read as '0'

bit 0 **TL:** Trace Logic bit
0 = Trace logic is not implemented

Note 1: These bits are set based on the value of the BOOTISA Configuration bit (DEVCFG0<6>).

REGISTER 4-1: BFxSEQ3: BOOT FLASH 'x' SEQUENCE WORD 3 REGISTER ('x' = 1 AND 2)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/P	R/P	R/P	R/P	R/P	R/P	R/P	R/P
	CSEQ<15:8>							
23:16	R/P	R/P	R/P	R/P	R/P	R/P	R/P	R/P
	CSEQ<7:0>							
15:8	R/P	R/P	R/P	R/P	R/P	R/P	R/P	R/P
	TSEQ<15:8>							
7:0	R/P	R/P	R/P	R/P	R/P	R/P	R/P	R/P
	TSEQ<7:0>							

Legend:		P = Programmable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **CSEQ<15:0>:** Boot Flash Complement Sequence Number bits

bit 15-0 **TSEQ<15:0>:** Boot Flash True Sequence Number bits

Note: The BFxSEQ0, BFxSEQ1, and BFxSEQ2 registers are used for Quad Word programming operation when programming the BFxSEQ3 registers, and do not contain any valid information.

TABLE 4-9: SYSTEM BUS TARGET 1 REGISTER MAP (CONTINUED)

Virtual Address (BF8F_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
84E0	SBT1REG5	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
84F0	SBT1RD5	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
84F8	SBT1WR5	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8500	SBT1REG6	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
8510	SBT1RD6	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8518	SBT1WR6	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8520	SBT1REG7	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
8530	SBT1RD7	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8538	SBT1WR7	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8540	SBT1REG8	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
8550	SBT1RD8	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
8558	SBT1WR8	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note: For reset values listed as 'xxxx', please refer to Table 4-6 for the actual reset values.

TABLE 10-3: DMA CHANNEL 0 THROUGH CHANNEL 7 REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
14A0	DCH5DPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDPTR<15:0>																0000
14B0	DCH5CSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCSIZ<15:0>																0000
14C0	DCH5CPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCPTR<15:0>																0000
14D0	DCH5DAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHPDAT<15:0>																0000
14E0	DCH6CON	31:16	CHPIGN<7:0>								—	—	—	—	—	—	—	—	0000
		15:0	CHBUSY	—	CHPIGNEN	—	CHPATLEN	—	—	CHCHNS	CHEN	CHAED	CHCHN	CHAEN	—	CHEDET	CHPRI<1:0>		0000
14F0	DCH6ECON	31:16	—	—	—	—	—	—	—	—	CHAIRQ<7:0>								00FF
		15:0	CHSIRQ<7:0>								CFORCE	CABORT	PATEN	SIRQEN	AIRQEN	—	—	—	FF00
1500	DCH6INT	31:16	—	—	—	—	—	—	—	—	CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE	CHERIE	0000
		15:0	—	—	—	—	—	—	—	—	CHSDIF	CHSHIF	CHDDIF	CHDHIF	CHBCIF	CHCCIF	CHTAIF	CHERIF	0000
1510	DCH6SSA	31:16	CHSSA<31:0>																0000
		15:0																	0000
1520	DCH6DSA	31:16	CHDSA<31:0>																0000
		15:0																	0000
1530	DCH6SSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSSIZ<15:0>																0000
1540	DCH6DSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDSIZ<15:0>																0000
1550	DCH6SPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSPTR<15:0>																0000
1560	DCH6DPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDPTR<15:0>																0000
1570	DCH6CSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCSIZ<15:0>																0000
1580	DCH6CPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCPTR<15:0>																0000
1590	DCH6DAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHPDAT<15:0>																0000
15A0	DCH7CON	31:16	CHPIGN<7:0>								—	—	—	—	—	—	—	—	0000
		15:0	CHBUSY	—	CHPIGNEN	—	CHPATLEN	—	—	CHCHNS	CHEN	CHAED	CHCHN	CHAEN	—	CHEDET	CHPRI<1:0>		0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 "CLR, SET, and INV Registers"** for more information.

REGISTER 10-8: DCHxECON: DMA CHANNEL x EVENT CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
	CHAIRQ<7:0>(1)							
15:8	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
	CHSIRQ<7:0>(1)							
7:0	S-0	S-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0
	CFORCE	CABORT	PATEN	SIRQEN	AIRQEN	—	—	—

Legend:	S = Settable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-24 **Unimplemented:** Read as '0'

bit 23-16 **CHAIRQ<7:0>:** Channel Transfer Abort IRQ bits(1)

11111111 = Interrupt 255 will abort any transfers in progress and set CHAIF flag
•
•
•
00000001 = Interrupt 1 will abort any transfers in progress and set CHAIF flag
00000000 = Interrupt 0 will abort any transfers in progress and set CHAIF flag

bit 15-8 **CHSIRQ<7:0>:** Channel Transfer Start IRQ bits(1)

11111111 = Interrupt 255 will initiate a DMA transfer
•
•
•
00000001 = Interrupt 1 will initiate a DMA transfer
00000000 = Interrupt 0 will initiate a DMA transfer

bit 7 **CFORCE:** DMA Forced Transfer bit

1 = A DMA transfer is forced to begin when this bit is written to a '1'
0 = This bit always reads '0'

bit 6 **CABORT:** DMA Abort Transfer bit

1 = A DMA transfer is aborted when this bit is written to a '1'
0 = This bit always reads '0'

bit 5 **PATEN:** Channel Pattern Match Abort Enable bit

1 = Abort transfer and clear CHEN on pattern match
0 = Pattern match is disabled

bit 4 **SIRQEN:** Channel Start IRQ Enable bit

1 = Start channel cell transfer if an interrupt matching CHSIRQ occurs
0 = Interrupt number CHSIRQ is ignored and does not start a transfer

bit 3 **AIRQEN:** Channel Abort IRQ Enable bit

1 = Channel transfer is aborted if an interrupt matching CHAIRQ occurs
0 = Interrupt number CHAIRQ is ignored and does not terminate a transfer

bit 2-0 **Unimplemented:** Read as '0'

Note 1: See **Table 7-2: "Interrupt IRQ, Vector, and Bit Location"** for the list of available interrupt IRQ sources.

REGISTER 11-9: USBIENCSR1: USB INDEXED ENDPOINT CONTROL STATUS REGISTER 1 (ENDPOINT 1-7) (CONTINUED)

bit 18 **OVERRUN:** Data Overrun Status bit (*Device mode*)

1 = An OUT packet cannot be loaded into the RX FIFO.
0 = Written by software to clear this bit

This bit is only valid when the endpoint is operating in ISO mode. In Bulk mode, it always returns zero.

ERROR: No Data Packet Received Status bit (*Host mode*)

1 = Three attempts have been made to receive a packet and no data packet has been received. An interrupt is generated.

0 = Written by the software to clear this bit.

This bit is only valid when the RX endpoint is operating in Bulk or Interrupt mode. In ISO mode, it always returns zero.

bit 17 **FIFOFULL:** FIFO Full Status bit

1 = No more packets can be loaded into the RX FIFO
0 = The RX FIFO has at least one free space

bit 16 **RXPKTRDY:** Data Packet Reception Status bit

1 = A data packet has been received. An interrupt is generated.
0 = Written by software to clear this bit when the packet has been unloaded from the RX FIFO.

bit 15-11 **MULT<4:0>:** Multiplier Control bits

For Isochronous/Interrupt endpoints or of packet splitting on Bulk endpoints, multiplies TXMAXP by MULT+1 for the payload size.

For Bulk endpoints, MULT can be up to 32 and defines the number of “USB” packets of the specified payload into which a single data packet placed in the FIFO should be split, prior to transfer. The data packet is required to be an exact multiple of the payload specified by TXMAXP.

For Isochronous/Interrupts endpoints operating in Hi-Speed mode, MULT may be either 2 or 3 and specifies the maximum number of such transactions that can take place in a single microframe.

bit 10-0 **RXMAXP<10:0>:** Maximum RX Payload Per Transaction Control bits

This field sets the maximum payload (in bytes) transmitted in a single transaction. The value is subject to the constraints placed by the USB Specification on packet sizes for Bulk, Interrupt and Isochronous transfers in Full-Speed and Hi-Speed operations.

RXMAXP must be set to an even number of bytes for proper interrupt generation in DMA Mode 1.

REGISTER 20-20: SQI1BDRXDSTAT: SQI BUFFER DESCRIPTOR DMA RECEIVE STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	R-x	R-x	R-x	R-x	U-0
	—	—	—	RXSTATE<3:0>				—
23:16	U-0	U-0	U-0	R-x	R-x	R-x	R-x	R-x
	—	—	—	RXBUFCNT<4:0>				
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
	RXCURBUFLEN<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-29 **Unimplemented:** Read as '0'

bit 28-25 **RXSTATE<3:0>:** Current DMA Receive State Status bits
These bits provide information on the current DMA receive states.

bit 24-21 **Unimplemented:** Read as '0'

bit 20-16 **RXBUFCNT<4:0>:** DMA Buffer Byte Count Status bits
These bits provide information on the internal FIFO space.

bit 15-8 **Unimplemented:** Read as '0'

bit 7-0 **RXCURBUFLEN<7:0>:** Current DMA Receive Buffer Length Status bits
These bits provide the length of the current DMA receive buffer.

REGISTER 20-21: SQI1THR: SQI THRESHOLD CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	THRES<4:0>				

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-5 **Unimplemented:** Read as '0'

bit 4-0 **THRES<4:0>:** SQI Control Threshold Value bits
The SQI control threshold interrupt is asserted when the amount of space indicated by THRES<4:0> is available in the SQI control buffer.

REGISTER 21-2: I2CxSTAT: I^2C STATUS REGISTER (CONTINUED)

bit 5 **D_A:** Data/Address bit (when operating as I^2C slave)
1 = Indicates that the last byte received was data
0 = Indicates that the last byte received was device address
Hardware clear at device address match. Hardware set by reception of slave byte.

bit 4 **P:** Stop bit
1 = Indicates that a Stop bit has been detected last
0 = Stop bit was not detected last
Hardware set or clear when Start, Repeated Start or Stop detected.

bit 3 **S:** Start bit
1 = Indicates that a Start (or Repeated Start) bit has been detected last
0 = Start bit was not detected last
Hardware set or clear when Start, Repeated Start or Stop detected.

bit 2 **R_W:** Read/Write Information bit (when operating as I^2C slave)
1 = Read – indicates data transfer is output from slave
0 = Write – indicates data transfer is input to slave
Hardware set or clear after reception of I^2C device address byte.

bit 1 **RBF:** Receive Buffer Full Status bit
1 = Receive complete, I2CxRCV is full
0 = Receive not complete, I2CxRCV is empty
Hardware set when I2CxRCV is written with received byte. Hardware clear when software reads I2CxRCV.

bit 0 **TBF:** Transmit Buffer Full Status bit
1 = Transmit in progress, I2CxTRN is full
0 = Transmit complete, I2CxTRN is empty
Hardware set when software writes I2CxTRN. Hardware clear at completion of data transmission.

22.0 UNIVERSAL ASYNCHRONOUS RECEIVER TRANSMITTER (UART)

Note: This data sheet summarizes the features of the PIC32MZ EF family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 21. "Universal Asynchronous Receiver Transmitter (UART)"** (DS60001107) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

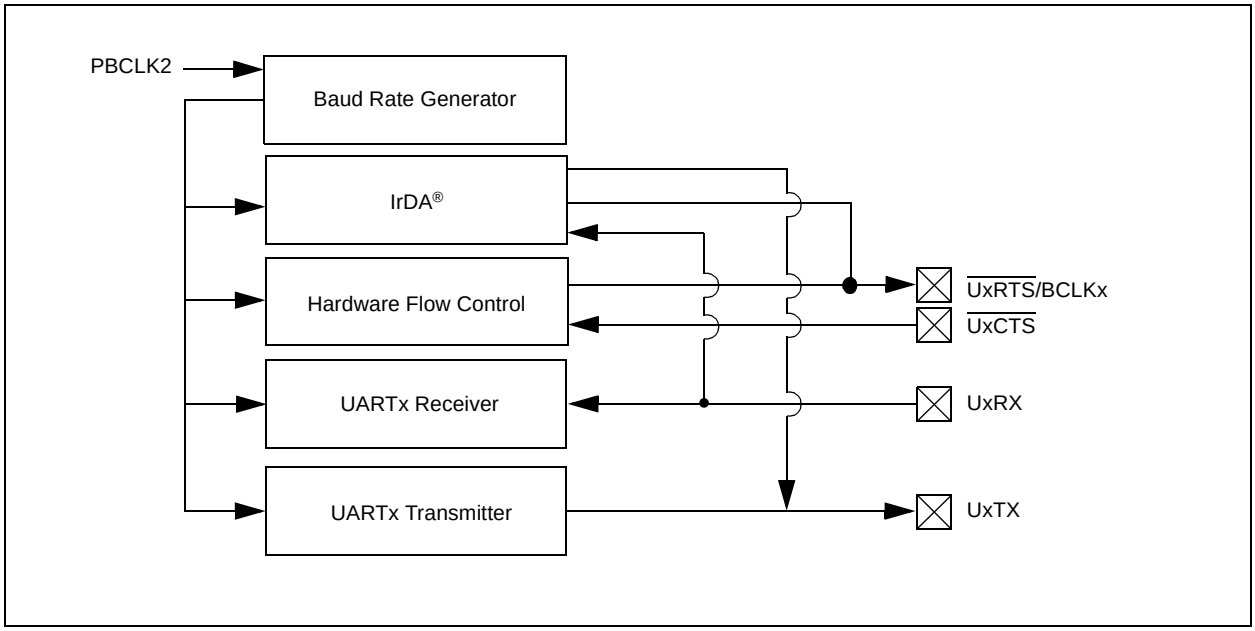
The UART module is one of the serial I/O modules available in the PIC32MZ EF family of devices. The UART is a full-duplex, asynchronous communication channel that communicates with peripheral devices and personal computers through protocols, such as RS-232, RS-485, LIN, and IrDA®. The module also supports the hardware flow control option, with $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$ pins, and also includes an IrDA encoder and decoder.

The primary features of the UART module are:

- Full-duplex, 8-bit or 9-bit data transmission
- Even, Odd or No Parity options (for 8-bit data)
- One or two Stop bits
- Hardware auto-baud feature
- Hardware flow control option
- Fully integrated Baud Rate Generator (BRG) with 16-bit prescaler
- Baud rates ranging from 76 bps to 25 Mbps at 100 MHz (PBCLK2)
- 8-level deep First-In-First-Out (FIFO) transmit data buffer
- 8-level deep FIFO receive data buffer
- Parity, framing and buffer overrun error detection
- Support for interrupt-only on address detect (9th bit = 1)
- Separate transmit and receive interrupts
- Loopback mode for diagnostic support
- LIN Protocol support
- IrDA encoder and decoder with 16x baud clock output for external IrDA encoder/decoder support

Figure 22-1 illustrates a simplified block diagram of the UART module.

FIGURE 22-1: UART SIMPLIFIED BLOCK DIAGRAM



REGISTER 23-1: PMCON: PARALLEL PORT CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	R/W-0, HC	U-0	U-0	U-0	U-0	U-0	R/W-0	U-0
	RDSTART	—	—	—	—	—	DUALBUF	—
15:8	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ON	—	SIDL	ADRMUX<1:0>		PMPTTL	PTWREN	PTRDEN
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
	CSF<1:0>(1)		ALP(1)	CS2P(1)	CS1P(1)	—	WRSP	RDSP

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-24 **Unimplemented:** Read as '0'

bit 23 **RDSTART:** Start Read on PMP Bus bit
This bit is cleared by hardware at the end of the read cycle.
1 = Start a read cycle on the PMP bus
0 = No effect

bit 22-18 **Unimplemented:** Read as '0'

bit 17 **DUALBUF:** Dual Read/Write Buffers enable bit
This bit is valid in Master mode only.
1 = PMP uses separate registers for reads and writes (PMRADDR, PMDATAIN, PMWADDR, PMDATAOUT)
0 = PMP uses legacy registers (PMADDR, PMDATA)

bit 16 **Unimplemented:** Read as '0'

bit 15 **ON:** Parallel Master Port Enable bit
1 = PMP is enabled
0 = PMP is disabled, no off-chip access performed

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit
1 = Discontinue module operation when device enters Idle mode
0 = Continue module operation in Idle mode

bit 12-11 **ADRMUX<1:0>:** Address/Data Multiplexing Selection bits
11 = Lower 8 bits of address are multiplexed on PMD<15:0> pins; upper 8 bits are not used
10 = All 16 bits of address are multiplexed on PMD<15:0> pins
01 = Lower 8 bits of address are multiplexed on PMD<7:0> pins, upper bits are on PMA<15:8>
00 = Address and data appear on separate pins

bit 10 **PMPTTL:** PMP Module TTL Input Buffer Select bit
1 = PMP module uses TTL input buffers
0 = PMP module uses Schmitt Trigger input buffer

bit 9 **PTWREN:** Write Enable Strobe Port Enable bit
1 = PMWR/PMENB port is enabled
0 = PMWR/PMENB port is disabled

bit 8 **PTRDEN:** Read/Write Strobe Port Enable bit
1 = PMRD/PMWR port is enabled
0 = PMRD/PMWR port is disabled

Note 1: These bits have no effect when their corresponding pins are used as address lines.

28.1 ADC Control Registers

TABLE 28-1: ADC REGISTER MAP

Virtual Address (BF84_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
B000	ADCCON1	31:16	TRBEN	TRBERR	TRBMST<2:0>			TRBSLV<2:0>			FRACT	SELRES<1:0>		STRGSRC<4:0>					0060
		15:0	ON	—	SIDL	AICPMPEN	CVDEN	FSSCLKEN	FSPBCLKEN	—	—	IRQVS<2:0>			STRGLVL	—	—	—	1000
B004	ADCCON2	31:16	BGVRRDY	REFFLT	EOSRDY	CVDCPL<2:0>			SAMC<9:0>										0000
		15:0	BGVRIEN	REFFLTIEN	EOSIEN	ADCEIOVR	—	ADCEIS<2:0>			—	ADCDIV<6:0>							0000
B008	ADCCON3	31:16	ADCSEL<1:0>		CONCLKDIV<5:0>						DIGEN7	—	—	DIGEN4	DIGEN3	DIGEN2	DIGEN1	DIGEN0	0000
		15:0	VREFSEL<2:0>			TRGSUSP	UPDIEN	UPDRDY	SAMP	RQCNVRT	GLSWTRG	GSWTRG	ADINSEL<5:0>						0000
B00C	ADCTRGMODE	31:16	—	—	—	—	—	—	SH4ALT<1:0>		SH3ALT<1:0>		SH2ALT<1:0>		SH1ALT<1:0>		SH0ALT<1:0>		0000
		15:0	—	—	—	STRGEN4	STRGEN3	STRGEN2	STRGEN1	STRGEN0	—	—	—	SSAMPEN4	SSAMPEN3	SSAMPEN2	SSAMPEN1	SSAMPEN0	0000
B010	ADCIMCON1	31:16	DIFF15	SIGN15	DIFF14	SIGN14	DIFF13	SIGN13	DIFF12	SIGN12	DIFF11	SIGN11	DIFF10	SIGN10	DIFF9	SIGN9	DIFF8	SIGN8	0000
		15:0	DIFF7	SIGN7	DIFF6	SIGN6	DIFF5	SIGN5	DIFF4	SIGN4	DIFF3	SIGN3	DIFF2	SIGN2	DIFF1	SIGN1	DIFF0	SIGN0	0000
B014	ADCIMCON2	31:16	DIFF31(1)	SIGN31(1)	DIFF30(1)	SIGN30(1)	DIFF29(1)	SIGN29(1)	DIFF28(1)	SIGN28(1)	DIFF27(1)	SIGN27(1)	DIFF26(1)	SIGN26(1)	DIFF25(1)	SIGN25(1)	DIFF24(1)	SIGN24(1)	0000
		15:0	DIFF23(1)	SIGN23(1)	DIFF22(1)	SIGN22(1)	DIFF21(1)	SIGN21(1)	DIFF20(1)	SIGN20(1)	DIFF19(1)	SIGN19(1)	DIFF18	SIGN18	DIFF17	SIGN17	DIFF16	SIGN16	0000
B018	ADCIMCON3	31:16	—	—	—	—	—	—	DIFF44	SIGN44	DIFF43	SIGN43	DIFF42(2)	SIGN42(2)	DIFF41(2)	SIGN41(2)	DIFF40(2)	SIGN40(2)	0000
		15:0	DIFF39(2)	SIGN39(2)	DIFF38(2)	SIGN38(2)	DIFF37(2)	SIGN37(2)	DIFF36(2)	SIGN36(2)	DIFF35(2)	SIGN35(2)	DIFF34(1)	SIGN34(1)	DIFF33(1)	SIGN33(1)	DIFF32(1)	SIGN32(1)	0000
B020	ADCGIRQEN1	31:16	AGIEN31(1)	AGIEN30(1)	AGIEN29(1)	AGIEN28(1)	AGIEN27(1)	AGIEN26(1)	AGIEN25(1)	AGIEN24(1)	AGIEN23(1)	AGIEN22(1)	AGIEN21(1)	AGIEN20(1)	AGIEN19(1)	AGIEN18	AGIEN17	AGIEN16	0000
		15:0	AGIEN15	AGIEN14	AGIEN13	AGIEN12	AGIEN11	AGIEN10	AGIEN9	AGIEN8	AGIEN7	AGIEN6	AGIEN5	AGIEN4	AGIEN3	AGIEN2	AGIEN1	AGIEN0	0000
B024	ADCGIRQEN2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	AGIEN44	AGIEN43	AGIEN42(2)	AGIEN41(2)	AGIEN40(2)	AGIEN39(2)	AGIEN38(2)	AGIEN37(2)	AGIEN36(2)	AGIEN35(2)	AGIEN34(1)	AGIEN33(1)	AGIEN32(1)	0000
B028	ADCCSS1	31:16	CSS31(1)	CSS30(1)	CSS29(1)	CSS28(1)	CSS27(1)	CSS26(1)	CSS25(1)	CSS24(1)	CSS23(1)	CSS22(1)	CSS21(1)	CSS20(1)	CSS19(1)	CSS18	CSS17	CSS16	0000
		15:0	CSS15	CSS14	CSS13	CSS12	CSS11	CSS10	CSS9	CSS8	CSS7	CSS6	CSS5	CSS4	CSS3	CSS2	CSS1	CSS0	0000
B02C	ADCCSS2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	CSS44	CSS43	CSS42(2)	CSS41(2)	CSS40(2)	CSS39(2)	CSS38(2)	CSS37(2)	CSS36(2)	CSS35(2)	CSS34(1)	CSS33(1)	CSS32(1)	0000
B030	ADCDSTAT1	31:16	ARDY31(1)	ARDY30(1)	ARDY29(1)	ARDY28(1)	ARDY27(1)	ARDY26(1)	ARDY25(1)	ARDY24(1)	ARDY23(1)	ARDY22(1)	ARDY21(1)	ARDY20(1)	ARDY19(1)	ARDY18	ARDY17	ARDY16	0000
		15:0	ARDY15	ARDY14	ARDY13	ARDY12	ARDY11	ARDY10	ARDY9	ARDY8	ARDY7	ARDY6	ARDY5	ARDY4	ARDY3	ARDY2	ARDY1	ARDY0	0000
B034	ADCDSTAT2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	ARDY44	ARDY43	ARDY42(2)	ARDY41(2)	ARDY40(2)	ARDY39(2)	ARDY38(2)	ARDY37(2)	ARDY36(2)	ARDY35(2)	ARDY34(1)	ARDY33(1)	ARDY32(1)	0000
B038	ADCCMPEN1	31:16	CMPE31(1)	CMPE30(1)	CMPE29(1)	CMPE28(1)	CMPE27(1)	CMPE26(1)	CMPE25(1)	CMPE24(1)	CMPE23(1)	CMPE22(1)	CMPE21(1)	CMPE20(1)	CMPE19(1)	CMPE18	CMPE17	CMPE16	0000
		15:0	CMPE15	CMPE14	CMPE13	CMPE12	CMPE11	CMPE10	CMPE9	CMPE8	CMPE7	CMPE6	CMPE5	CMPE4	CMPE3	CMPE2	CMPE1	CMPE0	0000
B03C	ADCCMP1	31:16	DCMPHI<15:0>																0000
		15:0	DCMPLO<15:0>																0000
B040	ADCCMPEN2	31:16	CMPE31(1)	CMPE30(1)	CMPE29(1)	CMPE28(1)	CMPE27(1)	CMPE26(1)	CMPE25(1)	CMPE24(1)	CMPE23(1)	CMPE22(1)	CMPE21(1)	CMPE20(1)	CMPE19(1)	CMPE18	CMPE17	CMPE16	0000
		15:0	CMPE15	CMPE14	CMPE13	CMPE12	CMPE11	CMPE10	CMPE9	CMPE8	CMPE7	CMPE6	CMPE5	CMPE4	CMPE3	CMPE2	CMPE1	CMPE0	0000
B044	ADCCMP2	31:16	DCMPHI<15:0>																0000
		15:0	DCMPLO<15:0>																0000
B048	ADCCMPEN3	31:16	CMPE31(1)	CMPE30(1)	CMPE29(1)	CMPE28(1)	CMPE27(1)	CMPE26(1)	CMPE25(1)	CMPE24(1)	CMPE23(1)	CMPE22(1)	CMPE21(1)	CMPE20(1)	CMPE19(1)	CMPE18	CMPE17	CMPE16	0000
		15:0	CMPE15	CMPE14	CMPE13	CMPE12	CMPE11	CMPE10	CMPE9	CMPE8	CMPE7	CMPE6	CMPE5	CMPE4	CMPE3	CMPE2	CMPE1	CMPE0	0000

Note 1: This bit or register is not available on 64-pin devices.
2: This bit or register is not available on 64-pin and 100-pin devices.
3: Before enabling the ADC, the user application must initialize the ADC calibration values by copying them from the factory-programmed DEVADCx Flash registers into the corresponding ADCxCFG registers.

REGISTER 28-5: ADCIMCON1: ADC INPUT MODE CONTROL REGISTER 1 (CONTINUED)

bit 4 **SIGN2:** AN2 Signed Data Mode bit
1 = AN2 is using Signed Data mode
0 = AN2 is using Unsigned Data mode

bit 3 **DIFF1:** AN1 Mode bit
1 = AN1 is using Differential mode
0 = AN1 is using Single-ended mode

bit 2 **SIGN1:** AN1 Signed Data Mode bit
1 = AN1 is using Signed Data mode
0 = AN1 is using Unsigned Data mode

bit 1 **DIFF0:** AN0 Mode bit
1 = AN0 is using Differential mode
0 = AN0 is using Single-ended mode

bit 0 **SIGN0:** AN0 Signed Data Mode bit
1 = AN0 is using Signed Data mode
0 = AN0 is using Unsigned Data mode

REGISTER 28-18: ADCTRG2: ADC TRIGGER SOURCE 2 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	TRGSRC7<4:0>				
23:16	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	TRGSRC6<4:0>				
15:8	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	TRGSRC5<4:0>				
7:0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	TRGSRC4<4:0>				

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-29 **Unimplemented:** Read as '0'

bit 28-24 **TRGSRC7<4:0>:** Trigger Source for Conversion of Analog Input AN7 Select bits
11111 = Reserved
•
•
•
01101 = Reserved
01100 = Comparator 2 (COUT)
01011 = Comparator 1 (COUT)
01010 = OCMP5
01001 = OCMP3
01000 = OCMP1
00111 = TMR5 match
00110 = TMR3 match
00101 = TMR1 match
00100 = INT0 External interrupt
00011 = STRIG
00010 = Global level software trigger (GLSWTRG)
00001 = Global software edge Trigger (GSWTRG)
00000 = No Trigger

For STRIG, in addition to setting the trigger, it also requires programming of the STRGSRC<4:0> bits (ADCCON1<20:16>) to select the trigger source, and requires the appropriate CSS bits to be set in the ADCCSS*x* registers.

bit 23-21 **Unimplemented:** Read as '0'

bit 20-16 **TRGSRC6<4:0>:** Trigger Source for Conversion of Analog Input AN6 Select bits
See bits 28-24 for bit value definitions.

bit 15-13 **Unimplemented:** Read as '0'

bit 12-8 **TRGSRC5<4:0>:** Trigger Source for Conversion of Analog Input AN5 Select bits
See bits 28-24 for bit value definitions.

bit 7-5 **Unimplemented:** Read as '0'

bit 4-0 **TRGSRC4<4:0>:** Trigger Source for Conversion of Analog Input AN4 Select bits
See bits 28-24 for bit value definitions.

REGISTER 29-15: CiFLTCON5: CAN FILTER CONTROL REGISTER 5

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN23	MSEL23<1:0>		FSEL23<4:0>				
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN22	MSEL22<1:0>		FSEL22<4:0>				
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN21	MSEL21<1:0>		FSEL21<4:0>				
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FLTEN20	MSEL20<1:0>		FSEL20<4:0>				

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **FLTEN23:** Filter 23 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 30-29 **MSEL23<1:0>:** Filter 23 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 28-24 **FSEL23<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

bit 23 **FLTEN22:** Filter 22 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 22-21 **MSEL22<1:0>:** Filter 22 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 20-16 **FSEL22<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

Note: The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

REGISTER 30-31: EMAC1MCFG: ETHERNET CONTROLLER MAC MII MANAGEMENT CONFIGURATION REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	RESETMGMT	—	—	—	—	—	—	—
7:0	U-0	U-0	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	CLKSEL<3:0>(1)				NOPRE	SCANINC

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **RESETMGMT:** Test Reset MII Management bit
1 = Reset the MII Management module
0 = Normal Operation

bit 14-6 **Unimplemented:** Read as '0'

bit 5-2 **CLKSEL<3:0>:** MII Management Clock Select 1 bits(1)
These bits are used by the clock divide logic in creating the MII Management Clock (MDC), which the IEEE 802.3 Specification defines to be no faster than 2.5 MHz. Some PHYs support clock rates up to 12.5 MHz.

bit 1 **NOPRE:** Suppress Preamble bit
1 = The MII Management will perform read/write cycles without the 32-bit preamble field. Some PHYs support suppressed preamble
0 = Normal read/write cycles are performed

bit 0 **SCANINC:** Scan Increment bit
1 = The MII Management module will perform read cycles across a range of PHYs. The read cycles will start from address 1 through the value set in EMAC1MADR<PHYADDR>
0 = Continuous reads of the same PHY

Note 1: Table 30-7 provides a description of the clock divider encoding.

Note: Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware.

TABLE 30-7: MIIM CLOCK SELECTION

MIIM Clock Select	EMAC1MCFG<5:2>
TPBCLK5 divided by 4	000x
TPBCLK5 divided by 6	0010
TPBCLK5 divided by 8	0011
TPBCLK5 divided by 10	0100
TPBCLK5 divided by 14	0101
TPBCLK5 divided by 20	0110
TPBCLK5 divided by 28	0111
TPBCLK5 divided by 40	1000
TPBCLK5 divided by 48	1001
TPBCLK5 divided by 50	1010
Undefined	Any other combination

31.0 COMPARATOR

Note: This data sheet summarizes the features of the PIC32MZ EF family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 19. "Comparator"** (DS60001110) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

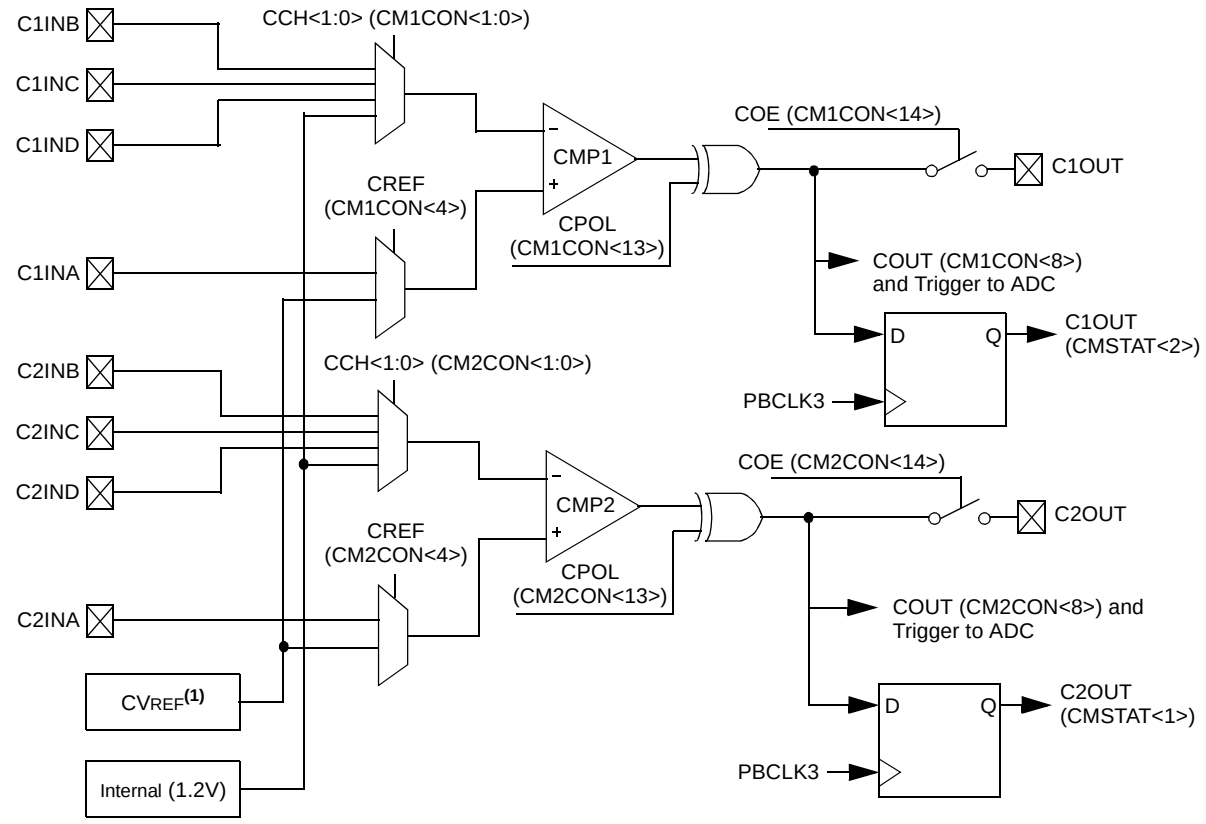
The Analog Comparator module consists of two comparators that can be configured in a variety of ways.

The following are key features of the Analog Comparator module:

- Differential inputs
- Rail-to-rail operation
- Selectable output polarity
- Selectable inputs:
  - Analog inputs multiplexed with I/O pins
  - On-chip internal absolute voltage reference
  - Comparator voltage reference (CVREF)
- Selectable interrupt generation

A block diagram of the comparator module is illustrated in Figure 31-1.

FIGURE 31-1: COMPARATOR BLOCK DIAGRAM



Note 1: Internally connected. See **Section 32.0 "Comparator Voltage Reference (CVREF)"** for more information.

FIGURE 37-12: SPIx MODULE SLAVE MODE (CKE = 0) TIMING CHARACTERISTICS

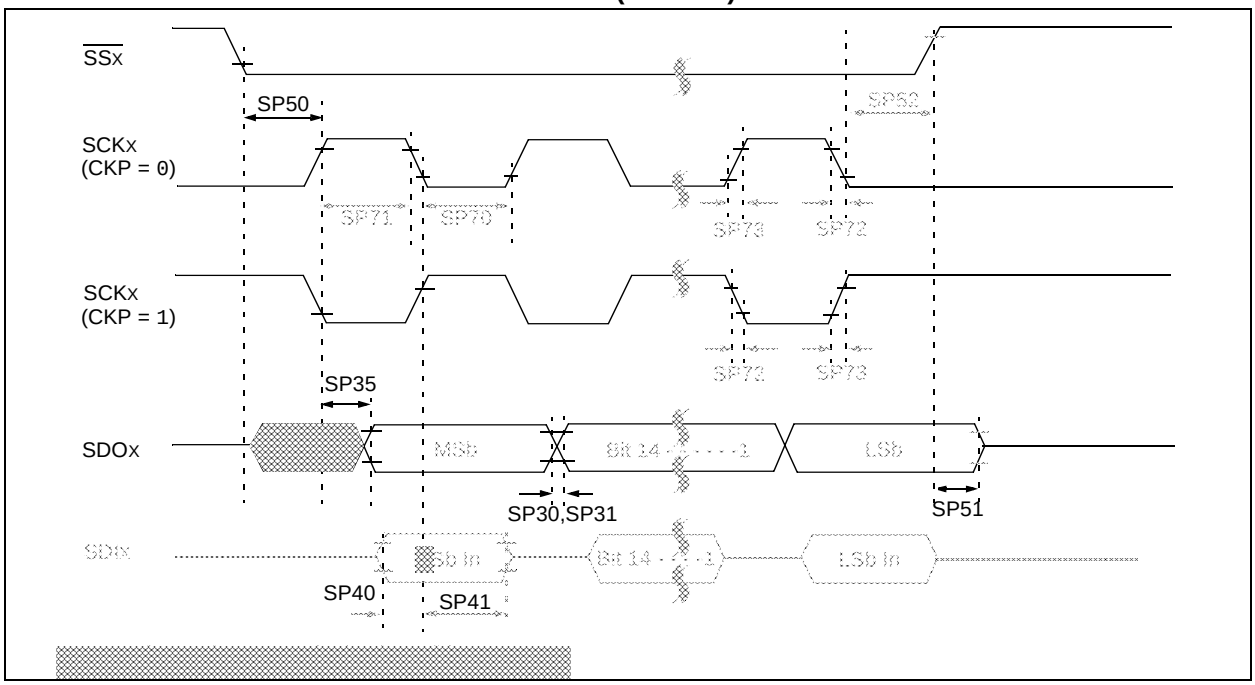


TABLE 37-32: SPIx MODULE SLAVE MODE (CKE = 0) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
SP70	TscL	SCKx Input Low Time **(Note 3)**	Tsck/2	—	—	ns	—
SP71	TscH	SCKx Input High Time **(Note 3)**	Tsck/2	—	—	ns	—
SP72	TscF	SCKx Input Fall Time	—	—	—	ns	See parameter DO32
SP73	TscR	SCKx Input Rise Time	—	—	—	ns	See parameter DO31
SP30	TdoF	SDOx Data Output Fall Time **(Note 4)**	—	—	—	ns	See parameter DO32
SP31	TdoR	SDOx Data Output Rise Time **(Note 4)**	—	—	—	ns	See parameter DO31
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	—	7	ns	VDD > 2.7V
			—	—	10	ns	VDD < 2.7V
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	5	—	—	ns	—
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	5	—	—	ns	—
SP50	TssL2scH, TssL2scL	$\overline{SSx}$ ↓ to SCKx ↑ or SCKx Input	88	—	—	ns	—
SP51	TssH2doZ	$\overline{SSx}$ ↑ to SDOx Output High-Impedance **(Note 3)**	2.5	—	12	ns	—
SP52	TscH2ssH TscL2ssH	$\overline{SSx}$ after SCKx Edge	10	—	—	ns	—

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: The minimum clock period for SCKx is 20 ns.

4: Assumes 30 pF load on all SPIx pins.

FIGURE 37-23: PARALLEL MASTER PORT WRITE TIMING DIAGRAM

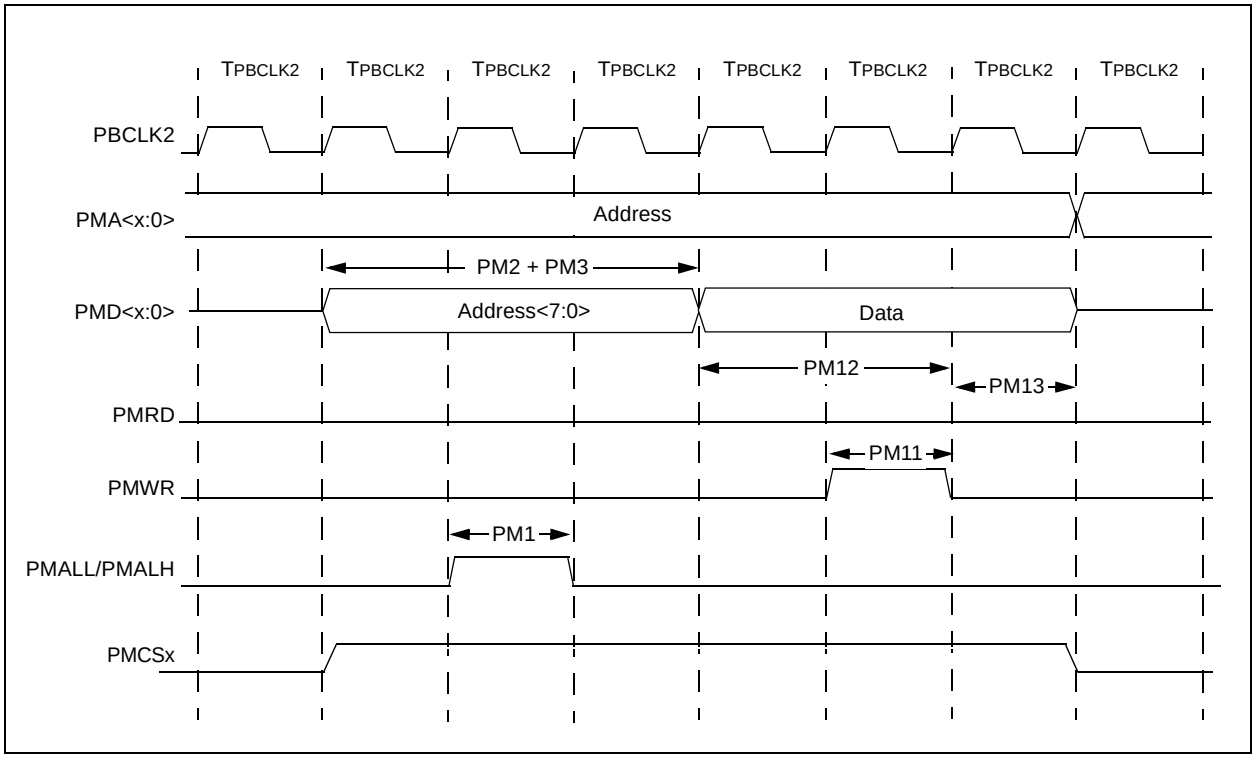


TABLE 37-44: PARALLEL MASTER PORT WRITE TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
PM11	TWR	PMWR Pulse Width	—	1 TPBCLK2	—	—	—
PM12	TDVSU	Data Out Valid before PMWR or PMENB goes Inactive (data setup time)	—	2 TPBCLK2	—	—	—
PM13	TDVHOLD	PMWR or PMEMB Invalid to Data Out Invalid (data hold time)	—	1 TPBCLK2	—	—	—

Note 1: These parameters are characterized, but not tested in manufacturing.

TABLE A-9: FLASH PROGRAMMING DIFFERENCES (CONTINUED)

PIC32MX5XX/6XX/7XX Feature	PIC32MZ EF Feature
Flash Programming	
	The op codes for programming the Flash memory have been changed to accommodate the new quad-word programming and dual-panel features. The row size has changed to 2 KB (512 IW) from 128 IW. The page size has changed to 16 KB (4K IW) from 4 KB (1K IW). Note that the NVMOP register is now protected, and requires the WREN bit be set to enable modification.
NVMOP<3:0> (NVMCON<3:0>) 1111 = Reserved • • • **0111 = Reserved** **0110 = No operation** **0101 = Program Flash (PFM) erase operation** 0100 = Page erase operation 0011 = Row program operation **0010 = No operation** 0001 = Word program operation 0000 = No operation	NVMOP<3:0> (NVMCON<3:0>) 1111 = Reserved • • • 1000 = Reserved **0111 = Program erase operation** **0110 = Upper program Flash memory erase operation** **0101 = Lower program Flash memory erase operation** 0100 = Page erase operation 0011 = Row program operation **0010 = Quad Word (128-bit) program operation** 0001 = Word program operation 0000 = No operation
PIC32MX devices feature a single NVMDATA register for word programming. NVMDATA	On PIC32MZ EF devices, to support quad word programming, the NVMDATA register has been expanded to four words. NVMDATA**x**, where 'x' = 0 through 3
Flash Endurance and Retention	
PIC32MX devices support Flash endurance and retention of up to 20K E/W cycles and 20 years.	On PIC32MZ EF devices, ECC must be enabled to support the same endurance and retention as PIC32MX devices.
Configuration Words	
On PIC32MX devices, Configuration Words can be programmed with **Word or Row program** operation.	On PIC32MZ EF devices, all Configuration Words must be programmed with **Quad Word or Row Program** operations.
Configuration Words Reserved Bit	
On PIC32MX devices, the **DEVCFG0<15>** bit is Reserved and must be programmed to '0'.	On PIC32MZ EF devices, this bit is **DEVSIGN0<31>**.

A.10 Package Differences

In general, PIC32MZ EF devices are mostly pin compatible with PIC32MX5XX/6XX/7XX devices; however, some pins are not. In particular, the VDD and VSS pins have been added and moved to different pins. In addition, I/O functions that were on fixed pins now will largely be on remappable pins.

TABLE A-11: PACKAGE DIFFERENCES

PIC32MX5XX/6XX/7XX Feature	PIC32MZ EF Feature
VCAP Pin	
On PIC32MX devices, an external capacitor is required between a VCAP pin and GND, which provides a filtering capacitor for the internal voltage regulator.	On PIC32MZ EF devices, this requirement has been removed.
A low-ESR capacitor (typically 10 µF) is required on the VCAP pin.	No VCAP pin.
VDD and VSS Pins	
	There are more VDD pins on PIC32MZ EF devices, and many are located on different pins.
VDD on 64-pin packages: 10, 26, 38, 57 VDD on 100-pin packages: 2, 16, 37, 46, 62, 86	VDD on 64-pin packages: 8, 26, 39, 54, 60 VDD on 100-pin packages: 14, 37, 46, 62, 74, 83, 93
	There are more VSS pins on PIC32MZ EF devices, and many are located on different pins.
VSS on 64-pin packages: 9, 25, 41 VSS on 100-pin packages: 15, 36, 45, 65, 75	VSS on 64-pin packages: 7, 25, 35, 40, 55, 59 VSS on 100-pin packages: 13, 36, 45, 53, 63, 75, 84, 92
PPS I/O Pins	
	Peripheral functions on PIC32MZ EF devices are now routed through a PPS module, which routes the signals to the desired pins. When migrating software, it is necessary to initialize the PPS I/O functions in order to get the signal to and from the correct pin.
All peripheral functions are fixed as to what pin upon which they operate.	PPS functionality for the following peripherals: • CAN • UART • SPI (except SCK) • Input Capture • Output Compare • External Interrupt (except INT0) • Timer Clocks (except Timer1) • Reference Clocks (except REFCLK2)