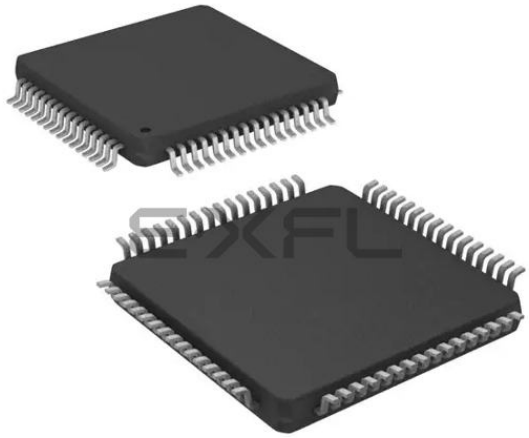
Microchip Technology - PIC32MZ2048EFM064-E/PT Datasheet



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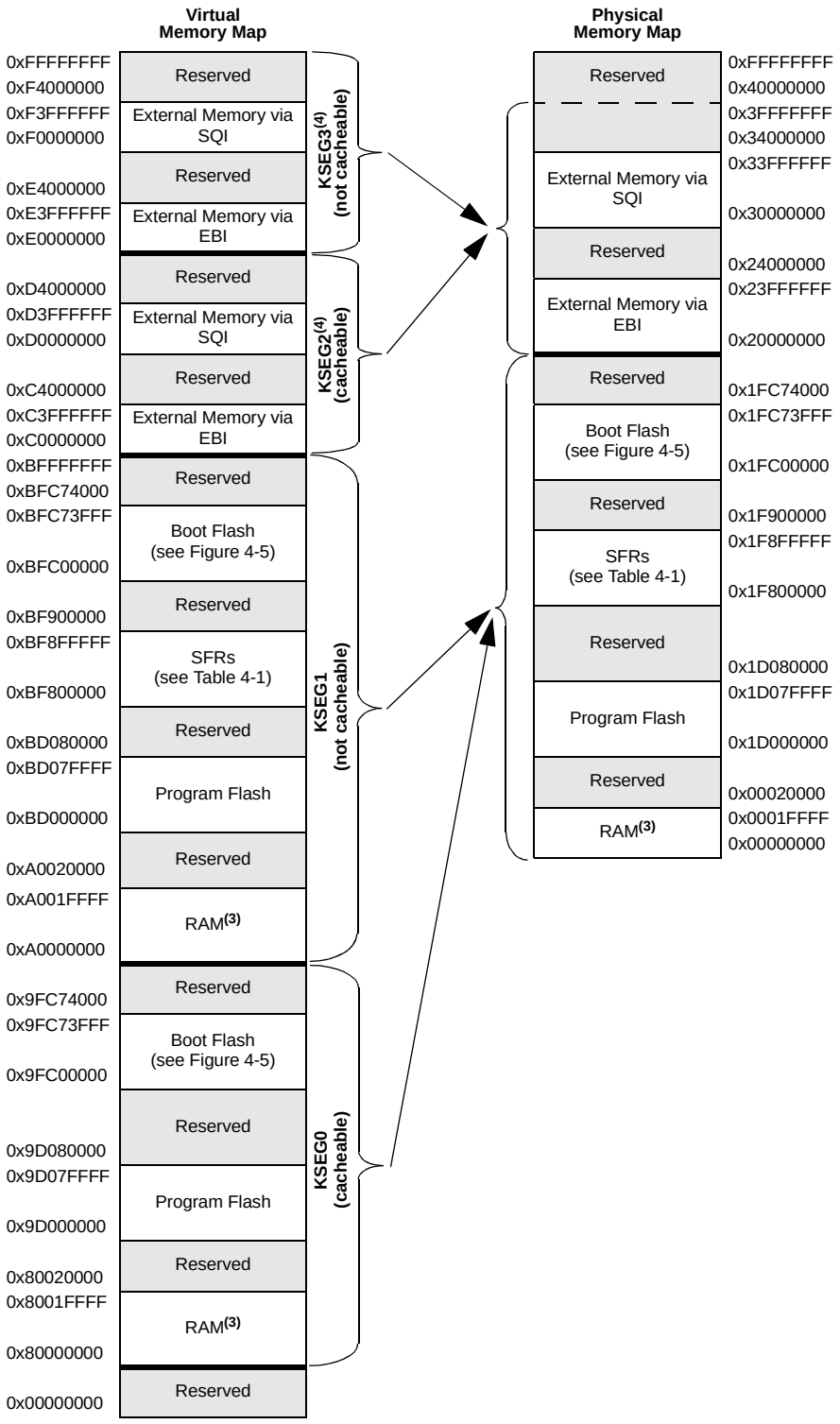
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® M-Class
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	CANbus, Ethernet, I²C, PMP, SPI, SQI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	46
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	2.1V ~ 3.6V
Data Converters	A/D 24x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mz2048efm064-e-pt

FIGURE 4-1: MEMORY MAP FOR DEVICES WITH 512 KB OF PROGRAM MEMORY(1,2)



Note 1: Memory areas are not shown to scale.
2: The Cache, MMU, and TLB are initialized by compiler start-up code.
3: RAM memory is divided into two equal banks: RAM Bank 1 and RAM Bank 2 on a half boundary.
4: The MMU must be enabled and the TLB must be set up to access this segment.

REGISTER 4-6: SBTxECLRS: SYSTEM BUS TARGET 'x' SINGLE ERROR CLEAR REGISTER ('x' = 0-13)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	R-0
	—	—	—	—	—	—	—	CLEAR

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared

bit 31-1 **Unimplemented:** Read as '0'

bit 0 **CLEAR:** Clear Single Error on Read bit
A single error as reported via SBTxELOG1 and SBTxELOG2 is cleared by a read of this register.

Note: Refer to Table 4-6 for the list of available targets and their descriptions.

REGISTER 4-7: SBTxECLRM: SYSTEM BUS TARGET 'x' MULTIPLE ERROR CLEAR REGISTER ('x' = 0-13)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	R-0
	—	—	—	—	—	—	—	CLEAR

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared

bit 31-1 **Unimplemented:** Read as '0'

bit 0 **CLEAR:** Clear Multiple Errors on Read bit
Multiple errors as reported via SBTxELOG1 and SBTxELOG2 is cleared by a read of this register.

Note: Refer to Table 4-6 for the list of available targets and their descriptions.

REGISTER 7-2: PRISS: PRIORITY SHADOW SELECT REGISTER (CONTINUED)

bit 15-12 **PRI3SS<3:0>:** Interrupt with Priority Level 3 Shadow Set bits(1)
1xxx = Reserved (by default, an interrupt with a priority level of 3 uses Shadow Set 0)
0111 = Interrupt with a priority level of 3 uses Shadow Set 7
0110 = Interrupt with a priority level of 3 uses Shadow Set 6
•
•
•
0001 = Interrupt with a priority level of 3 uses Shadow Set 1
0000 = Interrupt with a priority level of 3 uses Shadow Set 0

bit 11-8 **PRI2SS<3:0>:** Interrupt with Priority Level 2 Shadow Set bits(1)
1xxx = Reserved (by default, an interrupt with a priority level of 2 uses Shadow Set 0)
0111 = Interrupt with a priority level of 2 uses Shadow Set 7
0110 = Interrupt with a priority level of 2 uses Shadow Set 6
•
•
•
0001 = Interrupt with a priority level of 2 uses Shadow Set 1
0000 = Interrupt with a priority level of 2 uses Shadow Set 0

bit 7-4 **PRI1SS<3:0>:** Interrupt with Priority Level 1 Shadow Set bits(1)
1xxx = Reserved (by default, an interrupt with a priority level of 1 uses Shadow Set 0)
0111 = Interrupt with a priority level of 1 uses Shadow Set 7
0110 = Interrupt with a priority level of 1 uses Shadow Set 6
•
•
•
0001 = Interrupt with a priority level of 1 uses Shadow Set 1
0000 = Interrupt with a priority level of 1 uses Shadow Set 0

bit 3-1 **Unimplemented:** Read as '0'

bit 0 **SS0:** Single Vector Shadow Register Set bit
1 = Single vector is presented with a shadow set
0 = Single vector is not presented with a shadow set

Note 1: These bits are ignored if the MVEC bit (INTCON<12>) = 0.

TABLE 11-1: USB REGISTER MAP 1 (CONTINUED)

Virtual Address (BF8E_#)	Register Name	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
3340	USB DPBFD	31:16	—	—	—	—	—	—	—	—	EP7TXD	EP6TXD	EP5TXD	EP4TXD	EP3TXD	EP2TXD	EP1TXD	—	0000
		15:0	—	—	—	—	—	—	—	—	EP7RXD	EP6RXD	EP5RXD	EP4RXD	EP3RXD	EP2RXD	EP1RXD	—	0000
3344	USB TMCON1	31:16	THHSRTN<15:0>																05E6
		15:0	TUCH<15:0>																4074
3348	USB TMCON2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	THSBT<3:0>				0000
3360	USB LPMR1	31:16	—	—	LPM ERRIE	LPM RESIE	LPMACKIE	LPMNYIE	LPMSTIE	LPMTOIE	—	—	—	LPMNAK(1)	LPMEN<1:0>		LPMRES	LPMXMT	0000
														__(2)	__(2)	__(2)			0000
		15:0	ENDPOINT<3:0>				—	—	—	RMTWAK	HIRD<3:0>				LNKSTATE<3:0>				0000
3364	USB LPMR2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	LPMFADDR<6:0>							—	—	LPMERR(1)	LPMRES	LPMNC	LPMACK	LPMNY	LPMST	0000
													__(2)						0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: Device mode.
2: Host mode.
3: Definition for Endpoint 0 (ENDPOINT<3:0> (USBCSR<19:16>) = 0).
4: Definition for Endpoints 1-7 (ENDPOINT<3:0> (USBCSR<19:16>) = 1 through 7).

TABLE 11-2: USB REGISTER MAP 2

Virtual Address (BF88_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
4000	USB CRCON	31:16	—	—	—	—	—	USBIF	USBRF	USBWKUP	—	—	—	—	—	—	—	—	0100
		15:0	—	—	—	—	—	—	USB IDOVEN	USB IDVAL	PHYIDEN	VBUS MONEN	ASVAL MONEN	BSVAL MONEN	SEND MONEN	USBIE	USBRIE	USB WKUPEN	8000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

21.0 INTER-INTEGRATED CIRCUIT (I^2C)

Note: This data sheet summarizes the features of the PIC32MZ EF family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 24. "Inter-Integrated Circuit (I^2C)"** (DS60001116) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

The I^2C module provides complete hardware support for both Slave and Multi-Master modes of the I^2C serial communication standard.

Each I^2C module has a 2-pin interface:

- SCLx pin is clock
- SDAx pin is data

Each I^2C module offers the following key features:

- I^2C interface supporting both master and slave operation
- I^2C Slave mode supports 7-bit and 10-bit addressing
- I^2C Master mode supports 7-bit and 10-bit addressing
- I^2C port allows bidirectional transfers between master and slaves
- Serial clock synchronization for the I^2C port can be used as a handshake mechanism to suspend and resume serial transfer (SCLREL control)
- I^2C supports multi-master operation; detects bus collision and arbitrates accordingly
- Provides support for address bit masking
- SMBus support

Figure 21-1 illustrates the I^2C module block diagram.

REGISTER 21-1: I2CxCON: I²C CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	PCIE	SCIE	BOEN	SDAHT	SBCDE	AHEN	DHEN
15:8	R/W-0	U-0	R/W-0	R/W-1, HC	R/W-0	R/W-0	R/W-0	R/W-0
	ON	—	SIDL	SCKREL	STRICT	A10M	DISSLW	SMEN
7:0	R/W-0	R/W-0	R/W-0	R/W-0, HC	R/W-0, HC	R/W-0, HC	R/W-0, HC	R/W-0, HC
	GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN

Legend:	HC = Cleared in Hardware		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-23 **Unimplemented:** Read as '0'

bit 22 **PCIE:** Stop Condition Interrupt Enable bit (I²C Slave mode only)
- 1 = Enable interrupt on detection of Stop condition
- 0 = Stop detection interrupts are disabled

bit 21 **SCIE:** Start Condition Interrupt Enable bit (I²C Slave mode only)
- 1 = Enable interrupt on detection of Start or Restart conditions
- 0 = Start detection interrupts are disabled

bit 20 **BOEN:** Buffer Overwrite Enable bit (I²C Slave mode only)
- 1 = I2CxRCV is updated and $\overline{\text{ACK}}$ is generated for a received address/data byte, ignoring the state of the I2COV bit (I2CxSTAT<6>)only if the RBF bit (I2CxSTAT<2>) = 0
- 0 = I2CxRCV is only updated when the I2COV bit (I2CxSTAT<6>) is clear

bit 19 **SDAHT:** SDA Hold Time Selection bit
- 1 = Minimum of 300 ns hold time on SDA after the falling edge of SCL
- 0 = Minimum of 100 ns hold time on SDA after the falling edge of SCL

bit 18 **SBCDE:** Slave Mode Bus Collision Detect Enable bit (I²C Slave mode only)
- 1 = Enable slave bus collision interrupts
- 0 = Slave bus collision interrupts are disabled

bit 18 **AHEN:** Address Hold Enable bit (Slave mode only)
- 1 = Following the 8th falling edge of SCL for a matching received address byte; SCKREL bit will be cleared and the SCL will be held low.
- 0 = Address holding is disabled

bit 16 **DHEN:** Data Hold Enable bit (I²C Slave mode only)
- 1 = Following the 8th falling edge of SCL for a received data byte; slave hardware clears the SCKREL bit and SCL is held low
- 0 = Data holding is disabled

bit 15 **ON:** I²C Enable bit
- 1 = Enables the I²C module and configures the SDA and SCL pins as serial port pins
- 0 = Disables the I²C module; all I²C pins are controlled by PORT functions

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit
- 1 = Discontinue module operation when device enters Idle mode
- 0 = Continue module operation in Idle mode

REGISTER 23-8: PMWADDR: PARALLEL PORT WRITE ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	WCS2(1)	WCS1(3)	WADDR<13:8>					
	WADDR15(2)	WADDR14(4)						
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	WADDR<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **WCS2:** Chip Select 2 bit(1)
- 1 = Chip Select 2 is active
- 0 = Chip Select 2 is inactive

bit 15 **WADDR<15>:** Target Address bit 15(2)

bit 14 **WCS1:** Chip Select 1 bit(3)
- 1 = Chip Select 1 is active
- 0 = Chip Select 1 is inactive

bit 14 **WADDR<14>:** Target Address bit 14(4)

bit 13-0 **WADDR<13:0>:** Address bits

Note 1: When the CSF<1:0> bits (PMCON<7:6>) = 10 or 01.
2: When the CSF<1:0> bits (PMCON<7:6>) = 00.
3: When the CSF<1:0> bits (PMCON<7:6>) = 10.
4: When the CSF<1:0> bits (PMCON<7:6>) = 00 or 01.

Note: This register is only used when the DUALBUF bit (PMCON<17>) is set to '1'.

REGISTER 25-1: RTCCON: REAL-TIME CLOCK AND CALENDAR CONTROL REGISTER (CONTINUED)

bit 10-9 **RTCCLKSEL<1:0>:** RTCC Clock Select bits

When a new value is written to these bits, the Seconds Value register should also be written to properly reset the clock prescalers in the RTCC.

11 = Reserved
10 = Reserved
01 = RTCC uses the external 32.768 kHz Secondary Oscillator (SOSC)
00 = RTCC uses the internal 32 kHz oscillator (LPRC)

bit 8-7 **RTCOUTSEL<1:0>:** RTCC Output Data Select bits(2)

11 = Reserved
10 = RTCC Clock is presented on the RTCC pin
01 = Seconds Clock is presented on the RTCC pin
00 = Alarm Pulse is presented on the RTCC pin when the alarm interrupt is triggered

bit 6 **RTCCLKON:** RTCC Clock Enable Status bit(5)

1 = RTCC Clock is actively running
0 = RTCC Clock is not running

bit 5-4 **Unimplemented:** Read as '0'

bit 3 **RTCWREN:** Real-Time Clock Value Registers Write Enable bit(3)

1 = Real-Time Clock Value registers can be written to by the user
0 = Real-Time Clock Value registers are locked out from being written to by the user

bit 2 **RTCSYNC:** Real-Time Clock Value Registers Read Synchronization bit

1 = Real-time clock value registers can change while reading (due to a rollover ripple that results in an invalid data read). If the register is read twice and results in the same data, the data can be assumed to be valid.
0 = Real-time clock value registers can be read without concern about a rollover ripple

bit 1 **HALFSEC:** Half-Second Status bit(4)

1 = Second half period of a second
0 = First half period of a second

bit 0 **RTCOE:** RTCC Output Enable bit

1 = RTCC output is enabled
0 = RTCC output is not enabled

Note 1: The ON bit is only writable when RTCWREN = 1.
2: Requires RTCOE = 1 (RTCCON<0>) for the output to be active.
3: The RTCWREN bit can be set only when the write sequence is enabled.
4: This bit is read-only. It is cleared to '0' on a write to the seconds bit fields (RTCTIME<14:8>).
5: This bit is undefined when RTCCLKSEL<1:0> = 00 (LPRC is the clock source).

Note:	This register is reset only on a Power-on Reset (POR).

REGISTER 25-2: RTCALRM: REAL-TIME CLOCK ALARM CONTROL REGISTER (CONTINUED)

bit 7-0 **ARPT<7:0>:** Alarm Repeat Counter Value bits(2)

11111111 = Alarm will trigger 256 times
•
•
•
00000000 = Alarm will trigger one time
The counter decrements on any alarm event. The counter only rolls over from 0x00 to 0xFF if CHIME = 1.

Note 1: Hardware clears the ALRMEN bit anytime the alarm event occurs, when ARPT<7:0> = 00 and CHIME = 0.

2: This field should not be written when the RTCC ON bit = '1' (RTCCON<15>) and ALRMSYNC = 1.

Note:	This register is reset only on a Power-on Reset (POR).

REGISTER 28-30: ADCEISTAT1: ADC EARLY INTERRUPT STATUS REGISTER 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	EIRDY31(1)	EIRDY30(1)	EIRDY29(1)	EIRDY28(1)	EIRDY27(1)	EIRDY26(1)	EIRDY25(1)	EIRDY24(1)
23:16	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	EIRDY23(1)	EIRDY22(1)	EIRDY21(1)	EIRDY20(1)	EIRDY19(1)	EIRDY18	EIRDY17	EIRDY16
15:8	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	EIRDY15	EIRDY14	EIRDY13	EIRDY12	EIRDY11	EIRDY10	EIRDY9	EIRDY8
7:0	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	EIRDY7	EIRDY6	EIRDY5	EIRDY4	EIRDY3	EIRDY2	EIRDY1	EIRDY0

Legend:	HS = Hardware Set	HC = Hardware Cleared	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **EIRDY31:EIRDY0:** Early Interrupt for Corresponding Analog Input Ready bits

1 = This bit is set when the early interrupt event occurs for the specified analog input. An interrupt will be generated if early interrupts are enabled in the ADCEIEN1 register. For the Class 1 analog inputs, this bit will set as per the configuration of the ADCEIS<2:0> bits in the ADCxTIME register. For the shared ADC module, this bit will be set as per the configuration of the ADCEIS<2:0> bits in the ADCCON2 register.

0 = Interrupts are disabled

Note 1: This bit is not available on 64-pin devices.

NOTES:

TABLE 29-1: CAN1 REGISTER SUMMARY FOR PIC32MZXXXXECF AND PIC32MZXXXXECH DEVICES (CONTINUED)

Virtual Address (BF88_#)	Register Name(1)	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
00F0	C1FLTCON3	31:16	FLTEN15	MSEL15<1:0>		FSEL15<4:0>					FLTEN14	MSEL14<1:0>		FSEL14<4:0>					0000
		15:0	FLTEN13	MSEL13<1:0>		FSEL13<4:0>					FLTEN12	MSEL12<1:0>		FSEL12<4:0>					0000
0100	C1FLTCON4	31:16	FLTEN19	MSEL19<1:0>		FSEL19<4:0>					FLTEN18	MSEL18<1:0>		FSEL18<4:0>					0000
		15:0	FLTEN17	MSEL17<1:0>		FSEL17<4:0>					FLTEN16	MSEL16<1:0>		FSEL16<4:0>					0000
0110	C1FLTCON5	31:16	FLTEN23	MSEL23<1:0>		FSEL23<4:0>					FLTEN22	MSEL22<1:0>		FSEL22<4:0>					0000
		15:0	FLTEN21	MSEL21<1:0>		FSEL21<4:0>					FLTEN20	MSEL20<1:0>		FSEL20<4:0>					0000
0120	C1FLTCON6	31:16	FLTEN27	MSEL27<1:0>		FSEL27<4:0>					FLTEN26	MSEL26<1:0>		FSEL26<4:0>					0000
		15:0	FLTEN25	MSEL25<1:0>		FSEL25<4:0>					FLTEN24	MSEL24<1:0>		FSEL24<4:0>					0000
0130	C1FLTCON7	31:16	FLTEN31	MSEL31<1:0>		FSEL31<4:0>					FLTEN30	MSEL30<1:0>		FSEL30<4:0>					0000
		15:0	FLTEN29	MSEL29<1:0>		FSEL29<4:0>					FLTEN28	MSEL28<1:0>		FSEL28<4:0>					0000
0140-0330	C1RXFn (n = 0-31)	31:16	SID<10:0>											-—	EXID	—	EID<17:16>		xxxx
		15:0	EID<15:0>																xxxx
0340	C1FIFOBA	31:16	C1FIFOBA<31:0>																0000
		15:0																	0000
0350	C1FIFOCONn (n = 0)	31:16	—	—	—	—	—	—	—	—	—	—	—	FSIZE<4:0>					0000
		15:0	—	FRESET	UINC	DONLY	—	—	—	—	TXEN	TXABAT	TXLARB	TXERR	TXREQ	RTREN	TXPRI<1:0>		0000
0360	C1FIFOINTn (n = 0)	31:16	—	—	—	—	—	TXNFULLIE	TXHALFIE	TXEMPTYIE	—	—	—	—	RXOVFLIE	RXFULLIE	RXHALFIE	RXN EMPTYIE	0000
		15:0	—	—	—	—	—	TXNFULLIF	TXHALFIF	TXEMPTYIF	—	—	—	—	RXOVFLIF	RXFULLIF	RXHALFIF	RXN EMPTYIF	0000
0370	C1FIFOUAn (n = 0)	31:16	C1FIFOUA<31:0>																0000
		15:0																	0000
0380	C1FIFOCIn (n = 0)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	C1FIFOCI<4:0>					0000
0390-0B40	C1FIFOCONn C1FIFOINTn C1FIFOUAn C1FIFOCIn (n = 1-31)	31:16	—	—	—	—	—	—	—	—	—	—	—	FSIZE<4:0>					0000
		15:0	—	FRESET	UINC	DONLY	—	—	—	—	TXEN	TXABAT	TXLARB	TXERR	TXREQ	RTREN	TXPRI<1:0>		0000
		31:16	—	—	—	—	—	TXNFULLIE	TXHALFIE	TXEMPTYIE	—	—	—	—	RXOVFLIE	RXFULLIE	RXHALFIE	RXN EMPTYIE	0000
		15:0	—	—	—	—	—	TXNFULLIF	TXHALFIF	TXEMPTYIF	—	—	—	—	RXOVFLIF	RXFULLIF	RXHALFIF	RXN EMPTYIF	0000
		31:16	C1FIFOUA<31:0>																0000
		15:0																	0000
		31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	C1FIFOCI<4:0>					0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 "CLR, SET, and INV Registers"** for more information.

REGISTER 29-12: CiFLTCON2: CAN FILTER CONTROL REGISTER 2 (CONTINUED)

bit 15 **FLTEN9:** Filter 9 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 14-13 **MSEL9<1:0>:** Filter 9 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 12-8 **FSEL9<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

bit 7 **FLTEN8:** Filter 8 Enable bit
1 = Filter is enabled
0 = Filter is disabled

bit 6-5 **MSEL8<1:0>:** Filter 8 Mask Select bits
11 = Acceptance Mask 3 selected
10 = Acceptance Mask 2 selected
01 = Acceptance Mask 1 selected
00 = Acceptance Mask 0 selected

bit 4-0 **FSEL8<4:0>:** FIFO Selection bits
11111 = Message matching filter is stored in FIFO buffer 31
11110 = Message matching filter is stored in FIFO buffer 30
•
•
•
00001 = Message matching filter is stored in FIFO buffer 1
00000 = Message matching filter is stored in FIFO buffer 0

Note: The bits in this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.

REGISTER 30-9: ETHPMCS: ETHERNET CONTROLLER PATTERN MATCH CHECKSUM REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PMCS<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PMCS<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-8 **PMCS<15:8>:** Pattern Match Checksum 1 bits

bit 7-0 **PMCS<7:0>:** Pattern Match Checksum 0 bits

Note 1: This register is only used for RX operations.

2: The bits in this register may only be changed while the RXEN bit (ETHCON1<8>) = 0 or the PMMODE bit (ETHRXFC<11:8>) = 0.

REGISTER 30-10: ETHPMO: ETHERNET CONTROLLER PATTERN MATCH OFFSET REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PMO<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PMO<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **PMO<15:0>:** Pattern Match Offset 1 bits

Note 1: This register is only used for RX operations.

2: The bits in this register may only be changed while the RXEN bit (ETHCON1<8>) = 0 or the PMMODE bit (ETHRXFC<11:8>) = 0.

REGISTER 34-3: DEVCFG0/ADEVCFG0: DEVICE CONFIGURATION WORD 0 (CONTINUED)

bit 10 **FSLEEP:** Flash Sleep Mode bit
1 = Flash is powered down when the device is in Sleep mode
0 = Flash remains powered when the device is in Sleep mode

bit 9-8 **FECCCON<1:0>:** Dynamic Flash ECC Configuration bits
Upon a device Reset, the value of these bits is copied to the ECCCON<1:0> bits (CFGCON<5:4>).
11 = ECC and dynamic ECC are disabled (ECCCON<1:0> bits are writable)
10 = ECC and dynamic ECC are disabled (ECCCON<1:0> bits are locked)
01 = Dynamic Flash ECC is enabled (ECCCON<1:0> bits are locked)
00 = Flash ECC is enabled (ECCCON<1:0> bits are locked; disables word Flash writes)

bit 7 **Reserved:** Write as '1'

bit 6 **BOOTISA:** Boot ISA Selection bit
1 = Boot code and Exception code is MIPS32®
(ISAONEXC bit is set to '0' and the ISA<1:0> bits are set to '10' in the CP0 Config3 register)
0 = Boot code and Exception code is microMIPS™
(ISAONEXC bit is set to '1' and the ISA<1:0> bits are set to '11' in the CP0 Config3 register)

bit 5 **TRCEN:** Trace Enable bit
1 = Trace features in the CPU are enabled
0 = Trace features in the CPU are disabled

bit 4-3 **ICESEL<1:0>:** In-Circuit Emulator/Debugger Communication Channel Select bits
11 = PGEC1/PGED1 pair is used
10 = PGEC2/PGED2 pair is used
01 = Reserved
00 = Reserved

bit 2 **JTAGEN:** JTAG Enable bit(1)
1 = JTAG is enabled
0 = JTAG is disabled

bit 1-0 **DEBUG<1:0>:** Background Debugger Enable bits (forced to '11' if code-protect is enabled)
1x = Debugger is disabled
0x = Debugger is enabled

Note 1: This bit sets the value of the JTAGEN bit in the CFGCON register.

TABLE 37-7: DC CHARACTERISTICS: IDLE CURRENT (IIDLE)

DC CHARACTERISTICS			Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial	
Parameter No.	**Typical(2)**	**Maximum(4)**	**Units**	**Conditions**
Idle Current (IIDLE): Core Off, Clock on Base Current (Note 1)				
DC30a	7	22	mA	4 MHz **(Note 3)**
DC31a	8	24	mA	10 MHz
DC32a	13	32	mA	60 MHz **(Note 3)**
DC33a	21	42	mA	130 MHz **(Note 3)**
DC34	26	48	mA	180 MHz **(Note 3)**
DC35	28	52	mA	200 MHz

Note 1: The test conditions for IIDLE current measurements are as follows:

- Oscillator mode is EC (for 8 MHz and below) and EC+PLL (for above 8 MHz) with OSC1 driven by external square wave from rail-to-rail, (OSC1 input clock input over/undershoot < 100 mV required)
- OSC2/CLKO is configured as an I/O input pin
- USB PLL is disabled (USBPMD = 1), VUSB3V3 is connected to VSS, PBCLKx divisor = 1:128 ('x' ≠ 7)
- CPU is in Idle mode (CPU core Halted)
- L1 Cache and Prefetch modules are disabled
- No peripheral modules are operating, (ON bit = 0), but the associated PMD bit is cleared (except USBPMD)
- WDT, DMT, Clock Switching, Fail-Safe Clock Monitor, and Secondary Oscillator are disabled
- All I/O pins are configured as inputs and pulled to VSS
- $\overline{MCLR}$ = VDD
- RTCC and JTAG are disabled

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: This parameter is characterized, but not tested in manufacturing.

4: Data in the "Maximum" column is at 3.3V, +85ºC at specified operating frequency, unless otherwise stated. Parameters are for design guidance only and are not tested.

FIGURE 37-13: SPIx MODULE SLAVE MODE (CKE = 1) TIMING CHARACTERISTICS

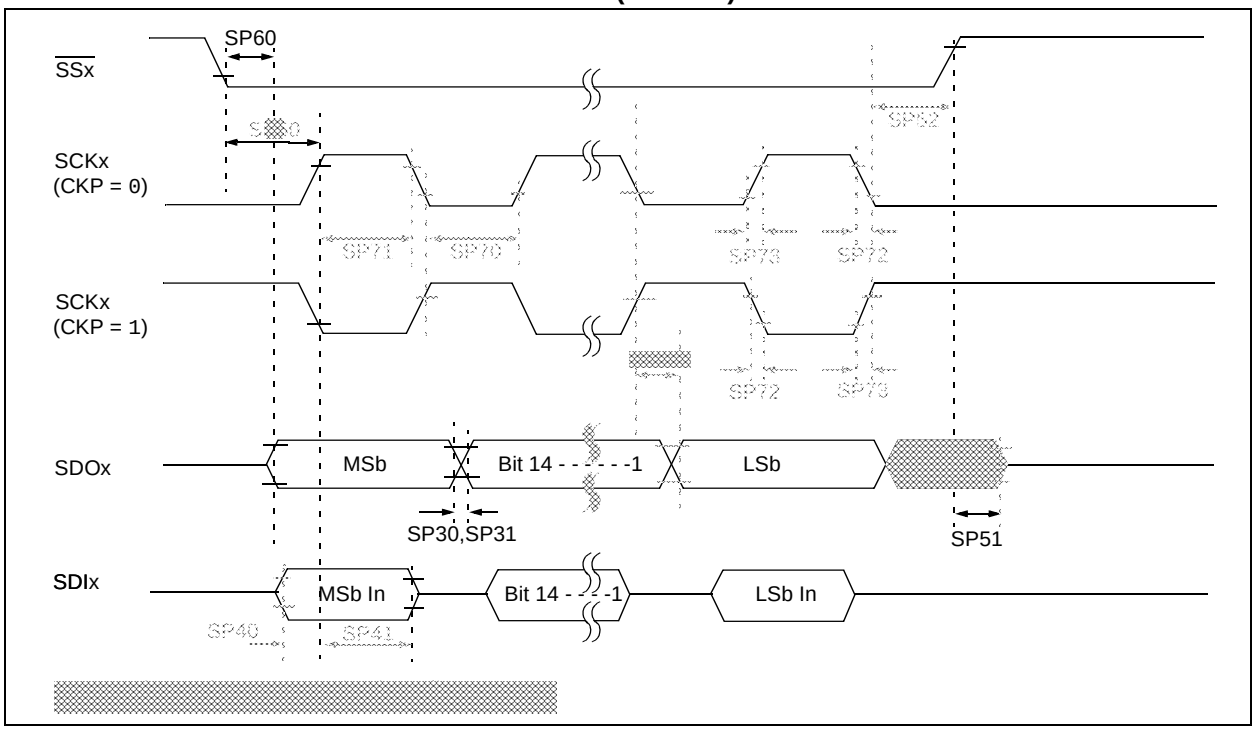


TABLE 37-33: SPIx MODULE SLAVE MODE (CKE = 1) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typical(2)**	**Max.**	**Units**	**Conditions**
SP70	TscL	SCKx Input Low Time **(Note 3)**	Tsck/2	—	—	ns	—
SP71	TscH	SCKx Input High Time **(Note 3)**	Tsck/2	—	—	ns	—
SP72	TscF	SCKx Input Fall Time	—	—	10	ns	—
SP73	TscR	SCKx Input Rise Time	—	—	10	ns	—
SP30	TdoF	SDOx Data Output Fall Time **(Note 4)**	—	—	—	ns	See parameter DO32
SP31	TdoR	SDOx Data Output Rise Time **(Note 4)**	—	—	—	ns	See parameter DO31
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	—	10	ns	VDD > 2.7V
			—	—	15	ns	VDD < 2.7V
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	0	—	—	ns	—
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	7	—	—	ns	—

Note 1: These parameters are characterized, but not tested in manufacturing.

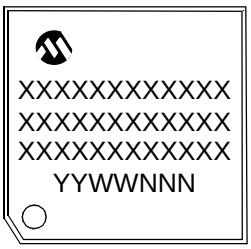
2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: The minimum clock period for SCKx is 20 ns.

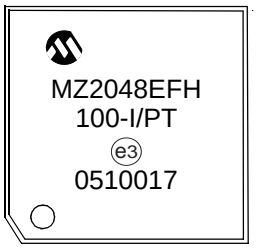
4: Assumes 30 pF load on all SPIx pins.

41.1 Package Marking Information (Continued)

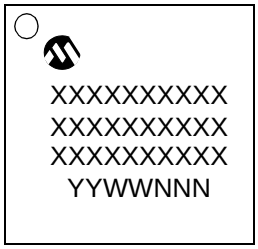
100-Lead TQFP (12x12x1 mm)



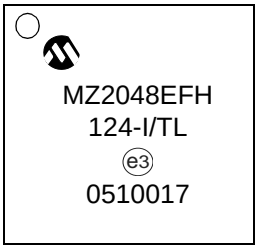
Example



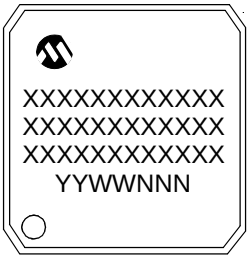
124-Lead VTLA (9x9x0.9 mm)



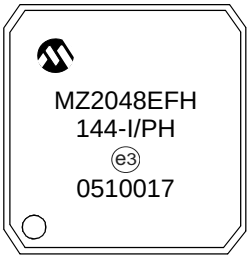
Example



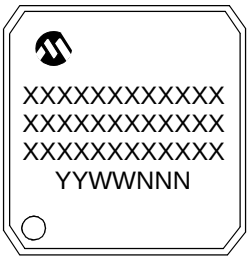
144-Lead TQFP (16x16x1 mm)



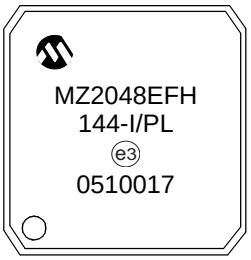
Example



144-Lead LQFP (20x20x1.40 mm)



Example



Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
		Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.	

TABLE A-3: ADC DIFFERENCES (CONTINUED)

PIC32MX5XX/6XX/7XX Feature	PIC32MZ EF Feature
Scan Trigger Source	
On PIC32MX devices, there are four sources that can trigger a scan conversion in the ADC module: Auto, Timer3, INT0, and clearing the SAMP bit. SSRC<2:0> (AD1CON1<7:5>) 111 = Auto convert 110 = Reserved 101 = Reserved 100 = Reserved 011 = Reserved 010 = Timer3 period match 001 = Active transition on INT0 pin 000 = Clearing SAMP bit	On PIC32MZ EF devices, the list of sources for triggering a scan conversion has been expanded to include the comparators, Output Compare, and two additional Timers. In addition, trigger sources can be simulated by setting the RQCNVRT (ADCCON3<8>) bit. STRGSRC<4:0> (ADCCON1<20:16>) 11111 = Reserved • • • 01101 = Reserved 01100 = Comparator 2 COUT 01011 = Comparator 1 COUT 01010 = OCMP5 01001 = OCMP3 01000 = OCMP1 00111 = TMR5 match 00110 = TMR3 match 00101 = TMR1 match 00100 = INT0 00011 = Reserved 00010 = Global level software trigger (GLSWTRG) 00001 = Global software trigger (GSWTRG) 00000 = No trigger
Output Format	
On PIC32MX devices, the output format was decided for all ADC channels based on the setting of the FORM<2:0> bits. FORM<2:0> (AD1CON1<10:8>) 011 = Signed Fractional 16-bit 010 = Fractional 16-bit 001 = Signed Integer 16-bit 000 = Integer 16-bit 111 = Signed Fractional 32-bit 110 = Fractional 32-bit 101 = Signed Integer 32-bit 100 = Integer 32-bit	On PIC32MZ EF devices, the FRACT bit determines whether fractional or integer format is used. Then, each input can have its own setting for input (differential or single-ended) and sign (signed or unsigned) using the DIFFx and SIGNx bits in the ADCIMODx registers. FRACT (ADCCON1<23>) 1 = Fractional 0 = Integer DIFFx (ADCIMODy) 1 = Channel x is using Differential mode 0 = Channel x is using Single-ended mode SIGNx (ADCMODy) 1 = Channel x is using Signed Data mode 0 = Channel x is using Unsigned Data mode
Interrupts	
On PIC32MX devices, an interrupt is triggered from the ADC module when a certain number of conversions have taken place, irrespective of which channel was converted. SMPI<3:0> (AD1CON2<5:2>) 1111 = Interrupt for each 16th sample/convert sequence 1110 = Interrupt for each 15th sample/convert sequence • • • 0001 = Interrupt for each 2nd sample/convert sequence 0000 = Interrupt for each sample/convert sequence	On PIC32MZ EF devices, the ADC module can trigger an interrupt for each channel when it is converted. Use the Interrupt Controller bits, IEC1<31:27>, IEC2<31:0>, and IEC3<7:0>, to enable/disable them. In addition, the ADC support one global interrupt to indicate conversion on any number of channels. AGIENxx (ADCGIRQENx<y>) 1 = Data ready event will generate a Global ADC interrupt 0 = No global interrupt In addition, interrupts can be generated for filter and comparator events.

B.6 Resets

On PIC32MZ EF devices, the Reset module adds eight bits to the NMICNT field to make the time-out period before device Reset longer, as described in Table B-5.

TABLE B-5: RESETS DIFFERENCES

PIC32MZ EC Feature	PIC32MZ EF Feature
Countdown to Reset During NMIs	
On PIC32MZ EC devices, the NMICNT<7:0> field is eight bits long, giving a maximum of 256 instructions before the device Reset.	On PIC32MZ EF devices, the NMICNT<15:0> field is now 16 bits long, giving a longer period of time (up to 65,536 instructions) prior to a device Reset.

B.7 USB

On PIC32MZ EF devices, a new USBCRCON register has been added to assist in controlling the reset of the USB module, and triggering interrupts based on VBUS voltage levels. This register also overcomes an errata on PIC32MZ EC devices that requires a three second start-up on the USB module.

B.8 I/O Ports

On PIC32MZ EF devices, many of the I/O pins now feature slew rate control bits to control how fast the pin makes a low-to-high or high-to-low transition. The Change Notification feature has also been enhanced to allow detection of level events in addition to edge detection. However, the SIDL bit is not present in the CNCONx registers on PIC32MZ EF devices, as it is on PIC32MZ EC devices.

B.9 Watchdog Timer

PIC32MZ EF devices use a new Watchdog Timer, although the overall control through the DEVCFGx words remains identical to that of PIC32MZ EC devices. Table B-6 lists two more changes, as well.

TABLE B-6: WATCHDOG TIMER DIFFERENCES

PIC32MZ EC Feature	PIC32MZ EF Feature
Watchdog Timer Postscaler	
On PIC32MZ EC devices, the SWDTPS<4:0> bits (WDTCON<6:2>) reflect the postscaler setting for the Watchdog Timer.	On PIC32MZ EF devices, the field has been changed to the RUNDIV<4:0> bits (WDTCON<12:8>).
Watchdog Windowed Mode	
On PIC32MZ EC devices, WDTWINEN is at bit position 1 (WDTCON<1>).	On PIC32MZ EF devices, WDTWINEN is now at bit position 0 (WDTCON<0>).