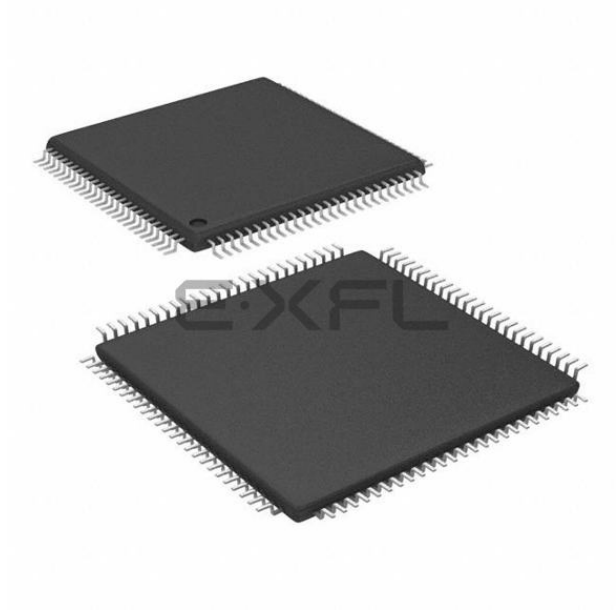
Microchip Technology - PIC32MZ2048EFM100-I/PF Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® M-Class
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, PMP, SPI, SQI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	78
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	2.1V ~ 3.6V
Data Converters	A/D 40x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mz2048efm100-i-pf

TABLE 3: PIN NAMES FOR 100-PIN DEVICES

100-PIN TQFP (TOP VIEW)

PIC32MZ0512EF(E/F/K)100
PIC32MZ1024EF(G/H/M)100
PIC32MZ1024EF(E/F/K)100
PIC32MZ2048EF(G/H/M)100

100

1

Pin #	Full Pin Name	Pin #	Full Pin Name
1	AN23/AERXERR/RG15	36	VSS
2	EBIA5/AN34/PMA5/RA5	37	VDD
3	EBID5/AN17/RPE5/PMD5/RE5	38	TCK/EBIA19/AN29/RA1
4	EBID6/AN16/PMD6/RE6	39	TDI/EBIA18/AN30/RPF13/SCK5/RF13
5	EBID7/AN15/PMD7/RE7	40	TDO/EBIA17/AN31/RPF12/RF12
6	EBIA6/AN22/RPC1/PMA6/RC1	41	EBIA11/AN7/ERXD0/AECRS/PMA11/RB12
7	EBIA12/AN21/RPC2/PMA12/RC2	42	AN8/ERXD1/AECOL/RB13
8	$\overline{\text{EBIWE}}$/AN20/RPC3/PMWR/RC3	43	EBIA1/AN9/ERXD2/AETXD3/RPB14/SCK3/PMA1/RB14
9	$\overline{\text{EBIOE}}$/AN19/RPC4/PMRD/RC4	44	EBIA0/AN10/ERXD3/AETXD2/RPB15/OCFB/PMA0/RB15
10	AN14/C1IND/ECOL/RPG6/SCK2/RG6	45	VSS
11	EBIA4/AN13/C1INC/ECRS/RPG7/SDA4/PMA4/RG7	46	VDD
12	EBIA3/AN12/C2IND/ERXDV/ECRSDV/AERXDV/ AECRSDV/RPG8/SCL4/PMA3/RG8	47	AN32/AETXD0/RPD14/RD14
13	VSS	48	AN33/AETXD1/RPD15/SCK6/RD15
14	VDD	49	OSC1/CLKI/RC12
15	$\overline{\text{MCLR}}$	50	OSC2/CLKO/RC15
16	EBIA2/AN11/C2INC/ERXCLK/EREFCLK/AERXCLK/ AEREFCLK/RPG9/PMA2/RG9	51	VBUS
17	TMS/EBIA16/AN24/RA0	52	VUSB3V3
18	AN25/AERXD0/RPE8/RE8	53	VSS
19	AN26/AERXD1/RPE9/RE9	54	D-
20	AN45/C1INA/RPB5/RB5	55	D+
21	AN4/C1INB/RB4	56	RPF3/USBID/RF3
22	AN3/C2INA/RPB3/RB3	57	EBIRDY3/RPF2/SDA3/RF2
23	AN2/C2INB/RPB2/RB2	58	EBIRDY2/RPF8/SCL3/RF8
24	PGEC1/AN1/RPB1/RB1	59	$\overline{\text{EBICS0}}$/SCL2/RA2
25	PGED1/AN0/RPB0/RB0	60	EBIRDY1/SDA2/RA3
26	PGEC2/AN46/RPB6/RB6	61	EBIA14/PMCS1/PMA14/RA4
27	PGED2/AN47/RPB7/RB7	62	VDD
28	VREF-/CVREF-/AN27/AERXD2/RA9	63	VSS
29	VREF+/CVREF+/AN28/AERXD3/RA10	64	EBIA9/RPF4/SDA5/PMA9/RF4
30	AVDD	65	EBIA8/RPF5/SCL5/PMA8/RF5
31	AVSS	66	AETXCLK/RPA14/SCL1/RA14
32	EBIA10/AN48/RPB8/PMA10/RB8	67	AETXEN/RPA15/SDA1/RA15
33	EBIA7/AN49/RPB9/PMA7/RB9	68	EBIA15/RPD9/PMCS2/PMA15/RD9
34	EBIA13/CVREFOUT/AN5/RPB10/PMA13/RB10	69	RPD10/SCK4/RD10
35	AN6/ERXERR/AETXERR/RB11	70	EMDC/AEMDC/RPD11/RD11

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and **Section 12.4 "Peripheral Pin Select (PPS)"** for restrictions.

2: Every I/O port pin (RAx-RGx) can be used as a change notification pin (CNAx-CNGx). See **Section 12.0 "I/O Ports"** for more information.

3: Shaded pins are 5V tolerant.

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TABLE 1-6: PORTA THROUGH PORTK PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number				Pin Type	Buffer Type	Description
	64-pin QFN/ TQFP	100-pin TQFP	124-pin VTLA	144-pin TQFP/ LQFP			
PORTD							
RD0	46	71	A48	104	I/O	ST	PORTD is a bidirectional I/O port
RD1	49	76	A52	109	I/O	ST	
RD2	50	77	B42	110	I/O	ST	
RD3	51	78	A53	111	I/O	ST	
RD4	52	81	A56	118	I/O	ST	
RD5	53	82	B46	119	I/O	ST	
RD6	—	—	A57	120	I/O	ST	
RD7	—	—	B47	121	I/O	ST	
RD9	43	68	B38	97	I/O	ST	
RD10	44	69	A46	98	I/O	ST	
RD11	45	70	B39	99	I/O	ST	
RD12	—	79	B43	112	I/O	ST	
RD13	—	80	A54	113	I/O	ST	
RD14	—	47	B27	69	I/O	ST	
RD15	—	48	A32	70	I/O	ST	
PORTE							
RE0	58	91	B52	135	I/O	ST	PORTE is a bidirectional I/O port
RE1	61	94	A64	138	I/O	ST	
RE2	62	98	A66	142	I/O	ST	
RE3	63	99	B56	143	I/O	ST	
RE4	64	100	A67	144	I/O	ST	
RE5	1	3	A3	3	I/O	ST	
RE6	2	4	B2	4	I/O	ST	
RE7	3	5	A4	5	I/O	ST	
RE8	—	18	B10	23	I/O	ST	
RE9	—	19	A12	24	I/O	ST	
PORTF							
RF0	56	85	A59	124	I/O	ST	PORTF is a bidirectional I/O port
RF1	57	86	B49	125	I/O	ST	
RF2	—	57	B31	79	I/O	ST	
RF3	38	56	A38	78	I/O	ST	
RF4	41	64	B36	90	I/O	ST	
RF5	42	65	A44	91	I/O	ST	
RF8	—	58	A39	80	I/O	ST	
RF12	—	40	B22	58	I/O	ST	
RF13	—	39	A26	57	I/O	ST	

Legend: CMOS = CMOS-compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = Transistor-transistor Logic input buffer; PPS = Peripheral Pin Select

4.0 MEMORY ORGANIZATION

Note: This data sheet summarizes the features of the PIC32MZ EF family of devices. It is not intended to be a comprehensive reference source.For detailed information, refer to **Section 48. "Memory Organization and Permissions"** in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

PIC32MZ EF microcontrollers provide 4 GB of unified virtual memory address space. All memory regions, including program, data memory, SFRs and Configuration registers, reside in this address space at their respective unique addresses. The program and data memories can be optionally partitioned into user and kernel memories. In addition, PIC32MZ EF devices allow execution from data memory.

Key features include:

- 32-bit native data width
- Separate User (KUSEG) and Kernel (KSEG0/ KSEG1/KSEG2/KSEG3) mode address space
- Separate boot Flash memory for protected code
- Robust bus exception handling to intercept runaway code
- Cacheable (KSEG0/KSEG2) and non-cacheable (KSEG1/KSEG3) address regions
- Read/write permission access to predefined memory regions

4.1 Memory Layout

PIC32MZ EF microcontrollers implement two address schemes: virtual and physical. All hardware resources, such as program memory, data memory and peripherals, are located at their respective physical addresses. Virtual addresses are exclusively used by the CPU to fetch and execute instructions as well as access peripherals. Physical addresses are used by bus master peripherals, such as DMA and the Flash controller, that access memory independently of the CPU.

The main memory maps for the PIC32MZ EF devices are illustrated in Figure 4-1 through Figure 4-4. Figure 4-5 provides memory map information for boot Flash and boot alias. Table 4-1 provides memory map information for Special Function Registers (SFRs).

TABLE 4-17: SYSTEM BUS TARGET 9 REGISTER MAP

Virtual Address (BF8F_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
A420	SBT9ELOG1	31:16	MULTI	—	—	—	CODE<3:0>				—	—	—	—	—	—	—	—	0000
		15:0	INITID<7:0>								REGION<3:0>				—	CMD<2:0>			0000
A424	SBT9ELOG2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	GROUP<1:0>		0000
A428	SBT9ECON	31:16	—	—	—	—	—	—	—	ERRP	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
A430	SBT9ECLRS	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
A438	SBT9ECLRM	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLEAR	0000
A440	SBT9REG0	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
A450	SBT9RD0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
A458	SBT9WR0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
A460	SBT9REG1	31:16	BASE<21:6>																xxxx
		15:0	BASE<5:0>						PRI	—	SIZE<4:0>					—	—	—	xxxx
A470	SBT9RD1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx
A478	SBT9WR1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	GROUP3	GROUP2	GROUP1	GROUP0	xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.
Note: For reset values listed as 'xxxx', please refer to Table 4-6 for the actual reset values.

REGISTER 5-3: NVMKEY: PROGRAMMING UNLOCK REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
	NVMKEY<31:24>							
23:16	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
	NVMKEY<23:16>							
15:8	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
	NVMKEY<15:8>							
7:0	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
	NVMKEY<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **NVMKEY<31:0>:** Unlock Register bits
These bits are write-only, and read as '0' on any read

Note: This register is used as part of the unlock sequence to prevent inadvertent writes to the PFM.

REGISTER 5-4: NVMADDR: FLASH ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMADDR<31:24>(1)							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMADDR<23:16>(1)							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMADDR<15:8>(1)							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMADDR<7:0>(1)							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **NVMADDR<31:0>:** Flash Address bits(1)

NVMOP<3:0> Selection	Flash Address Bits (NVMADDR<31:0>)
Page Erase	Address identifies the page to erase (NVMADDR<13:0> are ignored).
Row Program	Address identifies the row to program (NVMADDR<10:0> are ignored).
Word Program	Address identifies the word to program (NVMADDR<1:0> are ignored).
Quad Word Program	Address identifies the quad word (128-bit) to program (NVMADDR<3:0> bits are ignored).

Note 1: For all other NVMOP<3:0> bit settings, the Flash address is ignored. See the NVMCON register (Register 5-1) for additional information on these bits.

Note: The bits in this register are only reset by a Power-on Reset (POR) and are not affected by other reset sources.

FIGURE 11-1: PIC32MZ EF FAMILY USB INTERFACE DIAGRAM

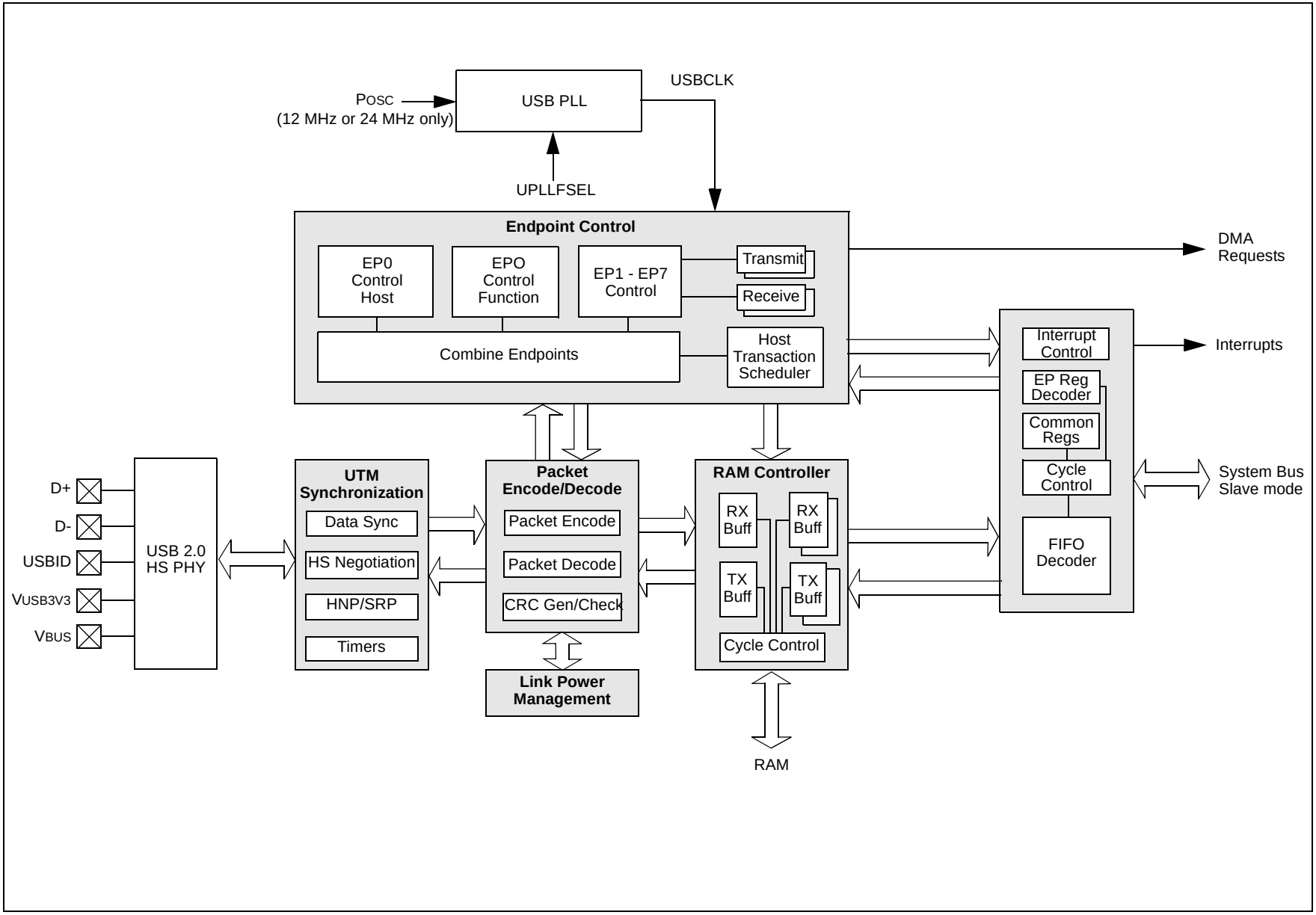


TABLE 11-1: USB REGISTER MAP 1 (CONTINUED)

Virtual Address (BF8E_#)	Register Name	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
3340	USB DPBFD	31:16	—	—	—	—	—	—	—	—	EP7TXD	EP6TXD	EP5TXD	EP4TXD	EP3TXD	EP2TXD	EP1TXD	—	0000
		15:0	—	—	—	—	—	—	—	—	EP7RXD	EP6RXD	EP5RXD	EP4RXD	EP3RXD	EP2RXD	EP1RXD	—	0000
3344	USB TMCON1	31:16	THHSRTN<15:0>																05E6
		15:0	TUCH<15:0>																4074
3348	USB TMCON2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	THSBT<3:0>				0000
3360	USB LPMR1	31:16	—	—	LPM ERRIE	LPM RESIE	LPMACKIE	LPMNYIE	LPMSTIE	LPMTOIE	—	—	—	LPMNAK(1)	LPMEN<1:0>		LPMRES	LPMXMT	0000
														__(2)	__(2)	__(2)			0000
		15:0	ENDPOINT<3:0>				—	—	—	RMTWAK	HIRD<3:0>				LNKSTATE<3:0>				0000
3364	USB LPMR2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	LPMFADDR<6:0>							—	—	LPMERR(1)	LPMRES	LPMNC	LPMACK	LPMNY	LPMST	0000
													__(2)						0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: Device mode.
2: Host mode.
3: Definition for Endpoint 0 (ENDPOINT<3:0> (USBCSR<19:16>) = 0).
4: Definition for Endpoints 1-7 (ENDPOINT<3:0> (USBCSR<19:16>) = 1 through 7).

TABLE 11-2: USB REGISTER MAP 2

Virtual Address (BF88_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
4000	USB CRCON	31:16	—	—	—	—	—	USBIF	USBRF	USBWKUP	—	—	—	—	—	—	—	—	0100
		15:0	—	—	—	—	—	—	USB IDOVEN	USB IDVAL	PHYIDEN	VBUS MONEN	ASVAL MONEN	BSVAL MONEN	SEND MONEN	USBIE	USBRIE	USB WKUPEN	8000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

REGISTER 11-9: USBIENCSR1: USB INDEXED ENDPOINT CONTROL STATUS REGISTER 1 (ENDPOINT 1-7) (CONTINUED)

bit 18 **OVERRUN:** Data Overrun Status bit (*Device mode*)

1 = An OUT packet cannot be loaded into the RX FIFO.
0 = Written by software to clear this bit

This bit is only valid when the endpoint is operating in ISO mode. In Bulk mode, it always returns zero.

ERROR: No Data Packet Received Status bit (*Host mode*)

1 = Three attempts have been made to receive a packet and no data packet has been received. An interrupt is generated.

0 = Written by the software to clear this bit.

This bit is only valid when the RX endpoint is operating in Bulk or Interrupt mode. In ISO mode, it always returns zero.

bit 17 **FIFOFULL:** FIFO Full Status bit

1 = No more packets can be loaded into the RX FIFO
0 = The RX FIFO has at least one free space

bit 16 **RXPKTRDY:** Data Packet Reception Status bit

1 = A data packet has been received. An interrupt is generated.
0 = Written by software to clear this bit when the packet has been unloaded from the RX FIFO.

bit 15-11 **MULT<4:0>:** Multiplier Control bits

For Isochronous/Interrupt endpoints or of packet splitting on Bulk endpoints, multiplies TXMAXP by MULT+1 for the payload size.

For Bulk endpoints, MULT can be up to 32 and defines the number of “USB” packets of the specified payload into which a single data packet placed in the FIFO should be split, prior to transfer. The data packet is required to be an exact multiple of the payload specified by TXMAXP.

For Isochronous/Interrupts endpoints operating in Hi-Speed mode, MULT may be either 2 or 3 and specifies the maximum number of such transactions that can take place in a single microframe.

bit 10-0 **RXMAXP<10:0>:** Maximum RX Payload Per Transaction Control bits

This field sets the maximum payload (in bytes) transmitted in a single transaction. The value is subject to the constraints placed by the USB Specification on packet sizes for Bulk, Interrupt and Isochronous transfers in Full-Speed and Hi-Speed operations.

RXMAXP must be set to an even number of bytes for proper interrupt generation in DMA Mode 1.

REGISTER 11-13: USBOTG: USB OTG CONTROL/STATUS REGISTER (CONTINUED)

bit 19-16 **TXFIFOSZ<3:0>:** TX Endpoint FIFO packet size bits

The maximum packet size to allowed for (before any splitting within the FIFO of Bulk/High-Bandwidth packets prior to transmission)

1111 = Reserved
•
•
•
1010 = Reserved
1001 = 4096 bytes
1000 = 2048 bytes
0111 = 1024 bytes
0110 = 512 bytes
0101 = 256 bytes
0100 = 128 bytes
0011 = 64 bytes
0010 = 32 bytes
0001 = 16 bytes
0000 = 8 bytes

bit 15-10 **Unimplemented:** Read as '0'

bit 9 **TXEDMA:** TX Endpoint DMA Assertion Control bit
1 = DMA_REQ signal for all IN endpoints will be deasserted when MAXP-8 bytes have been written to an endpoint. This is Early mode.
0 = DMA_REQ signal for all IN endpoints will be deasserted when MAXP bytes have been written to an endpoint. This is Late mode.

bit 8 **RXEDMA:** RX Endpoint DMA Assertion Control bit
1 = DMA_REQ signal for all OUT endpoints will be deasserted when MAXP-8 bytes have been written to an endpoint. This is Early mode.
0 = DMA_REQ signal for all OUT endpoints will be deasserted when MAXP bytes have been written to an endpoint. This is Late mode.

bit 7 **BDEV:** USB Device Type bit
1 = USB is operating as a 'B' device
0 = USB is operating as an 'A' device

bit 6 **FSDEV:** Full-Speed/Hi-Speed device detection bit (*Host mode*)
1 = A Full-Speed or Hi-Speed device has been detected being connected to the port
0 = No Full-Speed or Hi-Speed device detected

bit 5 **LSDEV:** Low-Speed Device Detection bit (*Host mode*)
1 = A Low-Speed device has been detected being connected to the port
0 = No Low-Speed device detected

bit 4-3 **VBUS<1:0>:** VBUS Level Detection bits
11 = Above VBUS Valid
10 = Above AValid, below VBUS Valid
01 = Above Session End, below AValid
00 = Below Session End

bit 2 **HOSTMODE:** Host Mode bit
1 = USB module is acting as a Host
0 = USB module is not acting as a Host

bit 1 **HOSTREQ:** Host Request Control bit
'B' device only:
1 = USB module initiates the Host Negotiation when Suspend mode is entered. This bit is cleared when Host Negotiation is completed.
0 = Host Negotiation is not taking place

REGISTER 11-15: USBHWVER: USB HARDWARE VERSION REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R-0	R-0	R-0	R-0	R-1	R-0	R-0	R-0
	RC	VERMAJOR<4:0>					VERMINOR<9:8>	
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	VERMINOR<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **RC:** Release Candidate bit
1 = USB module was created using a release candidate
0 = USB module was created using a full release

bit 14-10 **VERMAJOR<4:0>:** USB Module Major Version number bits
This read-only number is the Major version number for the USB module.

bit 9-0 **VERMINOR<9:0>:** USB Module Minor Version number bits
This read-only number is the Minor version number for the USB module.

21.0 INTER-INTEGRATED CIRCUIT (I^2C)

Note: This data sheet summarizes the features of the PIC32MZ EF family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 24. "Inter-Integrated Circuit (I^2C)"** (DS60001116) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

The I^2C module provides complete hardware support for both Slave and Multi-Master modes of the I^2C serial communication standard.

Each I^2C module has a 2-pin interface:

- SCLx pin is clock
- SDAx pin is data

Each I^2C module offers the following key features:

- I^2C interface supporting both master and slave operation
- I^2C Slave mode supports 7-bit and 10-bit addressing
- I^2C Master mode supports 7-bit and 10-bit addressing
- I^2C port allows bidirectional transfers between master and slaves
- Serial clock synchronization for the I^2C port can be used as a handshake mechanism to suspend and resume serial transfer (SCLREL control)
- I^2C supports multi-master operation; detects bus collision and arbitrates accordingly
- Provides support for address bit masking
- SMBus support

Figure 21-1 illustrates the I^2C module block diagram.

25.0 REAL-TIME CLOCK AND CALENDAR (RTCC)

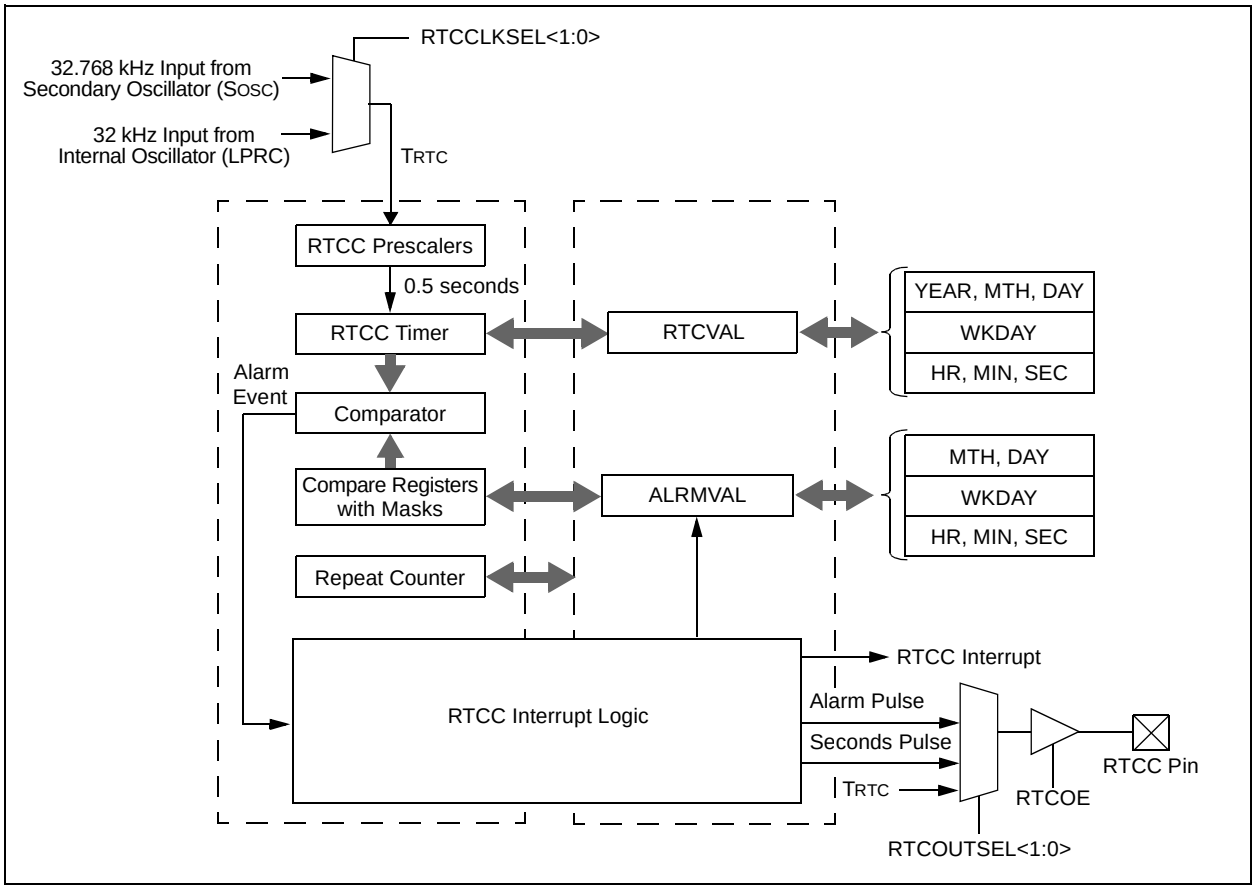
Note: This data sheet summarizes the features of the PIC32MZ EF family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 29. "Real-Time Clock and Calendar (RTCC)"** (DS60001125) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

The RTCC module is intended for applications in which accurate time must be maintained for extended periods of time with minimal or no CPU intervention. Low-power optimization provides extended battery lifetime while keeping track of time.

The following are key features of the RTCC module:

- Time: hours, minutes, and seconds
- 24-hour format (military time)
- Visibility of one-half second period
- Provides calendar: Weekday, date, month and year
- Alarm intervals are configurable for half of a second, one second, 10 seconds, one minute, 10 minutes, one hour, one day, one week, one month, and one year
- Alarm repeat with decrementing counter
- Alarm with indefinite repeat: Chime
- Year range: 2000 to 2099
- Leap year correction
- BCD format for smaller firmware overhead
- Optimized for long-term battery operation
- Fractional second synchronization
- User calibration of the clock crystal frequency with auto-adjust
- Calibration range: ±0.66 seconds error per month
- Calibrates up to 260 ppm of crystal error
- Uses external 32.768 kHz crystal or 32 kHz internal oscillator
- Alarm pulse, seconds clock, or internal clock output on RTCC pin

FIGURE 25-1: RTCC BLOCK DIAGRAM



REGISTER 25-1: RTCCON: REAL-TIME CLOCK AND CALENDAR CONTROL REGISTER (CONTINUED)

bit 10-9 **RTCCLKSEL<1:0>:** RTCC Clock Select bits

When a new value is written to these bits, the Seconds Value register should also be written to properly reset the clock prescalers in the RTCC.

11 = Reserved
10 = Reserved
01 = RTCC uses the external 32.768 kHz Secondary Oscillator (SOSC)
00 = RTCC uses the internal 32 kHz oscillator (LPRC)

bit 8-7 **RTCOUTSEL<1:0>:** RTCC Output Data Select bits(2)

11 = Reserved
10 = RTCC Clock is presented on the RTCC pin
01 = Seconds Clock is presented on the RTCC pin
00 = Alarm Pulse is presented on the RTCC pin when the alarm interrupt is triggered

bit 6 **RTCCLKON:** RTCC Clock Enable Status bit(5)

1 = RTCC Clock is actively running
0 = RTCC Clock is not running

bit 5-4 **Unimplemented:** Read as '0'

bit 3 **RTCWREN:** Real-Time Clock Value Registers Write Enable bit(3)

1 = Real-Time Clock Value registers can be written to by the user
0 = Real-Time Clock Value registers are locked out from being written to by the user

bit 2 **RTCSYNC:** Real-Time Clock Value Registers Read Synchronization bit

1 = Real-time clock value registers can change while reading (due to a rollover ripple that results in an invalid data read). If the register is read twice and results in the same data, the data can be assumed to be valid.
0 = Real-time clock value registers can be read without concern about a rollover ripple

bit 1 **HALFSEC:** Half-Second Status bit(4)

1 = Second half period of a second
0 = First half period of a second

bit 0 **RTCOE:** RTCC Output Enable bit

1 = RTCC output is enabled
0 = RTCC output is not enabled

Note 1: The ON bit is only writable when RTCWREN = 1.
2: Requires RTCOE = 1 (RTCCON<0>) for the output to be active.
3: The RTCWREN bit can be set only when the write sequence is enabled.
4: This bit is read-only. It is cleared to '0' on a write to the seconds bit fields (RTCTIME<14:8>).
5: This bit is undefined when RTCCLKSEL<1:0> = 00 (LPRC is the clock source).

Note:	This register is reset only on a Power-on Reset (POR).

REGISTER 28-1: ADCCON1: ADC CONTROL REGISTER 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R-0, HS, HC	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	TRBEN	TRBERR	TRBMST<2:0>			TRBSLV<2:0>		
23:16	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FRACT	SELRES<1:0>		STRGSRC<4:0>				
15:8	R/W-0	U-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-0	U-0
	ON		SIDL	AICPMPEN	CVDEN	FSSCLKEN	FSPBCLKEN	—
7:0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0
	—	IRQVS<2:0>			STRGLVL	—	—	—

Legend:	HC = Hardware Set	HS = Hardware Cleared	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **TRBEN:** Turbo Channel Enable bit
1 = Enable the Turbo channel
0 = Disable the Turbo channel

bit 30 **TRBERR:** Turbo Channel Error Status bit
1 = An error occurred while setting the Turbo channel and Turbo channel function to be disabled regardless of the TRBEN bit being set to '1'.
0 = Turbo channel error did not occur

Note: The status of this bit is valid only after the TRBEN bit is set.

bit 29-27 **TRBMST<2:0>:** Turbo Master ADCx bits
111 = Reserved
110 = ADC4 is selected as the Turbo Master
•
•
•
000 = ADC0 is selected as the Turbo Master

bit 26-24 **TRBSLV<2:0>:** Turbo Slave ADCx bits
111 = Reserved
110 = ADC4 is selected as the Turbo Slave
•
•
•
000 = ADC0 is selected as the Turbo Slave

bit 23 **FRACT:** Fractional Data Output Format bit
1 = Fractional
0 = Integer

bit 22-21 **SELRES<1:0>:** Shared ADC (ADC7) Resolution bits
11 = 12 bits (default)
10 = 10 bits
01 = 8 bits
00 = 6 bits

Note: Changing the resolution of the ADC does not shift the result in the corresponding ADCDATAx register. The result will still occupy 12 bits, with the corresponding lower unused bits set to '0'. For example, a resolution of 6 bits will result in ADCDATAx<5:0> being set to '0', and ADCDATAx<11:6> holding the result.

REGISTER 28-10: ADCCSS1: ADC COMMON SCAN SELECT REGISTER 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CSS31(1)	CSS30(1)	CSS29(1)	CSS28(1)	CSS27(1)	CSS26(1)	CSS25(1)	CSS24(1)
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CSS23(1)	CSS22(1)	CSS21(1)	CSS20(1)	CSS19(1)	CSS18	CSS17	CSS16
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CSS15	CSS14	CSS13	CSS12	CSS11	CSS10	CSS9	CSS8
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CSS7	CSS6	CSS5	CSS4	CSS3	CSS2	CSS1	CSS0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **CSS31:CSS0:** Analog Common Scan Select bits(2,3)
1 = Select AN*x* for input scan
0 = Skip AN*x* for input scan

Note 1: This bit is not available on 64-pin devices.

2: In addition to setting the appropriate bits in this register, Class 1 and Class 2 analog inputs must select the STRIG input as the trigger source if they are to be scanned through the CSS*x* bits. Refer to the bit descriptions in the ADCTRGx registers for selecting the STRIG option.

3: If a Class 1 or Class 2 input is included in the scan by setting the CSSx bit to '1' and by setting the TRGSRCx<4:0> bits to STRIG mode (`'0b11`), the user application must ensure that no other triggers are generated for that input using the RQCNVRT bit in the ADCCON3 register or the hardware input or any digital filter. Otherwise, the scan behavior is unpredictable.

REGISTER 30-29: EMAC1SUPP: ETHERNET CONTROLLER MAC PHY SUPPORT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	R/W-0	U-0	U-0	R/W-0
	—	—	—	—	RESETRMII(1)	—	—	SPEEDRMII(1)
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-12 **Unimplemented:** Read as '0'

bit 11 **RESETRMII:** Reset RMII Logic bit(1)
1 = Reset the MAC RMII module
0 = Normal operation.

bit 10-9 **Unimplemented:** Read as '0'

bit 8 **SPEEDRMII:** RMII Speed bit(1)
This bit configures the Reduced MII logic for the current operating speed.
1 = RMII is running at 100 Mbps
0 = RMII is running at 10 Mbps

bit 7-0 **Unimplemented:** Read as '0'

Note 1: This bit is only used for the RMII module.

Note: Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware.

NOTES:

TABLE A-10: PERIPHERAL DIFFERENCES (CONTINUED)

PIC32MX5XX/6XX/7XX Feature	PIC32MZ EF Feature
Ethernet	
	On PIC32MZ EF devices, the input clock divider for the Ethernet module has expanded options to accommodate the faster peripheral bus clock.
CLKSEL<3:0> (EMAC1MCFG<5:2>) 1000 = SYSCLK divided by 40 0111 = SYSCLK divided by 28 0110 = SYSCLK divided by 20 0101 = SYSCLK divided by 14 0100 = SYSCLK divided by 10 0011 = SYSCLK divided by 8 0010 = SYSCLK divided by 6 000x = SYSCLK divided by 4	CLKSEL<3:0> (EMAC1MCFG<5:2>) **1010 = PBCLK5 divided by 50** **1001 = PBCLK5 divided by 48** 1000 = PBCLK5 divided by 40 0111 = PBCLK5 divided by 28 0110 = PBCLK5 divided by 20 0101 = PBCLK5 divided by 14 0100 = PBCLK5 divided by 10 0011 = PBCLK5 divided by 8 0010 = PBCLK5 divided by 6 000x = PBCLK5 divided by 4
Comparator/Comparator Voltage Reference	
On PIC32MX devices, it was possible to select the VREF+ pin as the output to the CVREFOUT pin. VREFSEL (CVRCON<10>) 1 = CVREF = VREF+ 0 = CVREF is generated by the resistor network	On PIC32MZ EF devices, the CVREFOUT pin must come from the resistor network. This bit is not available.
On PIC32MX devices, the internal voltage reference (IVREF) could be chosen by the BGSEL<1:0> bits. BGSEL<1:0> (CVRCON<9:8>) 11 = IVREF = VREF+ 10 = Reserved 01 = IVREF = 0.6V (nominal, default) 00 = IVREF = 1.2V (nominal)	On PIC32MZ EF devices, IVREF is fixed and cannot be changed. These bits are not available.
Change Notification	
On PIC32MX devices, Change Notification is controlled by the **CNCON, CNEN, and CNPUE** registers.	On PIC32MZ EF devices, Change Notification functionality has been relocated into each I/O port and is controlled by the **CNPUx, CNPDx, CNCONx, CNENx, and CNSTATx** registers.
System Bus	
On PIC32MX devices, the System Bus registers can be used to configure RAM memory for data and program memory partitions, cacheability of Flash memory, and RAM Wait states. These registers are: **BMXCON, BMXDKPBA, BMXDUDBA, BMXDUPBA, BMXPUPBA, BMXDRMSZ, BMXPFMSZ, and BMXBOOTSZ.**	On PIC32MZ EF devices, a new System Bus is utilized that supports using RAM memory for program or data without the need for special configuration. Therefore, no special registers are associated with the System Bus to configure these features.
On PIC32MX devices, various arbitration modes are used as initiators on the System Bus. These modes can be selected by the **BMXARB<2:0> (BMXCON<2:0>)** bits.	On PIC32MZ EF devices, a new arbitration scheme has been implemented on the System Bus. All initiators use the Least Recently Serviced (LRS) scheme, with the exception of the DMA, CPU, and the Flash Controller. The Flash Controller always has High priority over LRS initiators. The DMA and CPU (when servicing an interrupt) can be selected to have LRS or High priority using the **DMAPRI (CFGCON<25>)** and **CPUPRI (CFGCON<24>)** bits.

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