Microchip Technology - PIC32MZ2048EFM124-E/TL Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	MIPS32® M-Class
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, PMP, SPI, SQI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	97
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	2.1V ~ 3.6V
Data Converters	A/D 48x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C
Mounting Type	Surface Mount
Package / Case	124-VFTLA Dual Rows, Exposed Pad
Supplier Device Package	124-VTLA (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mz2048efm124-e-tl

2.10 Typical Application Connection Examples

Examples of typical application connections are shown in Figure 2-6 and Figure 2-7.

FIGURE 2-6: AUDIO PLAYBACK APPLICATION

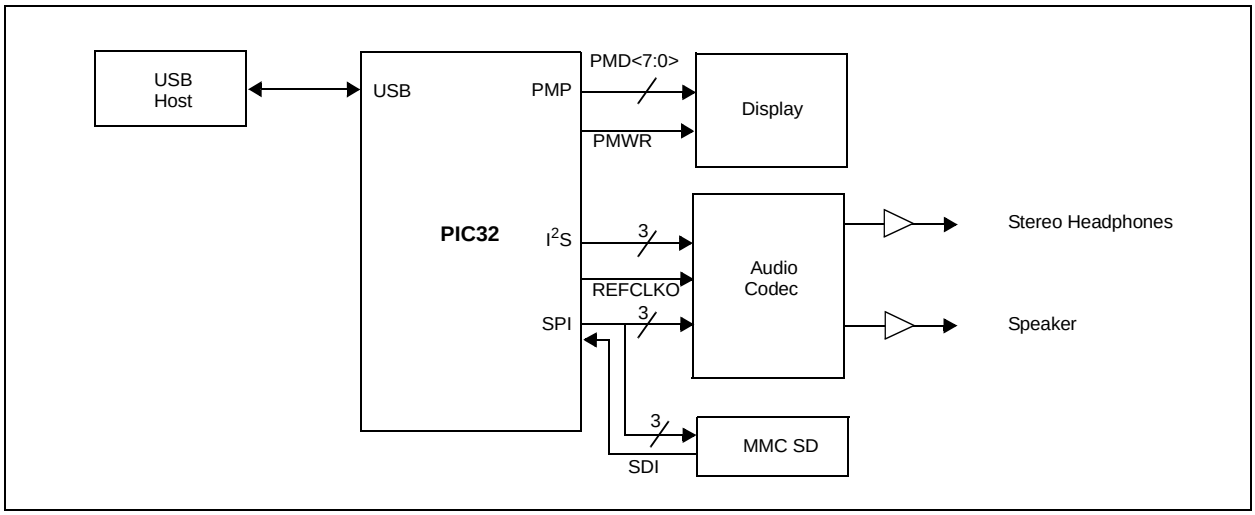
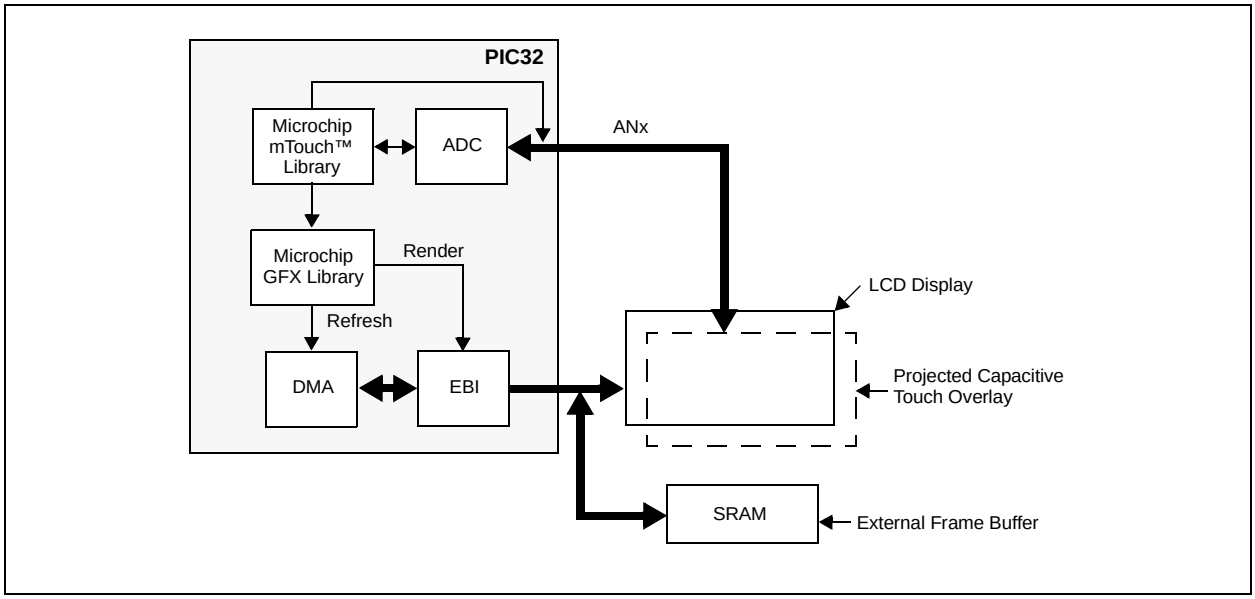


FIGURE 2-7: LOW-COST CONTROLLERLESS (LCC) GRAPHICS APPLICATION WITH PROJECTED CAPACITIVE TOUCH



REGISTER 6-2: RSWRST: SOFTWARE RESET REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	W-0, HC
	—	—	—	—	—	—	—	SWRST(1,2)

Legend:	HC = Hardware Cleared		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-1 **Unimplemented:** Read as '0'

bit 0 **SWRST:** Software Reset Trigger bit(1,2)
1 = Enable software Reset event
0 = No effect

Note 1: The system unlock sequence must be performed before the SWRST bit can be written. Refer to **Section 42. "Oscillators with Enhanced PLL"** in the *"PIC32 Family Reference Manual"* for details.

2: Once this bit is set, any read of the RSWRST register will cause a reset to occur.

TABLE 7-3: INTERRUPT REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0548	OFF002	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
054C	OFF003	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0550	OFF004	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0554	OFF005	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0558	OFF006	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
055C	OFF007	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0560	OFF008	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0564	OFF009	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0568	OFF010	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
056C	OFF011	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0570	OFF012	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0574	OFF013	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0578	OFF014	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
057C	OFF015	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0580	OFF016	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 "CLR, SET, and INV Registers"** for more information.
2: This bit or register is not available on 64-pin devices.
3: This bit or register is not available on devices without a CAN module.
4: This bit or register is not available on 100-pin devices.
5: Bits 31 and 30 are not available on 64-pin and 100-pin devices; bits 29 through 14 are not available on 64-pin devices.
6: Bits 31, 30, 29, and bits 5 through 0 are not available on 64-pin and 100-pin devices; bit 31 is not available on 124-pin devices; bit 22 is not available on 64-pin devices.
7: This bit or register is not available on devices without a Crypto module.
8: This bit or register is not available on 124-pin devices.

TABLE 7-3: INTERRUPT REGISTER MAP (CONTINUED)

Virtual Address (BF81_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
07E0	OFF168	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07E4	OFF169	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07E8	OFF170	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07EC	OFF171	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07F0	OFF172	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07F4	OFF173	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07F8	OFF174	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
07FC	OFF175	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0800	OFF176(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0804	OFF177(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0808	OFF178(2)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
080C	OFF179	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0810	OFF180	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0814	OFF181	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000
0818	OFF182	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<17:16>		0000
		15:0	VOFF<15:1>															—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 "CLR, SET, and INV Registers"** for more information.
2: This bit or register is not available on 64-pin devices.
3: This bit or register is not available on devices without a CAN module.
4: This bit or register is not available on 100-pin devices.
5: Bits 31 and 30 are not available on 64-pin and 100-pin devices; bits 29 through 14 are not available on 64-pin devices.
6: Bits 31, 30, 29, and bits 5 through 0 are not available on 64-pin and 100-pin devices; bit 31 is not available on 124-pin devices; bit 22 is not available on 64-pin devices.
7: This bit or register is not available on devices without a Crypto module.
8: This bit or register is not available on 124-pin devices.

REGISTER 10-12: DCHxSSIZ: DMA CHANNEL x SOURCE SIZE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHSSIZ<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHSSIZ<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **CHSSIZ<15:0>:** Channel Source Size bits

1111111111111111 = 65,535 byte source size

•
•
•

0000000000000010 = 2 byte source size

0000000000000001 = 1 byte source size

0000000000000000 = 65,536 byte source size

REGISTER 10-13: DCHxDSIZ: DMA CHANNEL x DESTINATION SIZE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHDSIZ<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHDSIZ<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **CHDSIZ<15:0>:** Channel Destination Size bits

1111111111111111 = 65,535 byte destination size

•
•
•

0000000000000010 = 2 byte destination size

0000000000000001 = 1 byte destination size

0000000000000000 = 65,536 byte destination size

REGISTER 11-6: USBIE0CSR2: USB INDEXED ENDPOINT CONTROL STATUS REGISTER 2 (ENDPOINT 0)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	NAKLIM<4:0>				
23:16	R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0
	SPEED<1:0>		—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	—	RXCNT<6:0>						

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-29 **Unimplemented:** Read as '0'

bit 28-24 **NAKLIM<4:0>:** Endpoint 0 NAK Limit bits

The number of frames/microframes (Hi-Speed transfers) after which Endpoint 0 should time-out on receiving a stream of NAK responses.

bit 23-22 **SPEED<1:0>:** Operating Speed Control bits
11 = Low-Speed
10 = Full-Speed
01 = Hi-Speed
00 = Reserved

bit 21-7 **Unimplemented:** Read as '0'

bit 6-0 **RXCNT<6:0>:** Receive Count bits

The number of received data bytes in the Endpoint 0 FIFO. The value returned changes as the contents of the FIFO change and is only valid while RXPKTRDY is set.

17.1 Input Capture Control Registers

TABLE 17-2: INPUT CAPTURE 1 THROUGH INPUT CAPTURE 9 REGISTER MAP

Virtual Address (BF84_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
2000	IC1CON(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	FEDGE	C32	ICTMR	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000
2010	IC1BUF	31:16	IC1BUF<31:0>																xxxx
		15:0																	xxxx
2200	IC2CON(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	FEDGE	C32	ICTMR	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000
2210	IC2BUF	31:16	IC2BUF<31:0>																xxxx
		15:0																	xxxx
2400	IC3CON(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	FEDGE	C32	ICTMR	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000
2410	IC3BUF	31:16	IC3BUF<31:0>																xxxx
		15:0																	xxxx
2600	IC4CON(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	FEDGE	C32	ICTMR	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000
2610	IC4BUF	31:16	IC4BUF<31:0>																xxxx
		15:0																	xxxx
2800	IC5CON(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	FEDGE	C32	ICTMR	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000
2810	IC5BUF	31:16	IC5BUF<31:0>																xxxx
		15:0																	xxxx
2A00	IC6CON(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	FEDGE	C32	ICTMR	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000
2A10	IC6BUF	31:16	IC6BUF<31:0>																xxxx
		15:0																	xxxx
2C00	IC7CON(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	FEDGE	C32	ICTMR	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000
2C10	IC7BUF	31:16	IC7BUF<31:0>																xxxx
		15:0																	xxxx
2E00	IC8CON(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	FEDGE	C32	ICTMR	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000
2E10	IC8BUF	31:16	IC8BUF<31:0>																xxxx
		15:0																	xxxx
3000	IC9CON(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	FEDGE	C32	ICTMR	ICI<1:0>		ICOV	ICBNE	ICM<2:0>			0000
3010	IC9BUF	31:16	IC9BUF<31:0>																xxxx
		15:0																	xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 "CLR, SET, and INV Registers"** for more information.

REGISTER 17-1: ICxCON: INPUT CAPTURE x CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0
	ON	—	SIDL	—	—	—	FEDGE	C32
7:0	R/W-0	R/W-0	R/W-0	R-0	R-0	R/W-0	R/W-0	R/W-0
	ICTMR(1)	ICI<1:0>		ICOV	ICBNE	ICM<2:0>		

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit
-n = Bit Value at POR: (‘0’, ‘1’, x = unknown)	P = Programmable bit	r = Reserved bit

bit 31-16 **Unimplemented:** Read as ‘0’

bit 15 **ON:** Input Capture Module Enable bit
- 1 = Module is enabled
- 0 = Disable and reset module, disable clocks, disable interrupt generation and allow SFR modifications

bit 14 **Unimplemented:** Read as ‘0’

bit 13 **SIDL:** Stop in Idle Control bit
- 1 = Halt in CPU Idle mode
- 0 = Continue to operate in CPU Idle mode

bit 12-10 **Unimplemented:** Read as ‘0’

bit 9 **FEDGE:** First Capture Edge Select bit (only used in mode 6, ICM<2:0> = 110)
- 1 = Capture rising edge first
- 0 = Capture falling edge first

bit 8 **C32:** 32-bit Capture Select bit
- 1 = 32-bit timer resource capture
- 0 = 16-bit timer resource capture

bit 7 **ICTMR:** Timer Select bit (Does not affect timer selection when C32 (ICxCON<8>) is ‘1’)(1)
- 0 = Timery is the counter source for capture
- 1 = Timerx is the counter source for capture

bit 6-5 **ICI<1:0>:** Interrupt Control bits
- 11 = Interrupt on every fourth capture event
- 10 = Interrupt on every third capture event
- 01 = Interrupt on every second capture event
- 00 = Interrupt on every capture event

bit 4 **ICOV:** Input Capture Overflow Status Flag bit (read-only)
- 1 = Input capture overflow is occurred
- 0 = No input capture overflow is occurred

bit 3 **ICBNE:** Input Capture Buffer Not Empty Status bit (read-only)
- 1 = Input capture buffer is not empty; at least one more capture value can be read
- 0 = Input capture buffer is empty

bit 2-0 **ICM<2:0>:** Input Capture Mode Select bits
- 111 = Interrupt-Only mode (only supported while in Sleep mode or Idle mode)
- 110 = Simple Capture Event mode – every edge, specified edge first and every edge thereafter
- 101 = Prescaled Capture Event mode – every sixteenth rising edge
- 100 = Prescaled Capture Event mode – every fourth rising edge
- 011 = Simple Capture Event mode – every rising edge
- 010 = Simple Capture Event mode – every falling edge
- 001 = Edge Detect mode – every edge (rising and falling)
- 000 = Input Capture module is disabled

Note 1: Refer to Table 17-1 for Timerx and Timery selections.

19.0 SERIAL PERIPHERAL INTERFACE (SPI) AND INTER-IC SOUND (I^2S)

Note: This data sheet summarizes the features of the PIC32MZ EF family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 23. "Serial Peripheral Interface (SPI)"** (DS60001106) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

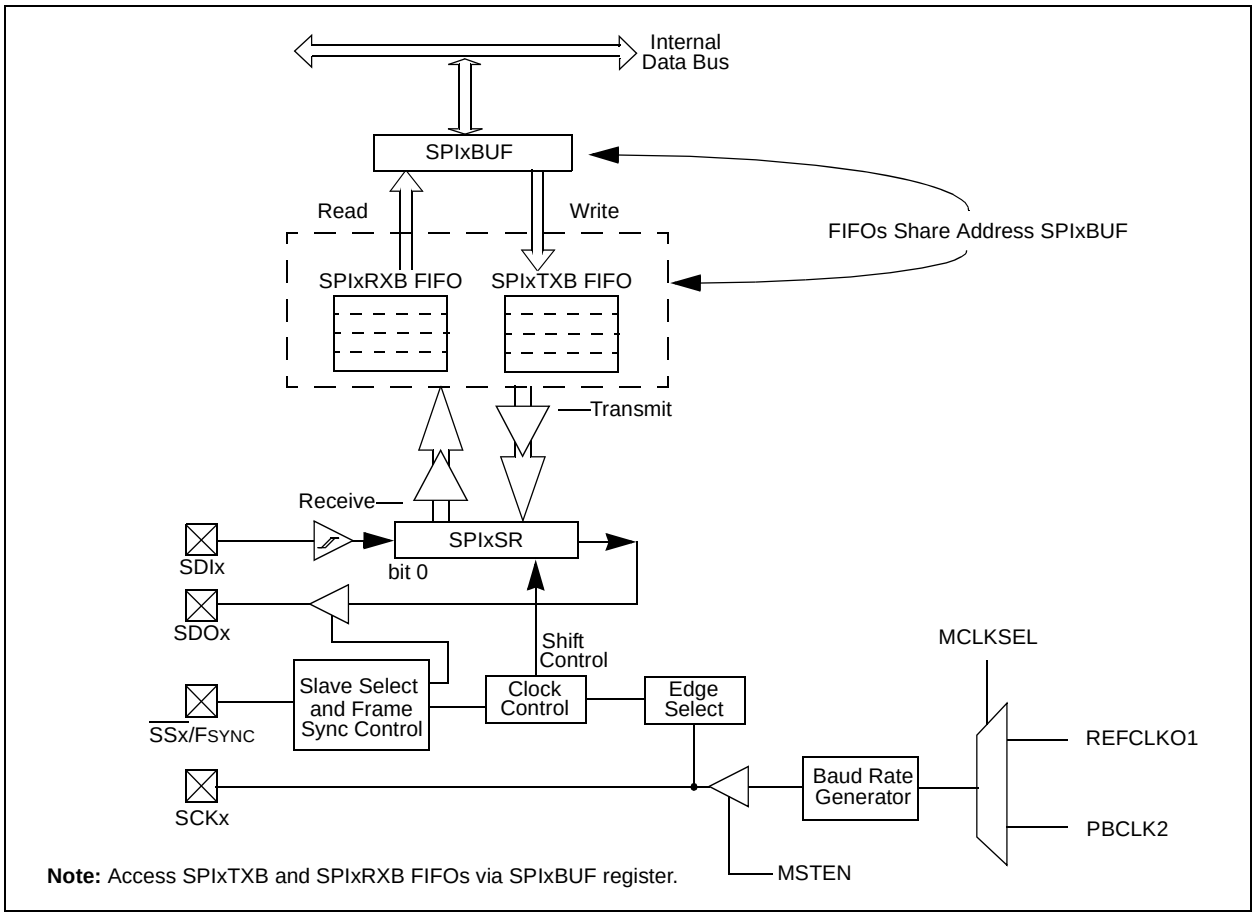
The SPI/I^2S module is a synchronous serial interface that is useful for communicating with external peripherals and other microcontroller devices, as well as digital audio devices. These peripheral devices may be Serial EEPROMs, Shift registers, display drivers, Analog-to-Digital Converters, and so on.

The SPI/I^2S module is compatible with Motorola® SPI and SIOP interfaces.

The following are key features of the SPI module:

- Master and Slave modes support
- Four different clock formats
- Enhanced Framed SPI protocol support
- User-configurable 8-bit, 16-bit and 32-bit data width
- Separate SPI FIFO buffers for receive and transmit
  - FIFO buffers act as 4/8/16-level deep FIFOs based on 32/16/8-bit data width
- Programmable interrupt event on every 8-bit, 16-bit and 32-bit data transfer
- Operation during Sleep and Idle modes
- Audio Codec Support:
  - I^2S protocol
  - Left-justified
  - Right-justified
  - PCM

FIGURE 19-1: SPI/I^2S MODULE BLOCK DIAGRAM



Note: Access SPIxTXB and SPIxRXB FIFOs via SPIxBUF register.

REGISTER 20-10: SQI1TXDATA: SQI TRANSMIT DATA BUFFER REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	TXDATA<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	TXDATA<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	TXDATA<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	TXDATA<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **TXDATA<31:0>:** Transmit Command Data bits

Data is loaded into this register before being transmitted. Prior to the data transfer, the data in TXDATA is loaded into the shift register (SFDR).

Multiple writes to TXDATA can occur while a transfer is in progress. There can be a maximum of eight commands that can be queued.

REGISTER 20-11: SQI1RXDATA: SQI RECEIVE DATA BUFFER REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	RXDATA<31:24>							
23:16	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	RXDATA<23:16>							
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	RXDATA<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	RXDATA<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **RXDATA<31:0>:** Receive Data Buffer bits

At the end of a data transfer, the data in the shift register is loaded into the RXDATA register. This register works like a FIFO. The depth of the receive buffer is eight words.

REGISTER 26-6: CEINTSRC: CRYPTO ENGINE INTERRUPT SOURCE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	R-0	R-0	R-0	R-0
	—	—	—	—	AREIF	PKTIF	CBDIF	PENDIF

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-4 **Unimplemented:** Read as '0'

bit 3 **AREIF:** Access Response Error Interrupt bit
1 = Error occurred trying to access memory outside the Crypto Engine
0 = No error has occurred

bit 2 **PKTIF:** DMA Packet Completion Interrupt Status bit
1 = DMA packet was completed
0 = DMA packet was not completed

bit 1 **CBDIF:** BD Transmit Status bit
1 = Last BD transmit was processed
0 = Last BD transmit has not been processed

bit 0 **PENDIF:** Crypto Engine Interrupt Pending Status bit
1 = Crypto Engine interrupt is pending (this value is the result of an OR of all interrupts in the Crypto Engine)
0 = Crypto Engine interrupt is not pending

REGISTER 28-6: ADCIMCON2: ADC INPUT MODE CONTROL REGISTER 2 (CONTINUED)

bit 6 **SIGN19:** AN19 Signed Data Mode bit(1)
1 = AN19 is using Signed Data mode
0 = AN19 is using Unsigned Data mode

bit 5 **DIFF18:** AN18 Mode bit
1 = AN18 is using Differential mode
0 = AN18 is using Single-ended mode

bit 4 **SIGN18:** AN18 Signed Data Mode bit
1 = AN18 is using Signed Data mode
0 = AN18 is using Unsigned Data mode

bit 3 **DIFF17:** AN17 Mode bit
1 = AN17 is using Differential mode
0 = AN17 is using Single-ended mode

bit 2 **SIGN17:** AN17 Signed Data Mode bit
1 = AN17 is using Signed Data mode
0 = AN17 is using Unsigned Data mode

bit 1 **DIFF16:** AN16 Mode bit
1 = AN16 is using Differential mode
0 = AN16 is using Single-ended mode

bit 0 **SIGN16:** AN16 Signed Data Mode bit
1 = AN16 is using Signed Data mode
0 = AN16 is using Unsigned Data mode

Note 1: This bit is not available on 64-pin devices.

REGISTER 30-15: ETHSTAT: ETHERNET CONTROLLER STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BUFCNT<7:0>(1)							
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0
	ETHBUSY(5)	TXBUSY(2,6)	RXBUSY(3,6)	—	—	—	—	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-24 **Unimplemented:** Read as '0'

bit 23-16 **BUFCNT<7:0>:** Packet Buffer Count bits(1)

Number of packet buffers received in memory. Once a packet has been successfully received, this register is incremented by hardware based on the number of descriptors used by the packet. Software decrements the counter (by writing to the BUFCDEC bit (ETHCON1<0>) for each descriptor used) after a packet has been read out of the buffer. The register does not roll over (0xFF to 0x00) when hardware tries to increment the register and the register is already at 0xFF. Conversely, the register does not roll under (0x00 to 0xFF) when software tries to decrement the register and the register is already at 0x0000. When software attempts to decrement the counter at the same time that the hardware attempts to increment the counter, the counter value will remain unchanged.

When this register value reaches 0xFF, the RX logic will halt (only if automatic Flow Control is enabled) awaiting software to write the BUFCDEC bit in order to decrement the register below 0xFF.

If automatic Flow Control is disabled, the RXDMA will continue processing and the BUFCNT will saturate at a value of 0xFF.

When this register is non-zero, the PKTPEND status bit will be set and an interrupt may be generated, depending on the value of the ETHIEN bit <PKTPENDIE> register.

When the ETHRXST register is written, the BUFCNT counter is automatically cleared to 0x00.

Note: BUFCNT will not be cleared when ON is set to '0'. This enables software to continue to utilize and decrement this count.

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **ETHBUSY:** Ethernet Module busy bit(5)

1 = Ethernet logic has been turned on (ON (ETHCON1<15>) = 1) or is completing a transaction
0 = Ethernet logic is idle

This bit indicates that the module has been turned on or is completing a transaction after being turned off.

Note 1: This bit is only used for RX operations.
2: This bit is only affected by TX operations.
3: This bit is only affected by RX operations.
4: This bit is affected by TX and RX operations.
5: This bit will be *set* when the ON bit (ETHCON1<15>) = 1.
6: This bit will be *cleared* when the ON bit (ETHCON1<15>) = 0.

NOTES:

TABLE 37-7: DC CHARACTERISTICS: IDLE CURRENT (IIDLE)

DC CHARACTERISTICS			Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial	
Parameter No.	**Typical(2)**	**Maximum(4)**	**Units**	**Conditions**
Idle Current (IIDLE): Core Off, Clock on Base Current (Note 1)				
DC30a	7	22	mA	4 MHz **(Note 3)**
DC31a	8	24	mA	10 MHz
DC32a	13	32	mA	60 MHz **(Note 3)**
DC33a	21	42	mA	130 MHz **(Note 3)**
DC34	26	48	mA	180 MHz **(Note 3)**
DC35	28	52	mA	200 MHz

Note 1: The test conditions for IIDLE current measurements are as follows:

- Oscillator mode is EC (for 8 MHz and below) and EC+PLL (for above 8 MHz) with OSC1 driven by external square wave from rail-to-rail, (OSC1 input clock input over/undershoot < 100 mV required)
- OSC2/CLKO is configured as an I/O input pin
- USB PLL is disabled (USBPMD = 1), VUSB3V3 is connected to VSS, PBCLKx divisor = 1:128 ('x' ≠ 7)
- CPU is in Idle mode (CPU core Halted)
- L1 Cache and Prefetch modules are disabled
- No peripheral modules are operating, (ON bit = 0), but the associated PMD bit is cleared (except USBPMD)
- WDT, DMT, Clock Switching, Fail-Safe Clock Monitor, and Secondary Oscillator are disabled
- All I/O pins are configured as inputs and pulled to VSS
- $\overline{MCLR}$ = VDD
- RTCC and JTAG are disabled

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: This parameter is characterized, but not tested in manufacturing.

4: Data in the "Maximum" column is at 3.3V, +85ºC at specified operating frequency, unless otherwise stated. Parameters are for design guidance only and are not tested.

FIGURE 37-22: PARALLEL MASTER PORT READ TIMING DIAGRAM

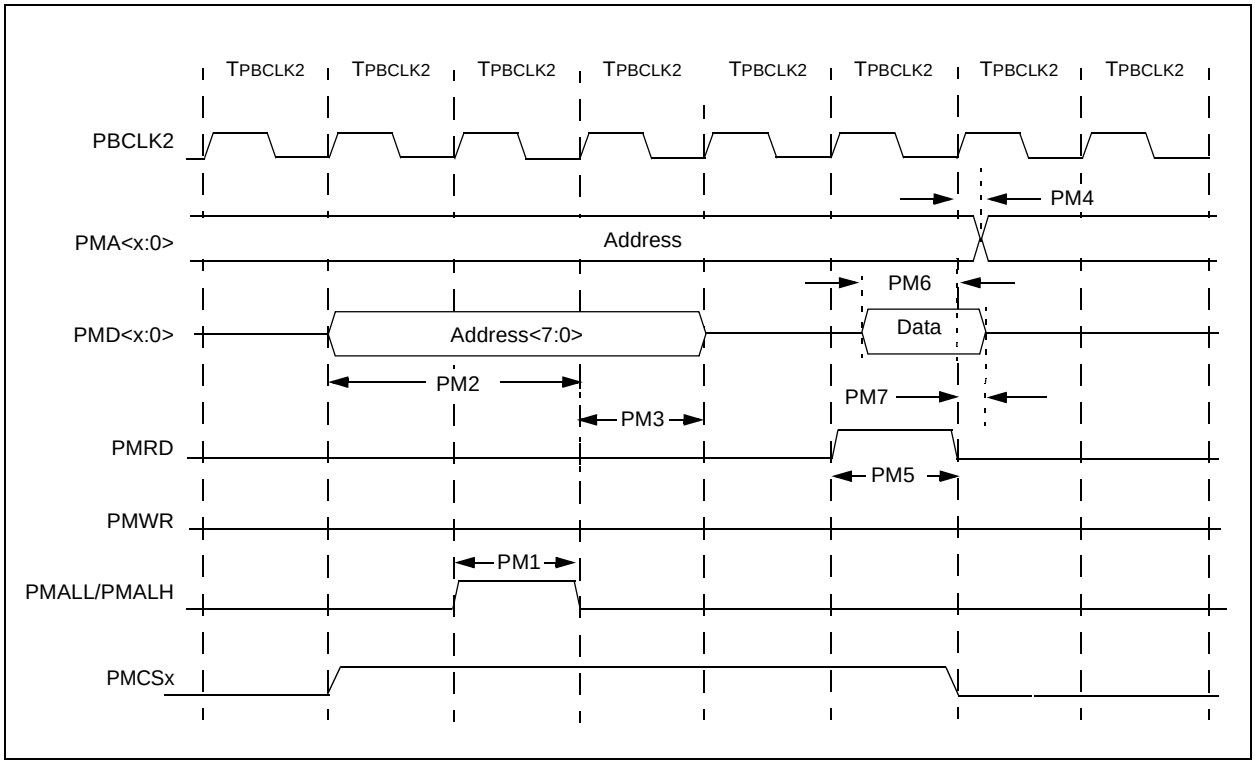


TABLE 37-43: PARALLEL MASTER PORT READ TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
PM1	TLAT	PMALL/PMALH Pulse Width	—	1 TPBCLK2	—	—	—
PM2	TADSU	Address Out Valid to PMALL/ PMALH Invalid (address setup time)	—	2 TPBCLK2	—	—	—
PM3	TADHOLD	PMALL/PMALH Invalid to Address Out Invalid (address hold time)	—	1 TPBCLK2	—	—	—
PM4	TAHOLD	PMRD Inactive to Address Out Invalid (address hold time)	5	—	—	ns	—
PM5	TRD	PMRD Pulse Width	—	1 TPBCLK2	—	—	—
PM6	TDSU	PMRD or PMENB Active to Data In Valid (data setup time)	15	—	—	ns	—
PM7	TDHOLD	PMRD or PMENB Inactive to Data In Invalid (data hold time)	—	80	—	ns	—

Note 1: These parameters are characterized, but not tested in manufacturing.

FIGURE 37-28: EBI PAGE READ TIMING

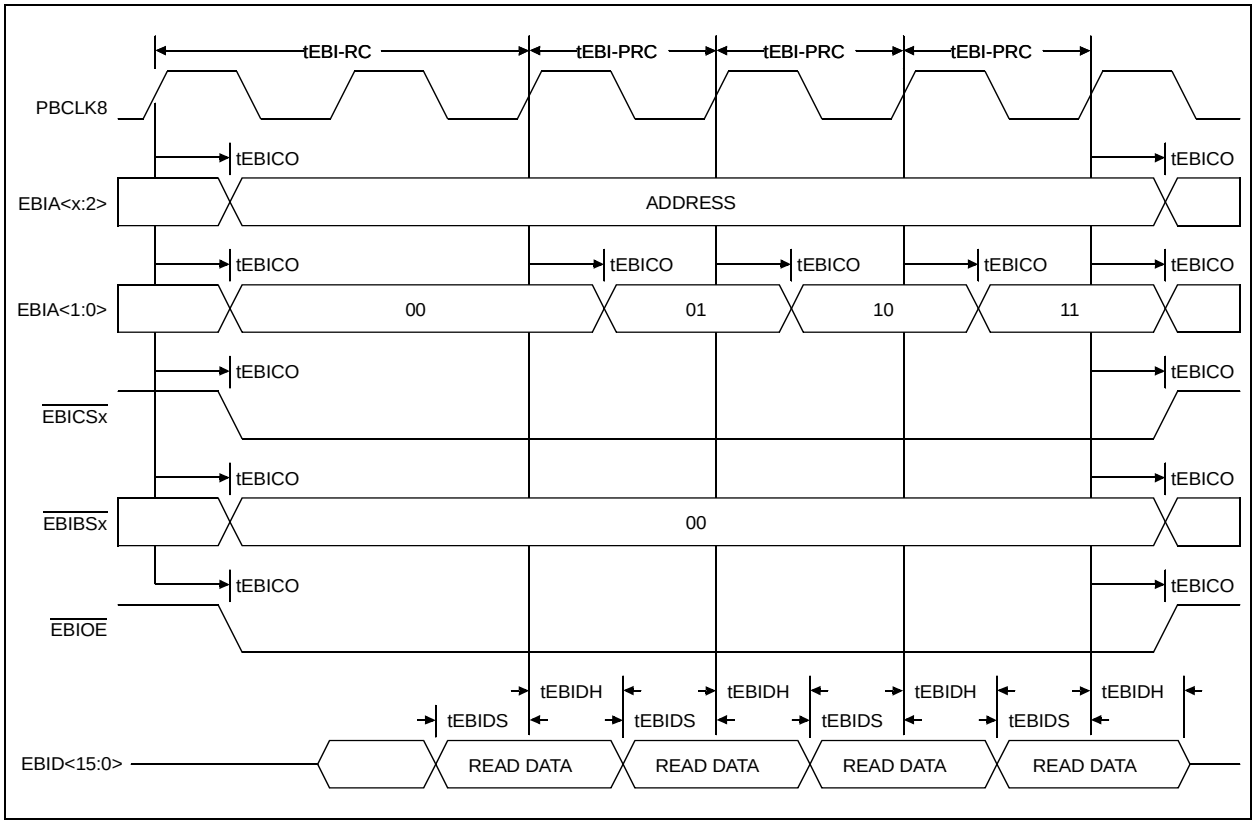


FIGURE 37-29: EBI WRITE TIMING

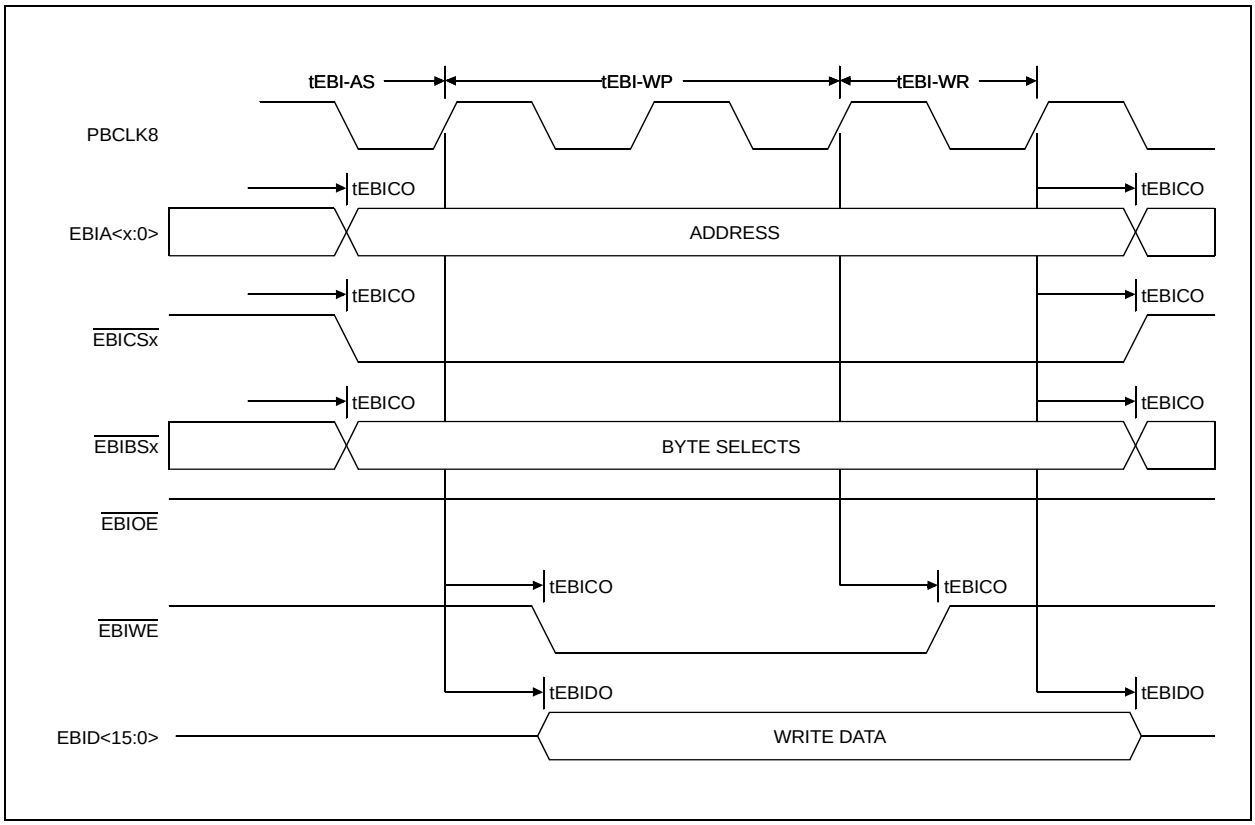


TABLE 37-47: EBI TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Symbol**	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
EB10	TEBICLK	Internal EBI Clock Period (PBCLK8)	10	—	—	ns	—
EB11	TEBIRC	EBI Read Cycle Time (TRC<5:0>)	20	—	—	ns	—
EB12	TEBIPRC	EBI Page Read Cycle Time (TPRC<3:0>)	20	—	—	ns	—
EB13	TEBIAS	EBI Write Address Setup (TAS<1:0>)	10	—	—	ns	—
EB14	TEBIWP	EBI Write Pulse Width (TWP<5:0>)	10	—	—	ns	—
EB15	TEBIWR	EBI Write Recovery Time (TWR<1:0>)	10	—	—	ns	—
EB16	TEBICO	EBI Output Control Signal Delay	—	—	5	ns	See **Note 1**
EB17	TEBIDO	EBI Output Data Signal Delay	—	—	5	ns	See **Note 1**
EB18	TEBIDS	EBI Input Data Setup	5	—	—	ns	See **Note 1**
EB19	TEBIDH	EBI Input Data Hold	3	—	—	ns	See **Note 1, 2**

Note 1: Maximum pin capacitance = 10 pF.

2: Hold time from EBI Address change is 0 ns.

TABLE 37-48: EBI THROUGHPUT REQUIREMENTS

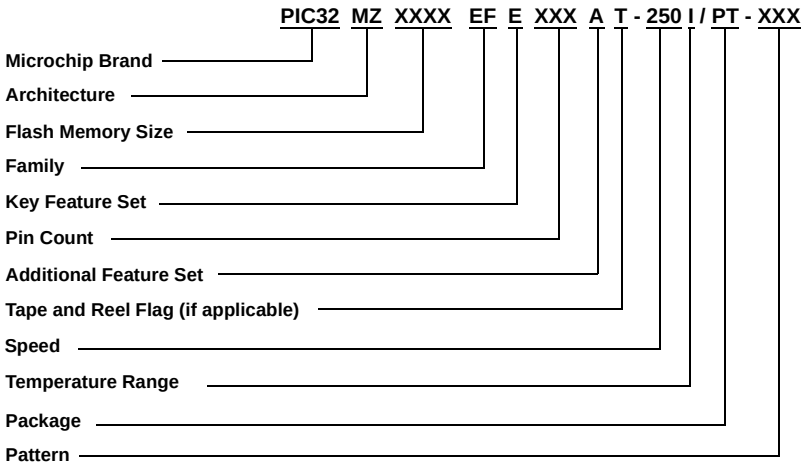
AC CHARACTERISTICS		Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
EB20	Asynchronous SRAM Read	—	100	—	Mbps	—
EB21	Asynchronous SRAM Write	—	533	—	Mbps	—

Note 1: Maximum pin capacitance = 10 pF.

2: Hold time from EBI Address change is 0 ns.

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.



Example:

PIC32MZ2048EFH144-I/PT:
Embedded Connectivity PIC32,
MIPS32® M-Class MPU core,
2048 KB program memory,
144-pin, with Floating Point Unit,
Industrial temperature, TQFP package.

Flash Memory Family

Architecture	MZ	= MIPS32® M-Class MPU Core
Flash Memory Size	0512	= 512 KB
	1024	= 1024 KB
	2048	= 2048 KB
Family	EF	= Embedded Connectivity Microcontroller Family with Floating Point Unit
Key Feature	E	= PIC32 EF Family Features (no CAN, no Crypto)
	F	= PIC32 EF Family Features (CAN, no Crypto)
	G	= PIC32 EF Family Features (no CAN, no Crypto)
	H	= PIC32 EF Family Features (CAN, no Crypto)
	K	= PIC32 EF Family Features (Crypto and CAN)
	M	= PIC32 EF Family Features (Crypto and CAN)
Pin Count	064	= 64-pin
	100	= 100-pin
	124	= 124-pin
	144	= 144-pin
Speed	Blank	= Up to 200 MHz
	250	= Up to 252 MHz
Temperature Range	I	= -40°C to +85°C (Industrial)
	E	= -40°C to +125°C (Extended)
Package	MR	= 64-Lead (9x9x0.9 mm) QFN (Plastic Quad Flatpack)
	PT	= 64-Lead (10x10x1 mm) TQFP (Thin Quad Flatpack)
	PT	= 100-Lead (12x12x1 mm) TQFP (Thin Quad Flatpack)
	PF	= 100-Lead (14x14x1 mm) TQFP (Thin Quad Flatpack)
	TL	= 124-Lead (9x9x0.9 mm) VTLA (Very Thin Leadless Array)
	PH	= 144-Lead (16x16x1 mm) TQFP (Thin Quad Flatpack)
	PL	= 144-Lead (20x20x1.40 mm) LQFP (Low Profile Quad Flatpack)
Pattern		Three-digit QTP, SQTP, Code or Special Requirements (blank otherwise)
	ES	= Engineering Sample