Microchip Technology - PIC32MZ2048EFM124T-I/TL Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	MIPS32® M-Class
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, PMP, SPI, SQI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	97
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	2.1V ~ 3.6V
Data Converters	A/D 48x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	124-VFTLA Dual Rows, Exposed Pad
Supplier Device Package	124-VTLA (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mz2048efm124t-i-tl

2.0 GUIDELINES FOR GETTING STARTED WITH 32-BIT MICROCONTROLLERS

Note 1: This data sheet summarizes the features of the PIC32MZ EF family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

2.1 Basic Connection Requirements

Getting started with the PIC32MZ EF family of 32-bit Microcontrollers (MCUs) requires attention to a minimal set of device pin connections before proceeding with development. The following is a list of pin names, which must always be connected:

- All VDD and VSS pins (see **2.2 "Decoupling Capacitors"**)
- All AVDD and AVSS pins, even if the ADC module is not used (see **2.2 "Decoupling Capacitors"**)
- $\overline{\text{MCLR}}$ pin (see **2.3 "Master Clear (MCLR) Pin"**)
- PGECx/PGEDx pins, used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes (see **2.4 "ICSP Pins"**)
- OSC1 and OSC2 pins, when external oscillator source is used (see **2.7 "External Oscillator Pins"**)

The following pin(s) may be required as well:

VREF+/VREF- pins, used when external voltage reference for the ADC module is implemented.

Note: The AVDD and AVSS pins must be connected, regardless of ADC use and the ADC voltage reference source.

2.2 Decoupling Capacitors

The use of decoupling capacitors on power supply pins, such as VDD, VSS, AVDD and AVSS is required. See Figure 2-1.

Consider the following criteria when using decoupling capacitors:

- **Value and type of capacitor:** A value of 0.1 µF (100 nF), 10-20V is recommended. The capacitor should be a low Equivalent Series Resistance (low-ESR) capacitor and have resonance frequency in the range of 20 MHz and higher. It is further recommended that ceramic capacitors be used.
- **Placement on the printed circuit board:** The decoupling capacitors should be placed as close to the pins as possible. It is recommended that the capacitors be placed on the same side of the board as the device. If space is constricted, the capacitor can be placed on another layer on the PCB using a via; however, ensure that the trace length from the pin to the capacitor is within one-quarter inch (6 mm) in length.
- **Handling high frequency noise:** If the board is experiencing high frequency noise, upward of tens of MHz, add a second ceramic-type capacitor in parallel to the above described decoupling capacitor. The value of the second capacitor can be in the range of 0.01 µF to 0.001 µF. Place this second capacitor next to the primary decoupling capacitor. In high-speed circuit designs, consider implementing a decade pair of capacitances as close to the power and ground pins as possible. For example, 0.1 µF in parallel with 0.001 µF.
- **Maximizing performance:** On the board layout from the power supply circuit, run the power and return traces to the decoupling capacitors first, and then to the device pins. This ensures that the decoupling capacitors are first in the power chain. Equally important is to keep the trace length between the capacitor and the power pins to a minimum thereby reducing PCB track inductance.

TABLE 4-6: SYSTEM BUS TARGETS AND ASSOCIATED PROTECTION REGISTERS

Target Number	Target Description[5]	SBTxREGy Register							SBTxRDy Register		SBTxWRy Register	
		Name	Region Base (BASE<21:0>) (see Note 2)	Physical Start Address	Region Size (SIZE<4:0>) (see Note 3)	Region Size	Priority (PRI)	Priority Level	Name	Read Permission (GROUP3, GROUP2, GROUP1, GROUP0)	Name	Write Permission (GROUP3, GROUP2, GROUP1, GROUP0)
0	System Bus	SBT0REG0	R	0x1F8F0000	R	64 KB	—	0	SBT0RD0	R/W[1]	SBT0WR0	R/W[1]
		SBT0REG1	R	0x1F8F8000	R	32 KB	—	3	SBT0RD1	R/W[1]	SBT0WR1	R/W[1]
1	**Flash Memory[6]:** Program Flash Boot Flash Prefetch Module	SBT1REG0	R	0x1D000000	R[4]	R[4]	—	0	SBT1RD0	R/W[1]	SBT1WR0	0, 0, 0, 0
		SBT1REG2	R	0x1F8E0000	R	4 KB	1	2	SBT1RD2	R/W[1]	SBT1WR2	R/W[1]
		SBT1REG3	R/W	R/W	R/W	R/W	1	2	SBT1RD3	R/W[1]	SBT1WR3	0, 0, 0, 0
		SBT1REG4	R/W	R/W	R/W	R/W	1	2	SBT1RD4	R/W[1]	SBT1WR4	0, 0, 0, 0
		SBT1REG5	R/W	R/W	R/W	R/W	1	2	SBT1RD5	R/W[1]	SBT1WR5	0, 0, 0, 0
		SBT1REG6	R/W	R/W	R/W	R/W	1	2	SBT1RD6	R/W[1]	SBT1WR6	0, 0, 0, 0
		SBT1REG7	R/W	R/W	R/W	R/W	0	1	SBT1RD7	R/W[1]	SBT1WR7	0, 0, 0, 0
		SBT1REG8	R/W	R/W	R/W	R/W	0	1	SBT1RD8	R/W[1]	SBT1WR8	0, 0, 0, 0
2	RAM Bank 1 Memory	SBT2REG0	R	0x00000000	R[4]	R[4]	—	0	SBT2RD0	R/W[1]	SBT2WR0	R/W[1]
		SBT2REG1	R/W	R/W	R/W	R/W	—	3	SBT2RD1	R/W[1]	SBT2WR1	R/W[1]
		SBT2REG2	R/W	R/W	R/W	R/W	0	1	SBT2RD2	R/W[1]	SBT2WR2	R/W[1]
3	RAM Bank 2 Memory	SBT3REG0	R[4]	R[4]	R[4]	R[4]	—	0	SBT3RD0	R/W[1]	SBT3WR0	R/W[1]
		SBT3REG1	R/W	R/W	R/W	R/W	—	3	SBT3RD1	R/W[1]	SBT3WR1	R/W[1]
		SBT3REG2	R/W	R/W	R/W	R/W	0	1	SBT3RD2	R/W[1]	SBT3WR2	R/W[1]
4	External Memory via EBI and EBI Module[6]	SBT4REG0	R	0x20000000	R	64 MB	—	0	SBT4RD0	R/W[1]	SBT4WR0	R/W[1]
		SBT4REG2	R	0x1F8E1000	R	4 KB	0	1	SBT4RD2	R/W[1]	SBT4WR2	R/W[1]
5	**Peripheral Set 1:** System Control Flash Control DMT/WDT RTCC CVR PPS Input PPS Output Interrupts DMA	SBT5REG0	R	0x1F800000	R	128 KB	—	0	SBT5RD0	R/W[1]	SBT5WR0	R/W[1]
		SBT5REG1	R/W	R/W	R/W	R/W	—	3	SBT5RD1	R/W[1]	SBT5WR1	R/W[1]
		SBT5REG2	R/W	R/W	R/W	R/W	0	1	SBT5RD2	R/W[1]	SBT5WR2	R/W[1]

Legend: R = Read; R/W = Read/Write; 'x' in a register name = 0-13; 'y' in a register name = 0-8.

Note 1: Reset values for these bits are '0', '1', '1', '1', respectively.

2: The BASE<21:0> bits must be set to the corresponding Physical Address and right shifted by 10 bits. For Read-only bits, this value is set by hardware on Reset.

3: The SIZE<4:0> bits must be set to the corresponding Region Size, based on the following formula: Region Size = $2^{(SIZE-1)}$ x 1024 bytes. For read-only bits, this value is set by hardware on Reset.

4: Refer to the Device Memory Maps (Figure 4-1 through Figure 4-4) for specific device memory sizes and start addresses.

5: See Table 4-1for information on specific target memory size and start addresses.

6: The SBTxREG1 SFRs are reserved, and therefore, are not listed in this table for this target.

REGISTER 4-4: SBTxELOG2: SYSTEM BUS TARGET 'x' ERROR LOG REGISTER 2 ('x' = 0-13)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	R-0	R-0
	—	—	—	—	—	—	GROUP<1:0>	

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared

bit 31-3 **Unimplemented:** Read as '0'

bit 1-0 **GROUP<1:0>:** Requested Permissions Group bits
11 = Group 3
10 = Group 2
01 = Group 1
00 = Group 0

Note: Refer to Table 4-6 for the list of available targets and their descriptions.

REGISTER 4-5: SBTxECON: SYSTEM BUS TARGET 'x' ERROR CONTROL REGISTER ('x' = 0-13)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
	—	—	—	—	—	—	—	ERRP
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared

bit 31-25 **Unimplemented:** Read as '0'

bit 24 **ERRP:** Error Control bit
1 = Report protection group violation errors
0 = Do not report protection group violation errors

bit 23-0 **Unimplemented:** Read as '0'

Note: Refer to Table 4-6 for the list of available targets and their descriptions.

REGISTER 11-17: USBEOFRST: USB END-OF-FRAME/SOFT RESET CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
	—	—	—	—	—	—	NRSTX	NRST
23:16	R/W-0	R/W-1	R/W-1	R/W-1	R/W-0	R.W-0	R/W-1	R/W-0
	LSEOF<7:0>							
15:8	R/W-0	R/W-1	R/W-1	R/W-1	R/W-0	R.W-1	R/W-1	R/W-1
	FSEOF<7:0>							
7:0	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R.W-0	R/W-0	R/W-0
	HSEOF<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-26 **Unimplemented:** Read as '0'

bit 25 **NRSTX:** Reset of XCLK Domain bit
1 = Reset the XCLK domain, which is clock recovered from the received data by the PHY
0 = Normal operation

bit 24 **NRST:** Reset of CLK Domain bit
1 = Reset the CLK domain, which is clock recovered from the peripheral bus
0 = Normal operation

bit 23-16 **LSEOF<7:0>:** Low-Speed EOF bits
These bits set the Low-Speed transaction in units of 1.067 µs (default setting is 121.6 µs) prior to the EOF to stop new transactions from beginning.

bit 15-8 **FSEOF<7:0>:** Full-Speed EOF bits
These bits set the Full-Speed transaction in units of 533.3 µs (default setting is 63.46 µs) prior to the EOF to stop new transactions from beginning.

bit 7-0 **HSEOF<7:0>:** Hi-Speed EOF bits
These bits set the Hi-Speed transaction in units of 133.3 µs (default setting is 17.07µs) prior to the EOF to stop new transactions from beginning.

REGISTER 21-1: I2CxCON: I²C CONTROL REGISTER (CONTINUED)

bit 12 **SCLREL:** SCLx Release Control bit (when operating as I²C slave)
1 = Release SCLx clock
0 = Hold SCLx clock low (clock stretch)
If STREN = 1:
Bit is R/W (i.e., software can write '0' to initiate stretch and write '1' to release clock). Hardware clear at beginning of slave transmission. Hardware clear at end of slave reception.
If STREN = 0:
Bit is R/S (i.e., software can only write '1' to release clock). Hardware clear at beginning of slave transmission.

bit 11 **STRICT:** Strict I²C Reserved Address Rule Enable bit
1 = Strict reserved addressing is enforced. Device does not respond to reserved address space or generate addresses in reserved address space.
0 = Strict I²C Reserved Address Rule is not enabled

bit 10 **A10M:** 10-bit Slave Address bit
1 = I2CxADD is a 10-bit slave address
0 = I2CxADD is a 7-bit slave address

bit 9 **DISSLW:** Disable Slew Rate Control bit
1 = Slew rate control is disabled
0 = Slew rate control is enabled

bit 8 **SMEN:** SMBus Input Levels bit
1 = Enable I/O pin thresholds compliant with SMBus specification
0 = Disable SMBus input thresholds

bit 7 **GCEN:** General Call Enable bit (when operating as I²C slave)
1 = Enable interrupt when a general call address is received in the I2CxRSR (module is enabled for reception)
0 = General call address is disabled

bit 6 **STREN:** SCLx Clock Stretch Enable bit (when operating as I²C slave)
Used in conjunction with SCLREL bit.
1 = Enable software or receive clock stretching
0 = Disable software or receive clock stretching

bit 5 **ACKDT:** Acknowledge Data bit (when operating as I²C master, applicable during master receive)
Value that is transmitted when the software initiates an Acknowledge sequence.
1 = Send NACK during Acknowledge
0 = Send ACK during Acknowledge

bit 4 **ACKEN:** Acknowledge Sequence Enable bit
(when operating as I²C master, applicable during master receive)
1 = Initiate Acknowledge sequence on SDAx and SCLx pins and transmit ACKDT data bit. Hardware clear at end of master Acknowledge sequence.
0 = Acknowledge sequence not in progress

bit 3 **RCEN:** Receive Enable bit (when operating as I²C master)
1 = Enables Receive mode for I²C. Hardware clear at end of eighth bit of master receive data byte.
0 = Receive sequence not in progress

bit 2 **PEN:** Stop Condition Enable bit (when operating as I²C master)
1 = Initiate Stop condition on SDAx and SCLx pins. Hardware clear at end of master Stop sequence.
0 = Stop condition not in progress

bit 1 **RSEN:** Repeated Start Condition Enable bit (when operating as I²C master)
1 = Initiate Repeated Start condition on SDAx and SCLx pins. Hardware clear at end of master Repeated Start sequence.
0 = Repeated Start condition not in progress

bit 0 **SEN:** Start Condition Enable bit (when operating as I²C master)
1 = Initiate Start condition on SDAx and SCLx pins. Hardware clear at end of master Start sequence.
0 = Start condition not in progress

TABLE 22-1: UART1 THROUGH UART6 REGISTER MAP (CONTINUED)

Virtual Address (BF82_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
2600	U4MODE(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	IREN	RTSMD	—	UEN<1:0>		WAKE	LPBACK	ABAUD	RXINV	BRGH	PDSEL<1:0>		STSEL	0000
2610	U4STA(1)	31:16	—	—	—	—	—	—	—	ADM_EN	ADDR<7:0>								0000
		15:0	UTXISEL<1:0>		UTXINV	URXEN	UTXBRK	UTXEN	UTXBF	TRMT	URXISEL<1:0>		ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110
2620	U4TXREG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	TX8	Transmit Register								0000
2630	U4RXREG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	RX8	Receive Register								0000
2640	U4BRG(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	Baud Rate Generator Prescaler																0000
2800	U5MODE(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	IREN	RTSMD	—	UEN<1:0>		WAKE	LPBACK	ABAUD	RXINV	BRGH	PDSEL<1:0>		STSEL	0000
2810	U5STA(1)	31:16	—	—	—	—	—	—	—	ADM_EN	ADDR<7:0>								0000
		15:0	UTXISEL<1:0>		UTXINV	URXEN	UTXBRK	UTXEN	UTXBF	TRMT	URXISEL<1:0>		ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110
2820	U5TXREG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	TX8	Transmit Register								0000
2830	U5RXREG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	RX8	Receive Register								0000
2840	U5BRG(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	Baud Rate Generator Prescaler																0000
2A00	U6MODE(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	IREN	RTSMD	—	UEN<1:0>		WAKE	LPBACK	ABAUD	RXINV	BRGH	PDSEL<1:0>		STSEL	0000
2A10	U6STA(1)	31:16	—	—	—	—	—	—	—	ADM_EN	ADDR<7:0>								0000
		15:0	UTXISEL<1:0>		UTXINV	URXEN	UTXBRK	UTXEN	UTXBF	TRMT	URXISEL<1:0>		ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110
2A20	U6TXREG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	TX8	Transmit Register								0000
2A30	U6RXREG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	RX8	Receive Register								0000
2A40	U6BRG(1)	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	Baud Rate Generator Prescaler																0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 "CLR, SET, and INV Registers"** for more information.

26.0 CRYPTO ENGINE

Note: This data sheet summarizes the features of the PIC32MZ EF family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 49. "Crypto Engine (CE) and Random Number Generator (RNG)"** (DS60001246) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

The Crypto Engine is intended to accelerate applications that need cryptographic functions. By executing these functions in the hardware module, software overhead is reduced and actions, such as encryption, decryption, and authentication can execute much more quickly.

The Crypto Engine uses an internal descriptor-based DMA for efficient programming of the security association data and packet pointers (allowing scatter/gather data fetching). An intelligent state machine schedules the Crypto Engines based on the protocol selection and packet boundaries. The hardware engines can perform the encryption and authentication in sequence or in parallel.

The following are key features of the Crypto Engine:

- Bulk ciphers and hash engines
- Integrated DMA to off-load processing:
  - Buffer descriptor-based
  - Secure association per buffer descriptor
- Some functions can execute in parallel

Bulk ciphers that are handled by the Crypto Engine include:

- AES:
  - 128-bit, 192-bit, and 256-bit key sizes
  - CBC, ECB, CTR, CFB, and OFB modes
- DES/TDES:
  - CBC, ECB, CFB, and OFB modes

Authentication engines that are available through the Crypto Engine include:

- SHA-1
- SHA-256
- MD-5
- AES-GCM
- HMAC operation (for all authentication engines)

The rate of data that can be processed by the Crypto Engine depends on these factors:

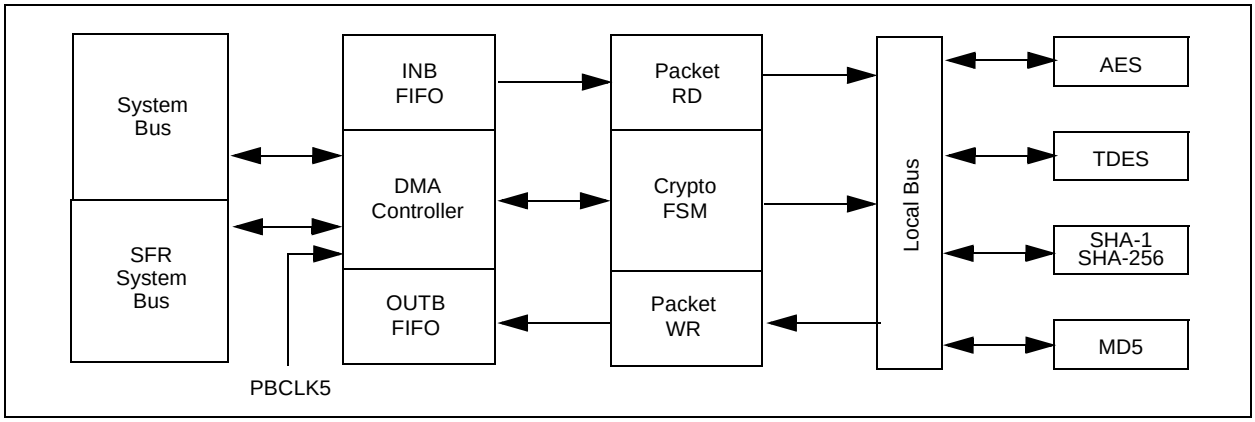
- Which engine is in use
- Whether the engines are used in parallel or in series
- The demands on source and destination memories by other parts of the system (i.e., CPU, DMA, etc.)
- The speed of PBCLK5, which drives the Crypto Engine

Table 26-1 shows typical performance for various engines.

TABLE 26-1: CRYPTO ENGINE PERFORMANCE

Engine/ Algorithm	Performance Factor (Mbps/MHz)	Maximum Mbps (PBCLK5 = 100 MHz)
DES	14.4	1440
TDES	6.6	660
AES-128	9.0	900
AES-192	7.9	790
AES-256	7.2	720
MD5	15.6	1560
SHA-1	13.2	1320
SHA-256	9.3	930

FIGURE 26-1: CRYPTO ENGINE BLOCK DIAGRAM



REGISTER 26-3: CEBDADDR: CRYPTO ENGINE BUFFER DESCRIPTOR REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	BDPADDR<31:24>							
23:16	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	BDPADDR<23:16>							
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	BDPADDR<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	BDPADDR<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **BDPADDR<31:0>:** Current Buffer Descriptor Process Address Status bits

These bits contain the current descriptor address that is being processed by the Buffer Descriptor Processor (BDP).

REGISTER 26-4: CEBDPADDR: CRYPTO ENGINE BUFFER DESCRIPTOR PROCESSOR REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BASEADDR<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BASEADDR<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BASEADDR<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BASEADDR<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **BASEADDR<31:0>:** Buffer Descriptor Base Address bits

These bits contain the physical address of the first Buffer Descriptor in the Buffer Descriptor chain. When enabled, the Crypto DMA begins fetching Buffer Descriptors from this address.

REGISTER 26-7: CEINTEN: CRYPTO ENGINE INTERRUPT ENABLE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	AREIE	PKTIE	BDPIE	PENDIE(1)

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-4 **Unimplemented:** Read as '0'

bit 3 **AREIE:** Access Response Error Interrupt Enable bit
- 1 = Access response error interrupts are enabled
- 0 = Access response error interrupts are not enabled

bit 2 **PKTIE:** DMA Packet Completion Interrupt Enable bit
- 1 = DMA packet completion interrupts are enabled
- 0 = DMA packet completion interrupts are not enabled

bit 1 **BDPIE:** DMA Buffer Descriptor Processor Interrupt Enable bit
- 1 = BDP interrupts are enabled
- 0 = BDP interrupts are not enabled

bit 0 **PENDIE:** Master Interrupt Enable bit(1)
- 1 = Crypto Engine interrupts are enabled
- 0 = Crypto Engine interrupts are not enabled

Note 1: The PENDIE bit is a global enable bit and must be enabled together with the other interrupts desired.

26.2 Crypto Engine Buffer Descriptors

Host software creates a linked list of buffer descriptors and the hardware updates them. Table 26-3 provides a list of the Crypto Engine buffer descriptors, followed by format descriptions of each buffer descriptor (see Figure 26-2 through Figure 26-9).

TABLE 26-3: CRYPTO ENGINE BUFFER DESCRIPTORS

Name (see Note 1)		Bit 31/2315/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
BD_CTRL	31:24	DESC_EN	—	CRY_MODE<2:0>			—	—	—
	23:16	—	SA_FETCH_EN	—	—	LAST_BD	LIFM	PKT_INT_EN	CBD_INT_EN
	15:8	BD_BUFLEN<15:8>							
	7:0	BD_BUFLEN<7:0>							
BD_SA_ADDR	31:24	BD_SAADDR<31:24>							
	23:16	BD_SAADDR<23:16>							
	15:8	BD_SAADDR<15:8>							
	7:0	BD_SAADR<7:0>							
BD_SCRADDR	31:24	BD_SRCADDR<31:24>							
	23:16	BD_SRCADDR<23:16>							
	15:8	BD_SRCADDR<15:8>							
	7:0	BD_SRCADDR<7:0>							
BD_DSTADDR	31:24	BD_DSTADDR<31:24>							
	23:16	BD_DSTADDR<23:16>							
	15:8	BD_DSTADDR<15:8>							
	7:0	BD_DSTADDR<7:0>							
BD_NXTPTR	31:24	BD_NXTADDR<31:24>							
	23:16	BD_NXTADDR<23:16>							
	15:8	BD_NXTADDR<15:8>							
	7:0	BD_NXTADDR<7:0>							
BD_UPDPTR	31:24	BD_UPDADDR<31:24>							
	23:16	BD_UPDADDR<23:16>							
	15:8	BD_UPDADDR<15:8>							
	7:0	BD_UPDADDR<7:0>							
BD_MSG_LEN	31:24	MSG_LENGTH<31:24>							
	23:16	MSG_LENGTH<23:16>							
	15:8	MSG_LENGTH<15:8>							
	7:0	MSG_LENGTH<7:0>							
BD_ENC_OFF	31:24	ENCR_OFFSET<31:24>							
	23:16	ENCR_OFFSET<23:16>							
	15:8	ENCR_OFFSET<15:8>							
	7:0	ENCR_OFFSET<7:0>							

Note 1: The buffer descriptor must be allocated in memory on a 64-bit boundary.

FIGURE 28-1: ADC BLOCK DIAGRAM

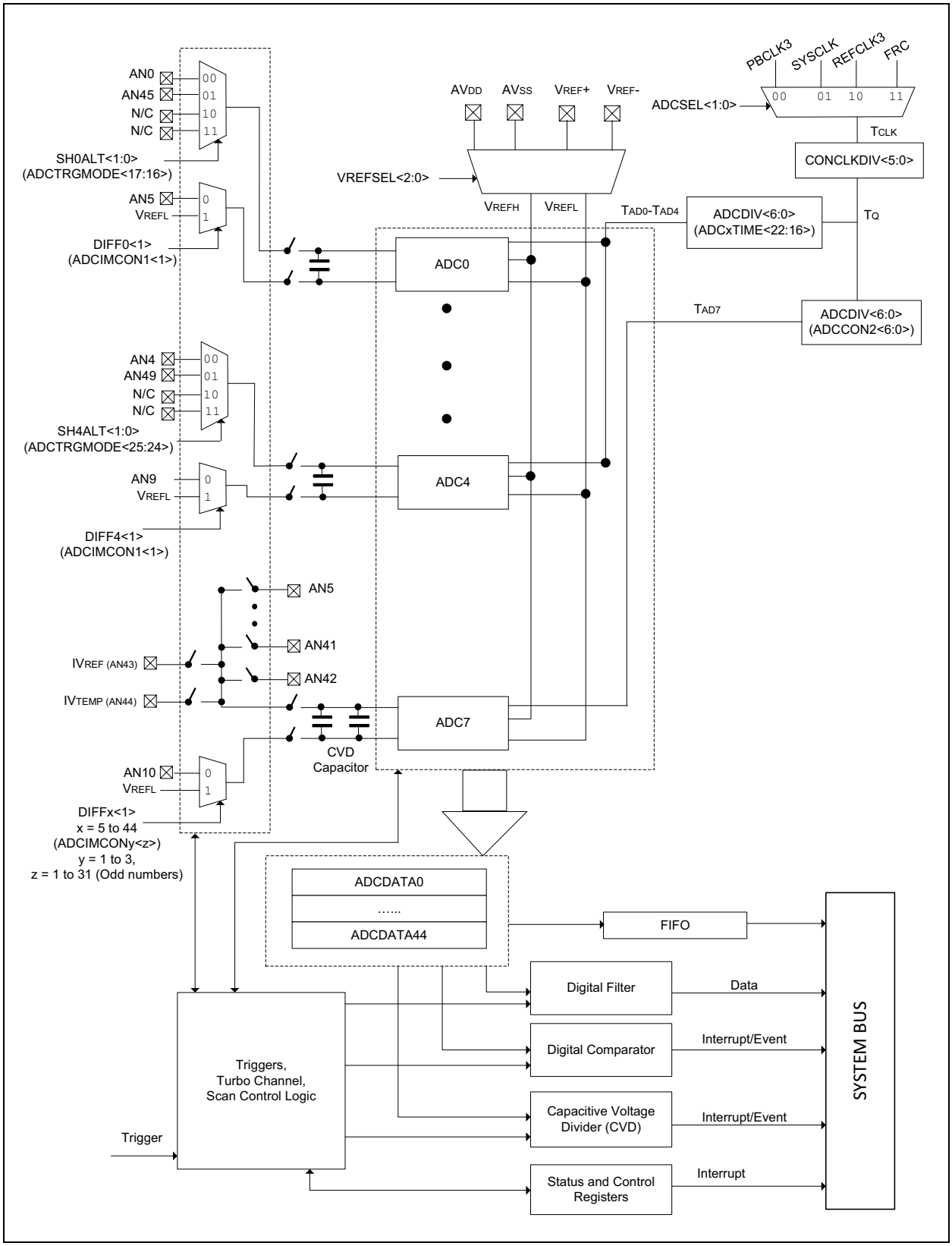


TABLE 28-1: ADC REGISTER MAP (CONTINUED)

Virtual Address (BF84_#)	Register Name	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
B234	ADCDATA13	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
B238	ADCDATA14	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
B23C	ADCDATA15	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
B240	ADCDATA16	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
B244	ADCDATA17	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
B248	ADCDATA18	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
B24C	ADCDATA19(1)	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
B250	ADCDATA20(1)	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
B254	ADCDATA21(1)	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
B258	ADCDATA22(1)	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
B25C	ADCDATA23(1)	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
B260	ADCDATA24(1)	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
B264	ADCDATA25(1)	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
B268	ADCDATA26(1)	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
B26C	ADCDATA27(1)	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
B270	ADCDATA28(1)	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
B274	ADCDATA29(1)	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
B278	ADCDATA30(1)	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000
B27C	ADCDATA31(1)	31:16	DATA<31:16>																0000
		15:0	DATA<15:0>																0000

Note 1: This bit or register is not available on 64-pin devices.
2: This bit or register is not available on 64-pin and 100-pin devices.
3: Before enabling the ADC, the user application must initialize the ADC calibration values by copying them from the factory-programmed DEVADCx Flash registers into the corresponding ADCxCFG registers.

REGISTER 28-25: ADCDATAx: ADC OUTPUT DATA REGISTER ('x' = 0 THROUGH 44)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	DATA<31:24>							
23:16	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	DATA<23:16>							
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	DATA<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	DATA<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **DATA<31:0>:** ADC Converted Data Output bits.

Note 1: The registers, ADCDATA19 through ADCDATA34, are not available on 64-pin devices.

2: The registers, ADCDATA35 through ADCDATA42, are not available on 64-pin and 100-pin devices.

3: When an alternate input is used as the input source for a dedicated ADC module, the data output is still read from the Primary input Data Output Register.

4: Reading the ADCDATAx register value after changing the FRACT bit converts the data into the format specified by FRACT bit.

REGISTER 29-18: CiRXFn: CAN ACCEPTANCE FILTER 'n' REGISTER 7 ('n' = 0-31)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	SID<10:3>							
23:16	R/W-x	R/W-x	R/W-x	U-0	R/W-0	U-0	R/W-x	R/W-x
	SID<2:0>			—	EXID	—	EID<17:16>	
15:8	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	EID<15:8>							
7:0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	EID<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-21 **SID<10:0>:** Standard Identifier bits
1 = Message address bit SIDx must be '1' to match filter
0 = Message address bit SIDx must be '0' to match filter

bit 20 **Unimplemented:** Read as '0'

bit 19 **EXID:** Extended Identifier Enable bits
1 = Match only messages with extended identifier addresses
0 = Match only messages with standard identifier addresses

bit 18 **Unimplemented:** Read as '0'

bit 17-0 **EID<17:0>:** Extended Identifier bits
1 = Message address bit EIDx must be '1' to match filter
0 = Message address bit EIDx must be '0' to match filter

Note: This register can only be modified when the filter is disabled (FLTENn = 0).

30.0 ETHERNET CONTROLLER

Note: This data sheet summarizes the features of the PIC32MZ EF family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 35. "Ethernet Controller"** (DS60001155) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

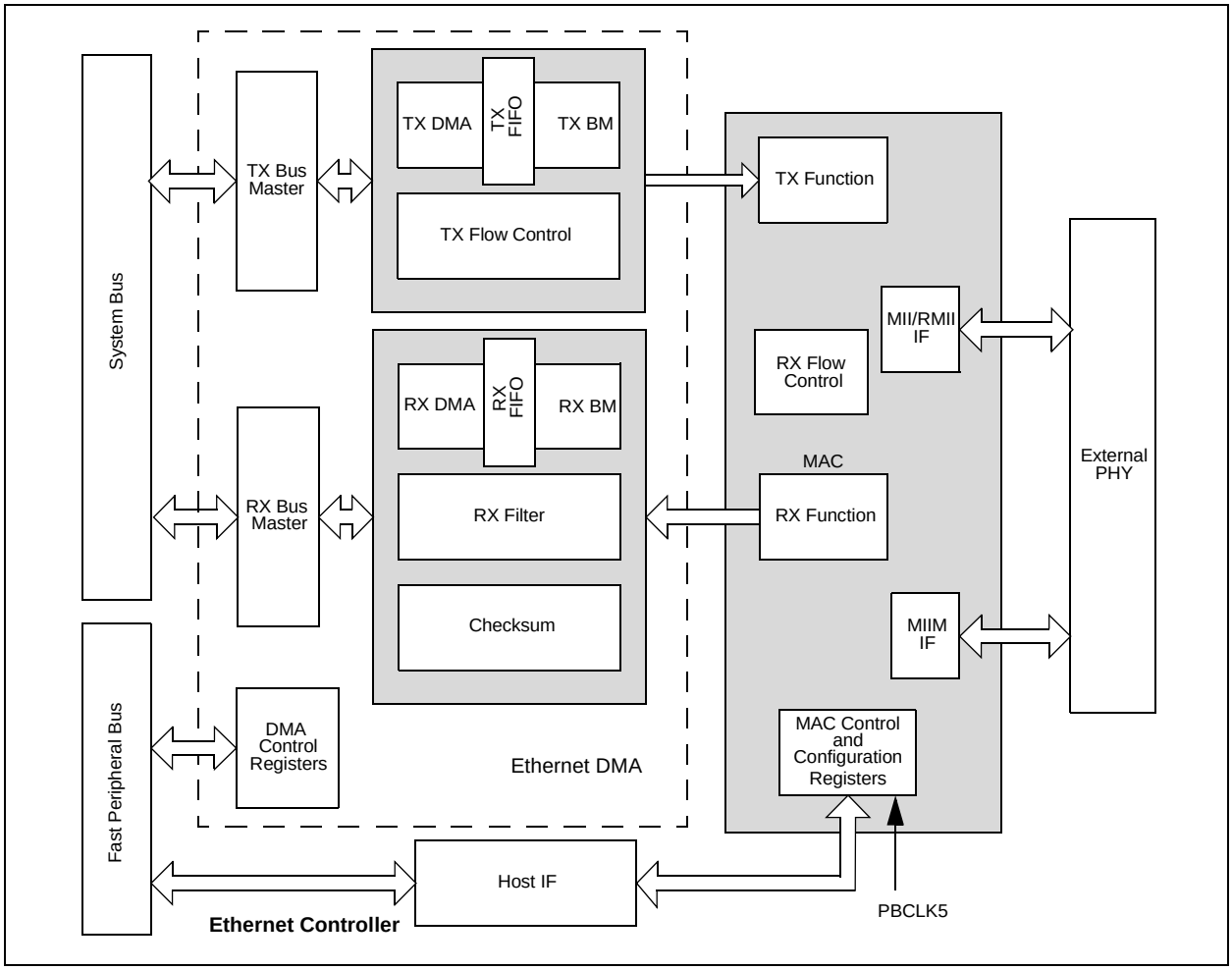
The Ethernet controller is a bus master module that interfaces with an off-chip Physical Layer (PHY) to implement a complete Ethernet node in a system.

Key features of the Ethernet Controller include:

- Supports 10/100 Mbps data transfer rates
- Supports full-duplex and half-duplex operation
- Supports RMII and MII PHY interface
- Supports MIIM PHY management interface
- Supports both manual and automatic Flow Control
- RAM descriptor-based DMA operation for both receive and transmit path
- Fully configurable interrupts
- Configurable receive packet filtering
  - CRC check
  - 64-byte pattern match
  - Broadcast, multicast and unicast packets
  - Magic Packet™
  - 64-bit hash table
  - Runt packet
- Supports packet payload checksum calculation
- Supports various hardware statistics counters

Figure 30-1 illustrates a block diagram of the Ethernet controller.

FIGURE 30-1: ETHERNET CONTROLLER BLOCK DIAGRAM



REGISTER 30-15: ETHSTAT: ETHERNET CONTROLLER STATUS REGISTER (CONTINUED)

bit 6 **TXBUSY:** Transmit Busy bit(2,6)

1 = TX logic is receiving data
0 = TX logic is idle

This bit indicates that a packet is currently being transmitted. A change in this status bit is not necessarily reflected by the TXDONE interrupt, as TX packets may be aborted or rejected by the MAC.

bit 5 **RXBUSY:** Receive Busy bit(3,6)

1 = RX logic is receiving data
0 = RX logic is idle

This bit indicates that a packet is currently being received. A change in this status bit is not necessarily reflected by the RXDONE interrupt, as RX packets may be aborted or rejected by the RX filter.

bit 4-0 **Unimplemented:** Read as '0'

Note 1: This bit is only used for RX operations.
2: This bit is only affected by TX operations.
3: This bit is only affected by RX operations.
4: This bit is affected by TX and RX operations.
5: This bit will be *set* when the ON bit (ETHCON1<15>) = 1.
6: This bit will be *cleared* when the ON bit (ETHCON1<15>) = 0.

REGISTER 30-19: ETHMCOLFRM: ETHERNET CONTROLLER MULTIPLE COLLISION FRAMES STATISTICS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	MCOLFRMCNT<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	MCOLFRMCNT<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **MCOLFRMCNT<15:0>:** Multiple Collision Frame Count bits

Increment count for frames that were successfully transmitted after there was more than one collision.

Note 1: This register is only used for TX operations.

2: This register is automatically cleared by hardware after a read operation, unless the byte enables for bytes 0/1 are '0'.

3: It is recommended to use the SET, CLR, or INV registers to set or clear any bit in this register. Setting or clearing any bits in this register should only be done for debug/test purposes.

REGISTER 30-28: EMAC1MAXF: ETHERNET CONTROLLER MAC MAXIMUM FRAME LENGTH REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-1
	MACMAXF<15:8>(1)							
7:0	R/W-1	R/W-1	R/W-1	R/W-0	R/W-1	R/W-1	R/W-1	R/W-0
	MACMAXF<7:0>(1)							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **MACMAXF<15:0>:** Maximum Frame Length bits(1)

These bits reset to 0x05EE, which represents a maximum receive frame of 1518 octets. An untagged maximum size Ethernet frame is 1518 octets. A tagged frame adds four octets for a total of 1522 octets. If a shorter/longer maximum length restriction is desired, program this 16-bit field.

Note 1: If a proprietary header is allowed, this bit should be adjusted accordingly. For example, if 4-byte headers are prepended to frames, MACMAXF could be set to 1527 octets. This would allow the maximum VLAN tagged frame plus the 4-byte header.

Note: Both 16-bit and 32-bit accesses are allowed to these registers (including the SET, CLR and INV registers). 8-bit accesses are not allowed and are ignored by the hardware.

TABLE A-1: OSCILLATOR CONFIGURATION DIFFERENCES (CONTINUED)

PIC32MX5XX/6XX/7XX Feature	PIC32MZ EF Feature
Crystal/Oscillator Selection for USB	
Any frequency that can be divided down to 4 MHz using UPLLIDIV, including 4, 8, 12, 16, 20, 40, and 48 MHz.	If the USB module is used, the Primary Oscillator is limited to either 12 MHz or 24 MHz. Which frequency is used is selected using the UPLLFSEL (DEVCFG2<30>) bit.
USB PLL Configuration	
On PIC32MX devices, the PLL for the USB requires an input frequency of 4 MHz. **UPLLIDIV<2:0> (DEVCFG2<10:8>)** **111 = 12x divider** **110 = 10x divider** **101 = 6x divider** **100 = 5x divider** **011 = 4x divider** **010 = 3x divider** **010 = 3x divider** **001 = 2x divider** **000 = 1x divider**	On PIC32MZ EF devices, the HS USB PHY requires an input frequency of 12 MHz or 24 MHz. UPLLIDIV has been replaced with UPLLFSEL. **UPLLFSEL (DEVCFG2<30>)** **1 = UPLL input clock is 24 MHz** **0 = UPLL input clock is 12 MHz**
Peripheral Bus Clock Configuration	
On PIC32MX devices, there is one peripheral bus, and the clock for that bus is divided from the SYSCLK using FPBDIV/PBDIV. In addition, the maximum PBCLK frequency is the same as SYSCLK. **FPBDIV<1:0> (DEVCFG1<5:4>)** PBDIV<**1**:0> (**OSCCON<20:19>**) **11 = PBCLK is SYSCLK divided by 8** **10 = PBCLK is SYSCLK divided by 4** **01 = PBCLK is SYSCLK divided by 2** **00 = PBCLK is SYSCLK divided by 1**	On PIC32MZ EF devices, there are eight peripheral buses with their own clocks. FPBDIV is removed, and each PBDIV is in its own register for each PBCLK. The initial PBCLK speed is fixed at reset, and the maximum PBCLK speed is limited to100 MHz for all buses, with the exception of PBCLK7, which is 200 MHz. PBDIV<**6**:0> (**PBxDIV**<**6**:0>) **1111111 = PBCLKx is SYSCLK divided by 128** **1111110 = PBCLKx is SYSCLK divided by 127** • • • **0000011 = PBCLKx is SYSCLK divided by 4** **0000010 = PBCLKx is SYSCLK divided by 3** **0000001 = PBCLKx is SYSCLK divided by 2** **(default value for x < 7)** **0000000 = PBCLKx is SYSCLK divided by 1** **(default value for x ≥ 7)**
CPU Clock Configuration	
On PIC32MX devices, the CPU clock is derived from SYSCLK.	On PIC32MZ EF devices, the CPU clock is derived from PBCLK7.
FRCDIV Default	
On PIC32MX devices, the default value for FRCDIV was to divide the FRC clock by two. FRCDIV<2:0> (OSCCON<26:24>) 111 = FRC divided by 256 110 = FRC divided by 64 101 = FRC divided by 32 100 = FRC divided by 16 011 = FRC divided by 8 010 = FRC divided by 4 001 = FRC divided by 2 **(default)** 000 = FRC divided by 1	On PIC32MZ EF devices, the default has been changed to divide by one. FRCDIV<2:0> (OSCCON<26:24>) 111 = FRC divided by 256 110 = FRC divided by 64 101 = FRC divided by 32 100 = FRC divided by 16 011 = FRC divided by 8 010 = FRC divided by 4 001 = FRC divided by 2 000 = FRC divided by 1 **(default)**

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