Microchip Technology - PIC32MZ2048EFM144-E/PL Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® M-Class
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, PMP, SPI, SQI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	120
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	2.1V ~ 3.6V
Data Converters	A/D 48x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mz2048efm144-e-pl

Referenced Sources

This device data sheet is based on the following individual sections of the *"PIC32 Family Reference Manual"*. These documents should be considered as the general reference for the operation of a particular module or device feature.

Note: To access the following documents, browse the documentation section of the Microchip web site (www.microchip.com).

- **Section 1. "Introduction"** (DS60001127)
- **Section 7. "Resets"** (DS60001118)
- **Section 8. "Interrupt Controller"** (DS60001108)
- **Section 9. "Watchdog, Deadman, and Power-up Timers"** (DS60001114)
- **Section 10. "Power-Saving Features"** (DS60001130)
- **Section 12. "I/O Ports"** (DS60001120)
- **Section 13. "Parallel Master Port (PMP)"** (DS60001128)
- **Section 14. "Timers"** (DS60001105)
- **Section 15. "Input Capture"** (DS60001122)
- **Section 16. "Output Compare"** (DS60001111)
- **Section 19. "Comparator"** (DS60001110)
- **Section 20. "Comparator Voltage Reference (CV_{REF})"** (DS60001109)
- **Section 21. "Universal Asynchronous Receiver Transmitter (UART)"** (DS60001107)
- **Section 22. "12-bit High-Speed Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC)"** (DS60001344)
- **Section 23. "Serial Peripheral Interface (SPI)"** (DS60001106)
- **Section 24. "Inter-Integrated Circuit (I^2C)"** (DS60001116)
- **Section 29. "Real-Time Clock and Calendar (RTCC)"** (DS60001125)
- **Section 31. "Direct Memory Access (DMA) Controller"** (DS60001117)
- **Section 32. "Configuration"** (DS60001124)
- **Section 33. "Programming and Diagnostics"** (DS60001129)
- **Section 34. "Controller Area Network (CAN)"** (DS60001154)
- **Section 35. "Ethernet Controller"** (DS60001155)
- **Section 41. "Prefetch Module for Devices with L1 CPU Cache"** (DS60001183)
- **Section 42. "Oscillators with Enhanced PLL"** (DS60001250)
- **Section 46. "Serial Quad Interface (SQI)"** (DS60001244)
- **Section 47. "External Bus Interface (EBI)"** (DS60001245)
- **Section 48. "Memory Organization and Permissions"** (DS60001214)
- **Section 49. "Crypto Engine (CE) and Random Number Generator (RNG)"** (DS60001246)
- **Section 50. "CPU for Devices with MIPS32® microAptiv™ and M-Class Cores"** (DS60001192)
- **Section 51. "Hi-Speed USB with On-The-Go (OTG)"** (DS60001326)
- **Section 52. "Flash Program Memory with Support for Live Update"** (DS60001193)

1.0 DEVICE OVERVIEW

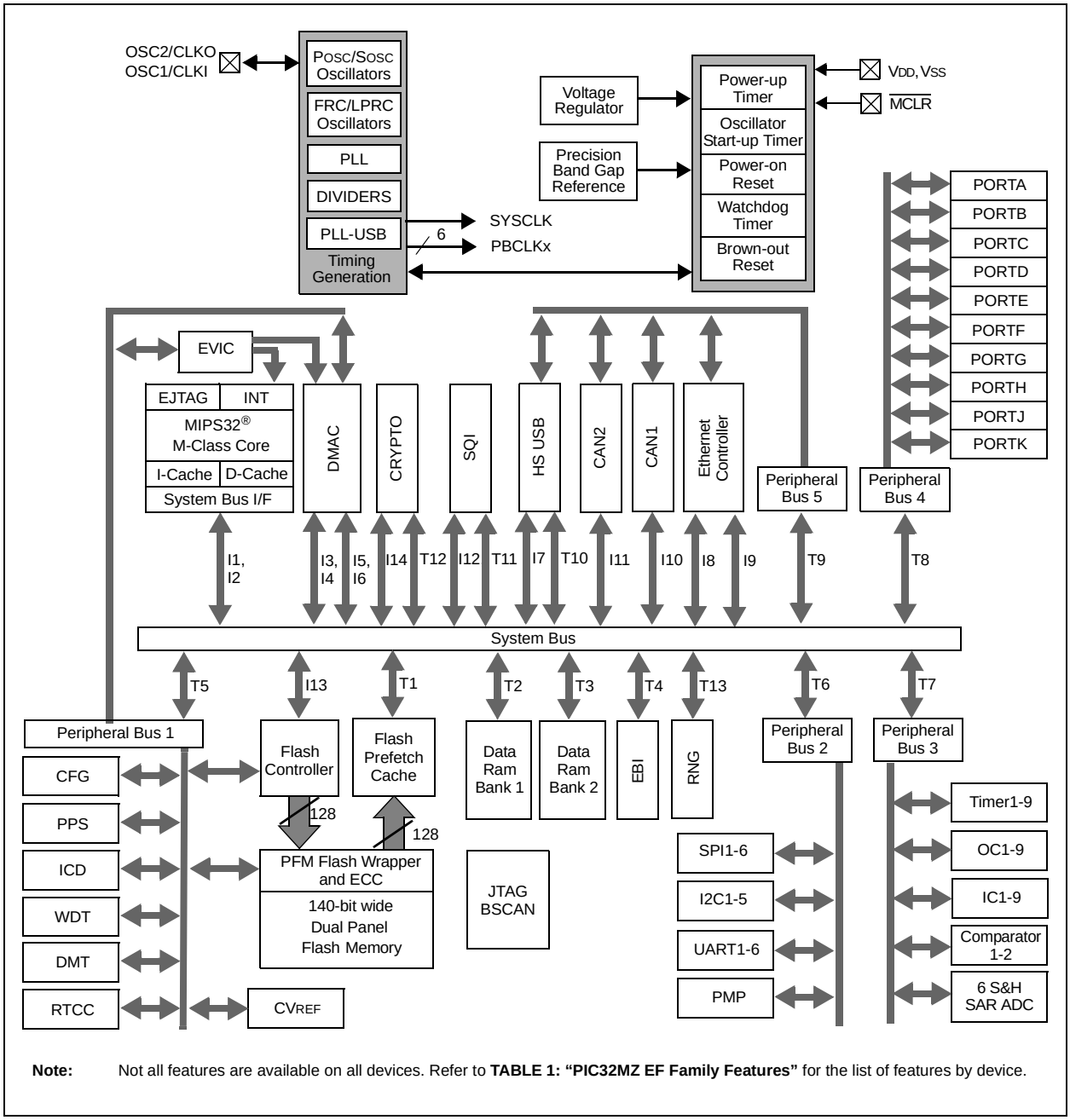
Note: This data sheet summarizes the features of the PIC32MZ EF family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

This data sheet contains device-specific information for PIC32MZ EF devices.

Figure 1-1 illustrates a general block diagram of the core and peripheral modules in the PIC32MZ EF family of devices.

Table 1-21 through Table 1-22 list the pinout I/O descriptions for the pins shown in the device pin tables (see Table 2 through Table 5).

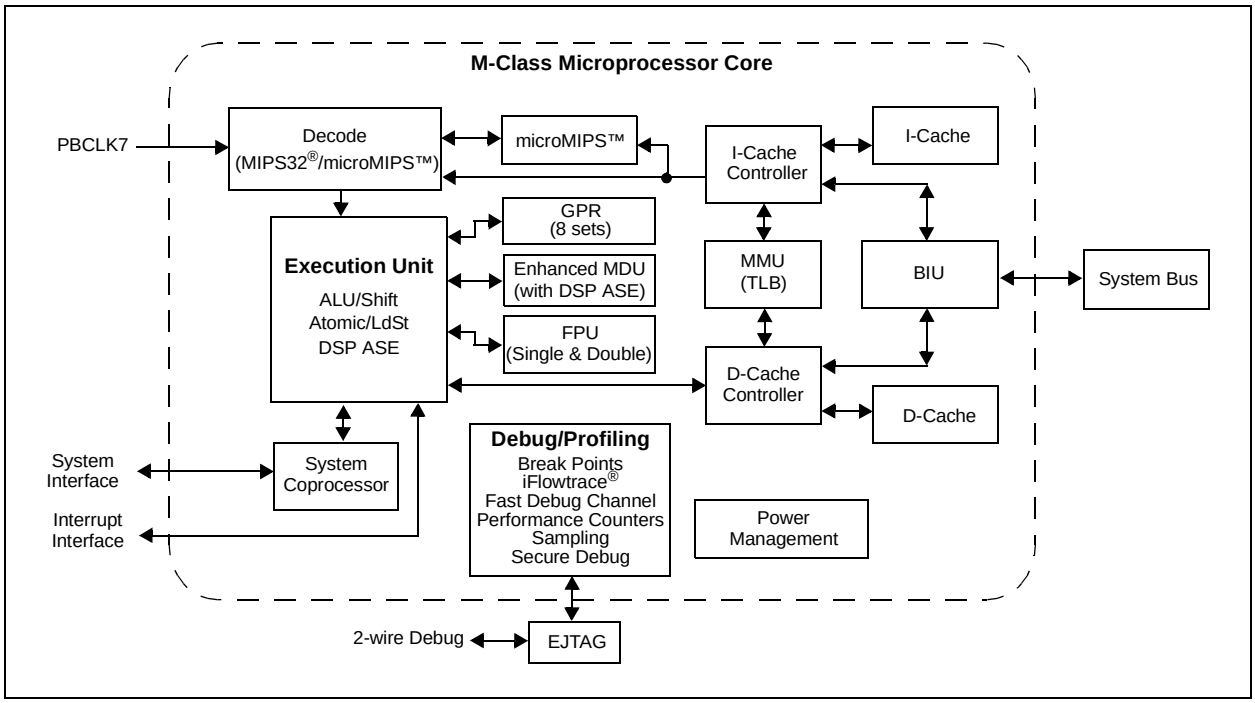
FIGURE 1-1: PIC32MZ EF FAMILY BLOCK DIAGRAM



Note: Not all features are available on all devices. Refer to **TABLE 1: "PIC32MZ EF Family Features"** for the list of features by device.

A block diagram of the PIC32MZ EF family processor core is shown in Figure 3-1.

FIGURE 3-1: PIC32MZ EF FAMILY MICROPROCESSOR CORE BLOCK DIAGRAM



8.2 Oscillator Control Registers

TABLE 8-2: OSCILLATOR CONFIGURATION REGISTER MAP

Virtual Address (BF80_#)	Register Name(1)	Bit Range	Bits																All Resets(2)
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
1200	OSCCON	31:16	—	—	—	—	—	FRCDIV<2:0>			DRMEN	—	SLP2SPD	—	—	—	—	—	0000
		15:0	—	COSC<2:0>			—	NOSC<2:0>			CLKLOCK	—	—	SLPEN	CF	—	SOSCEN	OSWEN	xx0x
1210	OSCTUN	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	TUN<5:0>						00xx
1220	SPLLCON	31:16	—	—	—	—	—	PLLODIV<2:0>			—	PLLMULT<6:0>								01xx
		15:0	—	—	—	—	—	PLLIDIV<2:0>			PLLICLK	—	—	—	—	PLLRANGE<2:0>			0x0x
1280	REFO1CON	31:16	—	RODIV<14:0>															0000
		15:0	ON	—	SIDL	OE	RSLP	—	DIVSWEN	ACTIVE	—	—	—	—	ROSEL<3:0>				0000
1290	REFO1TRIM	31:16	ROTRIM<8:0>									—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
12A0	REFO2CON	31:16	—	RODIV<14:0>															0000
		15:0	ON	—	SIDL	OE	RSLP	—	DIVSWEN	ACTIVE	—	—	—	—	ROSEL<3:0>				0000
12B0	REFO2TRIM	31:16	ROTRIM<8:0>									—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
12C0	REFO3CON	31:16	—	RODIV<14:0>															0000
		15:0	ON	—	SIDL	OE	RSLP	—	DIVSWEN	ACTIVE	—	—	—	—	ROSEL<3:0>				0000
12D0	REFO3TRIM	31:16	ROTRIM<8:0>									—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
12E0	REFO4CON	31:16	—	RODIV<14:0>															0000
		15:0	ON	—	SIDL	OE	RSLP	—	DIVSWEN	ACTIVE	—	—	—	—	ROSEL<3:0>				0000
12F0	REFO4TRIM	31:16	ROTRIM<8:0>									—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
1300	PB1DIV	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	PBDIVRDY	—	—	—	—	PBDIV<6:0>							8801
1310	PB2DIV	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	PBDIVRDY	—	—	—	—	PBDIV<6:0>							8801
1320	PB3DIV	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	PBDIVRDY	—	—	—	—	PBDIV<6:0>							8801
1330	PB4DIV	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	PBDIVRDY	—	—	—	—	PBDIV<6:0>							8801
1340	PB5DIV	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	PBDIVRDY	—	—	—	—	PBDIV<6:0>							8801

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 "CLR, SET, and INV Registers"** for more information.

2: Reset values are dependent on the DEVCFGx Configuration bits and the type of reset.

REGISTER 9-2: PRESTAT: PREFETCH MODULE STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	R/W-0, HS	R/W-0, HS	U-0	U-0
	—	—	—	—	PFMDED	PFMSEC	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0, HS	R/W-0, HS	R/W-0, HS	R/W-0, HS	R/W-0, HS	R/W-0, HS	R/W-0, HS	R/W-0, HS
	PFMSECCNT<7:0>							

Legend:		HS = Hardware Set	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-28 **Unimplemented:** Read as '0'

bit 27 **PFMDED:** Flash Double-bit Error Detected (DED) Status bit
This bit is set in hardware and can only be cleared (i.e., set to '0') in software.
1 = A DED error has occurred
0 = A DED error has not occurred

bit 26 **PFMSEC:** Flash Single-bit Error Corrected (SEC) Status bit
1 = A SEC error occurred when PFMSECCNT<7:0> was equal to zero
0 = A SEC error has not occurred

bit 25-8 **Unimplemented:** Read as '0'

bit 7-0 **PFMSECCNT<7:0>:** Flash SEC Count bits
11111111 - 00000000 = SEC count

REGISTER 15-4: DMTSTAT: DEADMAN TIMER STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R-0, HC, HS	R-0, HC, HS	R-0, HC, HS	U-0	U-0	U-0	U-0	R-0, HC, HS
	BAD1	BAD2	DMTEVENT	—	—	—	—	WINOPN

Legend:	HC = Hardware Cleared	HS = Hardware Set	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **BAD1:** Bad STEP1<7:0> Value Detect bit
- 1 = Incorrect STEP1<7:0> value was detected
- 0 = Incorrect STEP1<7:0> value was not detected

bit 6 **BAD2:** Bad STEP2<7:0> Value Detect bit
- 1 = Incorrect STEP2<7:0> value was detected
- 0 = Incorrect STEP2<7:0> value was not detected

bit 5 **DMTEVENT:** Deadman Timer Event bit
- 1 = Deadman timer event was detected (counter expired or bad STEP1<7:0> or STEP2<7:0> value was entered prior to counter increment)
- 0 = Deadman timer even was not detected

bit 4-1 **Unimplemented:** Read as '0'

bit 0 **WINOPN:** Deadman Timer Clear Window bit
- 1 = Deadman timer clear window is open
- 0 = Deadman timer clear window is not open

REGISTER 19-2: SPIxCON2: SPI CONTROL REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SPISGNEXT	—	—	FRMERREN	SPIROVEN	SPITUREN	IGNROV	IGNTUR
7:0	R/W-0	U-0	U-0	U-0	R/W-0	U-0	R/W-0	R/W-0
	AUDEN(1)	—	—	—	AUDMONO(1,2)	—	AUDMOD<1:0>(1,2)	

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **SPISGNEXT:** Sign Extend Read Data from the RX FIFO bit
- 1 = Data from RX FIFO is sign extended
- 0 = Data from RX FIFO is not sign extended

bit 14-13 **Unimplemented:** Read as '0'

bit 12 **FRMERREN:** Enable Interrupt Events via FRMERR bit
- 1 = Frame Error overflow generates error events
- 0 = Frame Error does not generate error events

bit 11 **SPIROVEN:** Enable Interrupt Events via SPIROV bit
- 1 = Receive overflow generates error events
- 0 = Receive overflow does not generate error events

bit 10 **SPITUREN:** Enable Interrupt Events via SPITUR bit
- 1 = Transmit Underrun Generates Error Events
- 0 = Transmit Underrun Does Not Generates Error Events

bit 9 **IGNROV:** Ignore Receive Overflow bit (for Audio Data Transmissions)
- 1 = A ROV is not a critical error; during ROV data in the FIFO is not overwritten by receive data
- 0 = A ROV is a critical error which stop SPI operation

bit 8 **IGNTUR:** Ignore Transmit Underrun bit (for Audio Data Transmissions)
- 1 = A TUR is not a critical error and zeros are transmitted until the SPIxTXB is not empty
- 0 = A TUR is a critical error which stop SPI operation

bit 7 **AUDEN:** Enable Audio CODEC Support bit(1)
- 1 = Audio protocol is enabled
- 0 = Audio protocol is disabled

bit 6-5 **Unimplemented:** Read as '0'

bit 3 **AUDMONO:** Transmit Audio Data Format bit(1,2)
- 1 = Audio data is mono (Each data word is transmitted on both left and right channels)
- 0 = Audio data is stereo

bit 2 **Unimplemented:** Read as '0'

bit 1-0 **AUDMOD<1:0>:** Audio Protocol Mode bit(1,2)
- 11 = PCM/DSP mode
- 10 = Right Justified mode
- 01 = Left Justified mode
- 00 = I^2S mode

Note 1: This bit can only be written when the ON bit = 0.

2: This bit is only valid for AUDEN = 1.

REGISTER 20-5: SQI1CLKCON: SQI CLOCK CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	CLKDIV<10:8>(1)		
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CLKDIV<7:0>(1)							
7:0	U-0	U-0	U-0	U-0	U-0	U-0	R-0	R/W-0
	—	—	—	—	—	—	STABLE	EN

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-19 **Unimplemented:** Read as '0'

bit 18-8 **CLKDIV<10:0>:** SQI Clock TSQI Frequency Select bit(1)

10000000000 = Base clock TBC is divided by 2048
01000000000 = Base clock TBC is divided by 1024
00100000000 = Base clock TBC is divided by 512
00010000000 = Base clock TBC is divided by 256
00001000000 = Base clock TBC is divided by 128
00000100000 = Base clock TBC is divided by 64
00000010000 = Base clock TBC is divided by 32
00000001000 = Base clock TBC is divided by 16
00000000100 = Base clock TBC is divided by 8
00000000010 = Base clock TBC is divided by 4
00000000001 = Base clock TBC is divided by 2
00000000000 = Base clock TBC

Setting these bits to '00000000000' specifies the highest frequency of the SQI clock.

bit 7-2 **Unimplemented:** Read as '0'

bit 1 **STABLE:** TSQI Clock Stable Select bit

This bit is set to '1' when the SQI clock, TSQI, is stable after writing a '1' to the EN bit.
1 = TSQI clock is stable
0 = TSQI clock is not stable

bit 0 **EN:** TSQI Clock Enable Select bit

When clock oscillation is stable, the SQI module will set the STABLE bit to '1'.
1 = Enable the SQI clock (TSQI) (when clock oscillation is stable, the SQI module sets the STABLE bit to '1')
0 = Disable the SQI clock (TSQI) (the SQI module should stop its clock to enter a low power state); SFRs can still be accessed, as they use PBCLK5

Note 1: Refer to Table 37-34 in **37.0 "Electrical Characteristics"** for the maximum clock frequency specifications.

REGISTER 25-6: ALRMDATE: ALARM DATE VALUE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	MONTH10<3:0>				MONTH01<3:0>			
15:8	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	DAY10<1:0>				DAY01<3:0>			
7:0	U-0	U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x
	—	—	—	—	WDAY01<3:0>			

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-24 **Unimplemented:** Read as '0'

bit 23-20 **MONTH10<3:0>:** Binary Coded Decimal value of months bits, 10 digits; contains a value from 0 to 1

bit 19-16 **MONTH01<3:0>:** Binary Coded Decimal value of months bits, 1 digit; contains a value from 0 to 9

bit 15-12 **DAY10<3:0>:** Binary Coded Decimal value of days bits, 10 digits; contains a value from 0 to 3

bit 11-8 **DAY01<3:0>:** Binary Coded Decimal value of days bits, 1 digit; contains a value from 0 to 9

bit 7-4 **Unimplemented:** Read as '0'

bit 3-0 **WDAY01<3:0>:** Binary Coded Decimal value of weekdays bits, 1 digit; contains a value from 0 to 6

27.1 RNG Control Registers

TABLE 27-2: RANDOM NUMBER GENERATOR (RNG) REGISTER MAP

Virtual Address (BF8E_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
6000	RNGVER	31:16	ID<15:0>																xxxx
		15:0	VERSION<7:0>								REVISION<7:0>								xxxx
6004	RNGCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	LOAD	TRNGMODE	CONT	PRNGEN	TRNGEN	PLEN<7:0>								0064
6008	RNGPOLY1	31:16	POLY<31:0>																FFFF
		15:0																	0000
600C	RNGPOLY2	31:16	POLY<31:0>																FFFF
		15:0																	0000
6010	RNGNUMGEN1	31:16	RNG<31:0>																FFFF
		15:0																	FFFF
6014	RNGNUMGEN2	31:16	RNG<31:0>																FFFF
		15:0																	FFFF
6018	RNGSEED1	31:16	SEED<31:0>																0000
		15:0																	0000
601C	RNGSEED2	31:16	SEED<31:0>																0000
		15:0																	0000
6020	RNGCNT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	RCNT<6:0>							0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

REGISTER 27-1: RNGVER: RANDOM NUMBER GENERATOR VERSION REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	ID<15:8>							
23:16	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	ID<7:0>							
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	VERSION<7:0>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	REVISION<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **ID<15:0>:** Block Identification bits

bit 15-8 **VERSION<7:0>:** Block Version bits

bit 7-0 **REVISION<7:0>:** Block Revision bits

REGISTER 28-6: ADCIMCON2: ADC INPUT MODE CONTROL REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DIFF31(1)	SIGN31(1)	DIFF30(1)	SIGN30(1)	DIFF29(1)	SIGN29(1)	DIFF28(1)	SIGN28(1)
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DIFF27(1)	SIGN27(1)	DIFF26(1)	SIGN26(1)	DIFF25(1)	SIGN25(1)	DIFF24(1)	SIGN24(1)
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DIFF23(1)	SIGN23(1)	DIFF22(1)	SIGN22(1)	DIFF21(1)	SIGN21(1)	DIFF20(1)	SIGN20(1)
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DIFF19(1)	SIGN19(1)	DIFF18	SIGN18	DIFF17	SIGN17	DIFF16	SIGN16

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **DIFF31:** AN31 Mode bit(1)
1 = AN31 is using Differential mode
0 = AN31 is using Single-ended mode

bit 30 **SIGN31:** AN31 Signed Data Mode bit(1)
1 = AN31 is using Signed Data mode
0 = AN31 is using Unsigned Data mode

bit 29 **DIFF30:** AN30 Mode bit(1)
1 = AN30 is using Differential mode
0 = AN30 is using Single-ended mode

bit 28 **SIGN30:** AN30 Signed Data Mode bit(1)
1 = AN30 is using Signed Data mode
0 = AN30 is using Unsigned Data mode

bit 27 **DIFF29:** AN29 Mode bit(1)
1 = AN29 is using Differential mode
0 = AN29 is using Single-ended mode

bit 26 **SIGN29:** AN29 Signed Data Mode bit(1)
1 = AN29 is using Signed Data mode
0 = AN29 is using Unsigned Data mode

bit 25 **DIFF28:** AN28 Mode bit(1)
1 = AN28 is using Differential mode
0 = AN28 is using Single-ended mode

bit 24 **SIGN28:** AN28 Signed Data Mode bit(1)
1 = AN28 is using Signed Data mode
0 = AN28 is using Unsigned Data mode

bit 23 **DIFF27:** AN27 Mode bit(1)
1 = AN27 is using Differential mode
0 = AN27 is using Single-ended mode

bit 22 **SIGN27:** AN27 Signed Data Mode bit(1)
1 = AN27 is using Signed Data mode
0 = AN27 is using Unsigned Data mode

Note 1: This bit is not available on 64-pin devices.

REGISTER 28-34: ADCSYSCFG1: ADC SYSTEM CONFIGURATION REGISTER 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-y	R-y	R-y	R-y	R-y	R-y	R-y	R-y
	AN<31:23>							
23:16	R-y	R-y	R-y	R-y	R-y	R-1	R-1	R-1
	AN<23:16>							
15:8	R-1	R-1	R-1	R-1	R-1	R-1	R-1	R-1
	AN<15:8>							
7:0	R-1	R-1	R-1	R-1	R-1	R-1	R-1	R-1
	AN<7:0>							

Legend:		y = POR value is determined by the specific device	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **AN<31:0>:** ADC Analog Input bits

These bits reflect the system configuration and are updated during boot-up time. By reading these read-only bits, the user application can determine whether or not an analog input in the device is available.

AN<31:0>: Reflects the presence or absence of the respective analog input (AN31-AN0).

REGISTER 28-35: ADCSYSCFG2: ADC SYSTEM CONFIGURATION REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	R-1	R-1	R-y	R-y	R-y
	—	—	—	AN<44:40>				
7:0	R-y	R-y	R-y	R-y	R-y	R-y	R-y	R-y
	AN<39:32>							

Legend:		y = POR value is determined by the specific device	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-13 **Unimplemented:** Read as '0'

bit 12-0 **AN<44:32>:** ADC Analog Input bits

These bits reflect the system configuration and are updated during boot-up time. By reading these read-only bits, the user application can determine whether or not an analog input in the device is available.

AN<63:32>: Reflects the presence or absence of the respective analog input (AN63-AN32).

REGISTER 30-3: ETHTXST: ETHERNET CONTROLLER TX PACKET DESCRIPTOR START ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	TXSTADDR<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	TXSTADDR<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	TXSTADDR<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0
	TXSTADDR<7:2>						—	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-2 **TXSTADDR<31:2>:** Starting Address of First Transmit Descriptor bits
This register should not be written while any transmit, receive or DMA operations are in progress.
This address must be 4-byte aligned (bits 1-0 must be '00').

bit 1-0 **Unimplemented:** Read as '0'

Note 1: This register is only used for TX operations.
2: This register will be updated by hardware with the last descriptor used by the last successfully transmitted packet.

REGISTER 30-4: ETHRXST: ETHERNET CONTROLLER RX PACKET DESCRIPTOR START ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RXSTADDR<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RXSTADDR<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RXSTADDR<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0
	RXSTADDR<7:2>						—	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-2 **RXSTADDR<31:2>:** Starting Address of First Receive Descriptor bits
This register should not be written while any transmit, receive or DMA operations are in progress.
This address must be 4-byte aligned (bits 1-0 must be '00').

bit 1-0 **Unimplemented:** Read as '0'

Note 1: This register is only used for RX operations.
2: This register will be updated by hardware with the last descriptor used by the last successfully transmitted packet.

32.1 Comparator Voltage Reference Control Registers

TABLE 32-1: COMPARATOR VOLTAGE REFERENCE REGISTER MAP

Virtual Address (BF80_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0E00	CVRCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	—	—	—	—	—	CVROE	CVRR	CVRSS	CVR<3:0>				0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: The register in this table has corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.3 "CLR, SET, and INV Registers"** for more information.

REGISTER 34-7: CFGCON: CONFIGURATION CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
	—	—	—	—	—	—	DMAPRI(1)	CPUPRI(1)
23:16	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
	—	—	—	—	—	—	ICACLK(1)	OCACLK(1)
15:8	U-0	U-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0
	—	—	IOLOCK(1)	PMDLOCK(1)	PGLOCK(1)	—	—	USBSSEN(1)
7:0	R/W-0	U-0	R/W-1	R/W-1	R/W-1	R/W-0	U-0	R/W-1
	IOANCPEN	—	ECCCON<1:0>		JTAGEN	TROEN	—	TDOEN

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-26 **Unimplemented:** Read as '0'

bit 25 **DMAPRI:** DMA Read and DMA Write Arbitration Priority to SRAM bit(1)
- 1 = DMA gets High Priority access to SRAM
- 0 = DMA uses Least Recently Serviced Arbitration (same as other initiators)

bit 24 **CPUPRI:** CPU Arbitration Priority to SRAM When Servicing an Interrupt bit(1)
- 1 = CPU gets High Priority access to SRAM
- 0 = CPU uses Least Recently Serviced Arbitration (same as other initiators)

bit 23-18 **Unimplemented:** Read as '0'

bit 17 **ICACLK:** Input Capture Alternate Clock Selection bit(1)
- 1 = Input Capture modules use an alternative Timer pair as their timebase clock
- 0 = All Input Capture modules use Timer2/3 as their timebase clock

bit 16 **OCACLK:** Output Compare Alternate Clock Selection bit(1)
- 1 = Output Compare modules use an alternative Timer pair as their timebase clock
- 0 = All Output Compare modules use Timer2/3 as their timebase clock

bit 15-14 **Unimplemented:** Read as '0'

bit 13 **IOLOCK:** Peripheral Pin Select Lock bit(1)
- 1 = Peripheral Pin Select is locked. Writes to PPS registers are not allowed
- 0 = Peripheral Pin Select is not locked. Writes to PPS registers are allowed

bit 12 **PMDLOCK:** Peripheral Module Disable bit(1)
- 1 = Peripheral module is locked. Writes to PMD registers are not allowed
- 0 = Peripheral module is not locked. Writes to PMD registers are allowed

bit 11 **PGLOCK:** Permission Group Lock bit(1)
- 1 = Permission Group registers are locked. Writes to PG registers are not allowed
- 0 = Permission Group registers are not locked. Writes to PG registers are allowed

bit 10-9 **Unimplemented:** Read as '0'

bit 8 **USBSSEN:** USB Suspend Sleep Enable bit(1)

Enables features for USB PHY clock shutdown in Sleep mode.
- 1 = USB PHY clock is shut down when Sleep mode is active
- 0 = USB PHY clock continues to run when Sleep is active

Note 1: To change this bit, the unlock sequence must be performed. Refer to **Section 42. "Oscillators with Enhanced PLL"** (DS60001250) in the *"PIC32 Family Reference Manual"* for details.

37.2 AC Characteristics and Timing Parameters

The information contained in this section defines PIC32MZ EF device AC characteristics and timing parameters.

FIGURE 37-1: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS

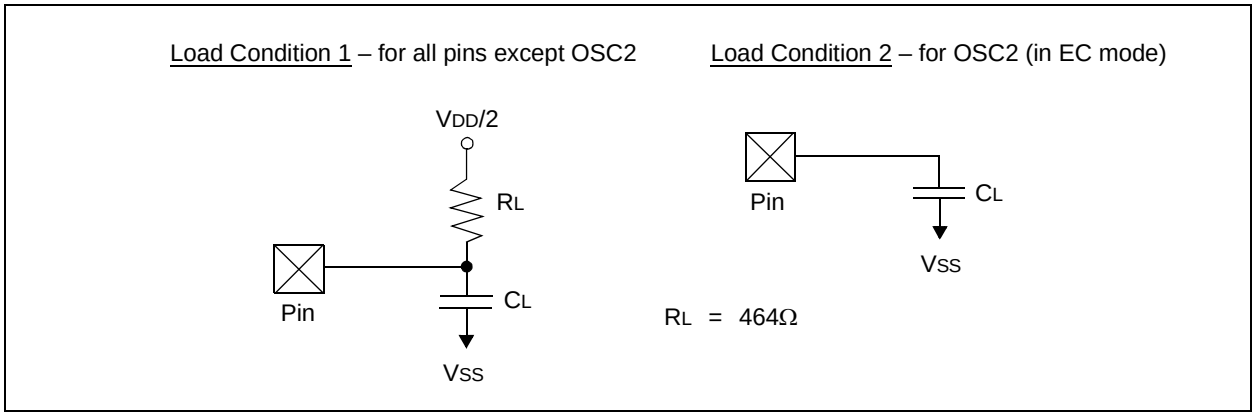


TABLE 37-16: CAPACITIVE LOADING REQUIREMENTS ON OUTPUT PINS

AC CHARACTERISTICS			Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Symbol**	**Characteristics**	**Min.**	**Typical(1)**	**Max.**	**Units**	**Conditions**
DO56	CL	All I/O pins (except pins used as CxOUT)	—	—	50	pF	EC mode for OSC2
DO58	CB	SCLx, SDAx	—	—	400	pF	In I^2C mode
DO59	CSQI	All SQI pins	—	—	10	pF	—

Note 1: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

TABLE 38-3: DC CHARACTERISTICS: IDLE CURRENT (IIDLE)

DC CHARACTERISTICS			Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +125°C for Extended	
Parameter No.	**Typical(2)**	**Maximum(4)**	**Units**	**Conditions**
Idle Current (IIDLE): Core Off, Clock on Base Current (Note 1)				
EDC30a	7	52	mA	4 MHz **(Note 3)**
EDC31a	8	56	mA	10 MHz
EDC32a	13	66	mA	60 MHz **(Note 3)**
EDC33a	21	86	mA	130 MHz **(Note 3)**
EDC34	26	96	mA	180 MHz **(Note 3)**

Note 1: The test conditions for IIDLE current measurements are as follows:

- Oscillator mode is EC+PLL with OSC1 driven by external square wave from rail-to-rail, (OSC1 input clock input over/undershoot < 100 mV required)
- OSC2/CLKO is configured as an I/O input pin
- USB PLL is disabled (USBPMD = 1), VUSB3V3 is connected to VSS, PBCLKx divisor = 1:128 ('x' ≠ 7)
- CPU is in Idle mode (CPU core Halted)
- L1 Cache and Prefetch modules are disabled
- No peripheral modules are operating, (ON bit = 0), but the associated PMD bit is cleared (except USBPMD)
- WDT, DMT, Clock Switching, Fail-Safe Clock Monitor, and Secondary Oscillator are disabled
- All I/O pins are configured as inputs and pulled to VSS
- $\overline{\text{MCLR}}$ = VDD
- RTCC and JTAG are disabled

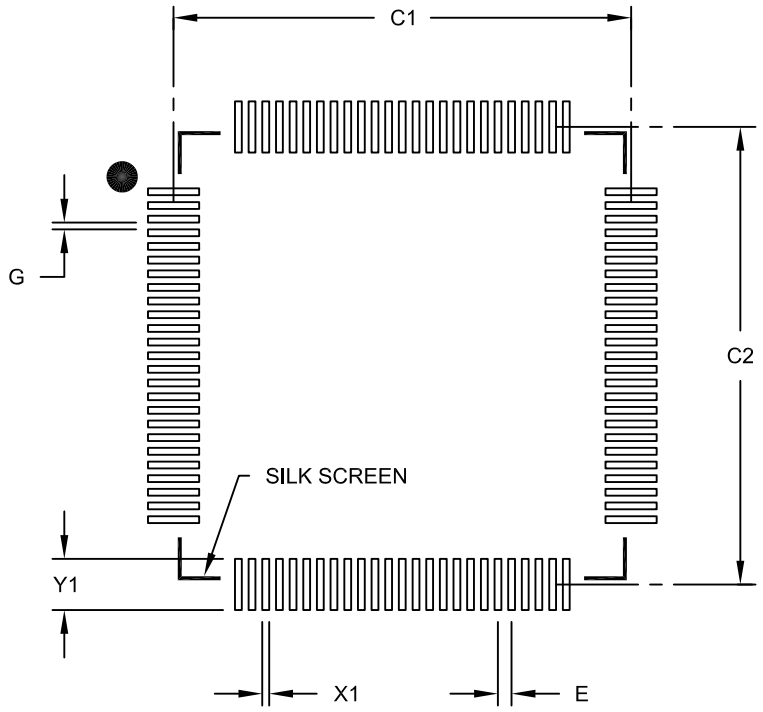
2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: This parameter is characterized, but not tested in manufacturing.

4: Data in the "Maximum" column is at 3.3V, +125ºC at specified operating frequency. Parameters are for design guidance only and are not tested.

100-Lead Plastic Thin Quad Flatpack (PT)-12x12x1mm Body, 2.00 mm Footprint [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.40 BSC	
Contact Pad Spacing	C1		13.40	
Contact Pad Spacing	C2		13.40	
Contact Pad Width (X100)	X1			0.20
Contact Pad Length (X100)	Y1			1.50
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2100B

TABLE A-3: ADC DIFFERENCES (CONTINUED)

PIC32MX5XX/6XX/7XX Feature	PIC32MZ EF Feature
Scan Trigger Source	
On PIC32MX devices, there are four sources that can trigger a scan conversion in the ADC module: Auto, Timer3, INT0, and clearing the SAMP bit. SSRC<2:0> (AD1CON1<7:5>) 111 = Auto convert 110 = Reserved 101 = Reserved 100 = Reserved 011 = Reserved 010 = Timer3 period match 001 = Active transition on INT0 pin 000 = Clearing SAMP bit	On PIC32MZ EF devices, the list of sources for triggering a scan conversion has been expanded to include the comparators, Output Compare, and two additional Timers. In addition, trigger sources can be simulated by setting the RQCNVRT (ADCCON3<8>) bit. STRGSRC<4:0> (ADCCON1<20:16>) 11111 = Reserved • • • 01101 = Reserved 01100 = Comparator 2 COUT 01011 = Comparator 1 COUT 01010 = OCMP5 01001 = OCMP3 01000 = OCMP1 00111 = TMR5 match 00110 = TMR3 match 00101 = TMR1 match 00100 = INT0 00011 = Reserved 00010 = Global level software trigger (GLSWTRG) 00001 = Global software trigger (GSWTRG) 00000 = No trigger
Output Format	
On PIC32MX devices, the output format was decided for all ADC channels based on the setting of the FORM<2:0> bits. FORM<2:0> (AD1CON1<10:8>) 011 = Signed Fractional 16-bit 010 = Fractional 16-bit 001 = Signed Integer 16-bit 000 = Integer 16-bit 111 = Signed Fractional 32-bit 110 = Fractional 32-bit 101 = Signed Integer 32-bit 100 = Integer 32-bit	On PIC32MZ EF devices, the FRACT bit determines whether fractional or integer format is used. Then, each input can have its own setting for input (differential or single-ended) and sign (signed or unsigned) using the DIFFx and SIGNx bits in the ADCIMODx registers. FRACT (ADCCON1<23>) 1 = Fractional 0 = Integer DIFFx (ADCIMODy) 1 = Channel x is using Differential mode 0 = Channel x is using Single-ended mode SIGNx (ADCMODy) 1 = Channel x is using Signed Data mode 0 = Channel x is using Unsigned Data mode
Interrupts	
On PIC32MX devices, an interrupt is triggered from the ADC module when a certain number of conversions have taken place, irrespective of which channel was converted. SMPI<3:0> (AD1CON2<5:2>) 1111 = Interrupt for each 16th sample/convert sequence 1110 = Interrupt for each 15th sample/convert sequence • • • 0001 = Interrupt for each 2nd sample/convert sequence 0000 = Interrupt for each sample/convert sequence	On PIC32MZ EF devices, the ADC module can trigger an interrupt for each channel when it is converted. Use the Interrupt Controller bits, IEC1<31:27>, IEC2<31:0>, and IEC3<7:0>, to enable/disable them. In addition, the ADC support one global interrupt to indicate conversion on any number of channels. AGIENxx (ADCGIRQENx<y>) 1 = Data ready event will generate a Global ADC interrupt 0 = No global interrupt In addition, interrupts can be generated for filter and comparator events.