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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

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Product Status	Active
Core Processor	MIPS32® M-Class
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, PMP, SPI, SQI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	120
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	2.1V ~ 3.6V
Data Converters	A/D 48x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mz2048efm144-i-pl

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TABLE 4:PIN NAMES FOR 124-PIN DEVICES

124	-PIN VTLA (BOTTOM VIEW) A1	7		213	A34 B29	
	PIC32MZ0512EF(E/F/K)124 PIC32MZ1024EF(G/H/M)124 PIC32MZ1024EF(E/F/K)124 PIC32MZ2048EF(G/H/M)124			B1 E	B41 56	A51
	Polarity	Indica	A1 tor	A	68	
Package Pin #	Full Pin Name		Package Pin #		Full Pin Name	
A1	No Connect	_	A35	VBUS		
A2	AN23/RG15		A36	VUSB3	/3	
Δ3	EBID5/AN17/RPE5/PMD5/RE5		Δ37	D-		
A4	EBID7/AN15/PMD7/RE7		A38	RPF3/	USBID/RE3	
A5			A39	FBIRE	Y2/RPF8/SCI 3/RF8	
A6	FBIA12/AN21/RPC2/PMA12/RC2		A40	FRXD	3/RH9	
Δ7			Δ41	EBICS	0/SCI 2/RA2	
A8	EBIA4/AN13/C1INC/RPG7/SDA4/PMA4/RG7		A42	FBIA1	4/PMCS1/PMA14/RA4	
A9	Vss		A43	Vss		
A10	MCLR		A44	EBIA8	/RPF5/SCL5/PMA8/RF5	
A11	TMS/EBIA16/AN24/RA0		A45	RPA1	5/SDA1/RA15	
A12	AN26/RPE9/RE9		A46	RPD1	D/SCK4/RD10	
A13	AN4/C1INB/RB4		A47	ECRS	/RH12	
A14	AN3/C2INA/RPB3/RB3		A48	RPD0	RTCC/INT0/RD0	
A15	Vdd		A49	SOSC	O/RPC14/T1CK/RC14	
A16	AN2/C2INB/RPB2/RB2		A50	Vdd		
A17	PGEC1/AN1/RPB1/RB1		A51	Vss		
A18	PGED1/AN0/RPB0/RB0		A52	RPD1	SCK1/RD1	
A19	PGED2/AN47/RPB7/RB7		A53	EBID1	5/RPD3/PMD15/RD3	
A20	VREF+/CVREF+/AN28/RA10		A54	EBID1	3/PMD13/RD13	
A21	AVss		A55	EMDIO	D/RJ1	
A22	AN39/ETXD3/RH1		A56	SQICS	60/RPD4/RD4	
A23	EBIA7/AN49/RPB9/PMA7/RB9		A57	ETXE	N/RPD6/RD6	
A24	AN6/RB11		A58	Vdd		
A25	Vdd		A59	EBID1	1/RPF0/PMD11/RF0	
A26	TDI/EBIA18/AN30/RPF13/SCK5/RF13		A60	EBID	/RPG1/PMD9/RG1	
A27	EBIA11/AN7/PMA11/RB12		A61	TRCL	K/SQICLK/RA6	
A28	EBIA1/AN9/RPB14/SCK3/PMA1/RB14		A62	RJ4		
A29	Vss		A63	Vss		
A30	AN40/ERXERR/RH4		A64	EBID1	/PMD1/RE1	
A31	AN42/ERXD2/RH6		A65	TRD1/	SQID1/RG12	
A32	AN33/RPD15/SCK6/RD15		A66	EBID2	/SQID2/PMD2/RE2	
A33	OSC2/CLKO/RC15		A67	EBID4	/AN18/PMD4/RE4	
A34	No Connect		A68	No Co	nnect	

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and Section 12.4 "Peripheral Pin Select (PPS)" for restrictions.

2: Every I/O port pin (RAx-RJx) can be used as a change notification pin (CNAx-CNJx). See Section 12.0 "I/O Ports" for more information.

3: Shaded pins are 5V tolerant.

4: The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to Vss externally.

		Pin Nu	mber				
Pin Name	64-pin QFN/ TQFP	100-pin TQFP	124-pin VTLA	144-pin TQFP/ LQFP	Pin Type	Buffer Type	Description
AN0	16	25	A18	36	I	Analog	Analog Input Channels
AN1	15	24	A17	35	I	Analog	
AN2	14	23	A16	34	I	Analog	
AN3	13	22	A14	31	I	Analog	
AN4	12	21	A13	26	I	Analog	
AN5	23	34	B19	49	I	Analog	
AN6	24	35	A24	50	I	Analog	
AN7	27	41	A27	59	I	Analog	
AN8	28	42	B23	60	I	Analog	
AN9	29	43	A28	61	I	Analog	
AN10	30	44	B24	62	I	Analog	
AN11	10	16	B9	21	I	Analog	
AN12	6	12	B7	16	I	Analog	
AN13	5	11	A8	15	I	Analog	
AN14	4	10	B6	14	I	Analog	
AN15	3	5	A4	5	I	Analog	
AN16	2	4	B2	4	I	Analog	
AN17	1	3	A3	3	I	Analog	
AN18	64	100	A67	144	I	Analog	
AN19	—	9	A7	13	I	Analog	
AN20	—	8	B5	12	I	Analog	
AN21	—	7	A6	11	I	Analog	
AN22	—	6	B3	6	I	Analog	
AN23	—	1	A2	1	I	Analog	
AN24	—	17	A11	22	I	Analog	
AN25	—	18	B10	23	I	Analog	
AN26	—	19	A12	24	I	Analog	
AN27	—	28	B15	39	I	Analog	
AN28	—	29	A20	40	I	Analog	
AN29	—	38	B21	56	I	Analog	
AN30	—	39	A26	57	I	Analog	
AN31	—	40	B22	58	I	Analog	
AN32	—	47	B27	69	I	Analog	
AN33	—	48	A32	70	Ι	Analog	
AN34	_	2	B1	2	Ι	Analog	
AN35	_	_	A5	7	Ι	Analog	
Legend:	CMOS = C	MOS-comp	atible input	t or output		Analog =	Analog input P = Power

TABLE 1-1: ADC PINOUT I/O DESCRIPTIONS

egend: CMOS = CMOS-compatible input or output ST = Schmitt Trigger input with CMOS levels TTL = Transistor-transistor Logic input buffer

Analog = Analog input O = Output PPS = Peripheral Pin Select

I = Input

TABLE 7-3: INTERRUPT REGISTER MAP (CONTINUED)

Perform Perform <t< th=""><th>ress !)</th><th></th><th>е</th><th></th><th></th><th></th><th></th><th></th><th></th><th></th><th>B</th><th>its</th><th></th><th></th><th></th><th></th><th></th><th></th><th></th><th>s</th></t<>	ress !)		е								B	its								s
0760 0F113 11.6 - 0 0000 0	Virtual Add (BF81 #	Registel Name ⁽¹⁾	Bit Rang	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Reset
01000 01710 150	0700	055400	31:16		_	_	—	_	—	—	_	—	_	_	_	_	_	VOFF<	17:16>	0000
<table-container>And and and any any angle of any any angle of any any any any angle of any any angle of any</table-container>	0768	OFF138	15:0								VOFF<15:1>								-	0000
0000 01130 150 - 00000 0000 0000 <	0760	OEE130	31:16		_	—		—	—	—	—	—	_	_	—	—	—	VOFF<	17:16>	0000
Prime Prime <	0700	011139	15:0			-					VOFF<15:1>									0000
No. 0000 model 10.0 mode	0770	OFF140	31:16	_	—	—	—	—	—	—	—	—	—	—	—	—	—	VOFF<	17:16>	0000
0774 0F140 116 - - - - - - - - - 000 0000 0778 0F142 116 - - - - - - - - 000 0000 0778 0F143 116 - - - - - - - - 000 0770 0F143 116 - - - - - - - 000 0771 06143 116 - - - - - - - 0000 0771 0771 116 - - - - - - - 0000 0772 0771 116 - - - - - - - 0000 0773 0771 116 - - - - - - - 0000 0000 0780 07714 116 - - - - - - - - 0000 0780 0714 116 - - - - - - - - -	00	0	15:0								VOFF<15:1>							1	—	0000
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0778 0FF12 1.16 - - - - - - - - - - - 000 0770 0FF13 15.0 - - - - - - - - 070 0710 0771 0F13 15.0 - - - - - - - - 070 070 0780 0F143 15.0 - - - - - - - - 070 070 0781 15.0 - - - - - - - - - 070 070 0783 0F143 116 - - - - - - - - 070 070 0784 0F145 15.0 - - - - - - - 070 070 0714 15.0 070 - - - - 070 070 0714 15.0 - - - - - - 070 070 0714 15.1 - - - - - - - 070 070		-	15:0			-		-			VOFF<15:1>				r	r		1	—	0000
Normal Alian	0778	OFF142	31:16	_		—		—			—	—			—	—	—	VOFF<	17:16>	0000
0770 0FF143 116 - - - - - - - - 000 0780 0FF143 116 - - - - - - - - 000 0780 0FF144 15.0 - - - - - - - - - 000 0780 0FF145 15.0 - - - - - - - - 000 0780 0FF146 15.0 - - - - - - - - 000 0780 0FF146 15.0 - - - - - - - - 000 0780 0FF146 15.0 - - - - - - - - 000 0780 0FF146 15.0 - - - - - - - - 000 0780 0FF147 15.0 - - - - - - - - 000 0790 0FF149(* 15.0 - - - - - -			15:0		i	1	i	1	i	i	VOFF<15:1>	I	i	i			1		—	0000
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0780 0FF144 1:10 - - - - - - - - - - - - 000 0784 0FF145 31:6 - - - - - - - - - 000 0788 0FF145 31:6 - - - - - - - - 000 0788 0FF146 31:6 - - - - - - - - 000 0788 0FF147 31:6 - - - - - - - - 000 0788 0FF147 31:6 - - - - - - - - 000 0786 0FF147 31:6 - - - - - - - - - 000 0787 0FF1478 31:16 - - - - - - - - 000 0790 0FF148(2) 31:16 - - - - - - - - 000 0798 0FF149(2) 31:16 -			15:0								VOFF<15:1>	•							-	0000
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0FF146 1.10			15.0								VUFF<15.1>	•						VOEE	17:16	0000
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0788 0Ff146 0780 0Ff146 0780 0780 0Ff147 15.0 0000 0780 0Ff147 13.16 - - - - - - 0000 0780 0Ff147 13.16 - - - - - - - 0000 0780 0Ff147 13.16 - - - - - - - 0000 0780 0Ff148(2) 13.16 - - - - - - - 0000 0790 0Ff149(2) 13.16 - - - - - - - 0000 0791 0Ff10(2) 13.16 - - - - - - - 0000 0792 0Ff15(2) 13.16 - - - - - - - 0000 0793 0Ff15(2) 13.16 - - - - - - - 0000 0794 0Ff15(2) 13.16 - - - - - - - - 0000 0795 0Ff15(2) 13.16 - - </td <td></td> <td></td> <td>31.16</td> <td>_</td> <td></td> <td>_</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>_</td> <td>_</td> <td></td> <td>VOFE</td> <td>17:16></td> <td>0000</td>			31.16	_		_									_	_		VOFE	17:16>	0000
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0/30 0/11/01/12 15:0 - 0000 07A0 0FF152(3) 31:16 - - - - - 0000 07A0 0FF152(3) 31:16 - - - - - - 0000 07A0 0FF152(3) 31:16 - - - - - - 0000 07A0 0FF152(3) 15:0 VOFF VOFF - 0000	0700	OFE151(3)	31:16	_	_	—		—	_	_	—	—	_	_	—	—	—	VOFF<	17:16>	0000
07A0 OFF152 ⁽³⁾ 31:16 VOFF<17:16> 0000 15:0 VOFF<15:1> - 0000	0190	011101.7	15:0								VOFF<15:1>								_	0000
VOFF<15:1>0000	0740	OFF152(3)	31:16	_	_	-	_	-	_	_	-		_	_			-	VOFF<	17:16>	0000
	UTAC	011102	15:0								VOFF<15:1>	•							—	0000

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x = unknown value on Reset; --- = unimplemented, read as '0'. Reset values are shown in hexadecimal.

All registers in this table with the exception of the OFFx registers, have corresponding CLR, SET, and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 12.3 "CLR, SET, and INV Note 1: **Registers**" for more information. This bit or register is not available on 64-pin devices.

2:

3: This bit or register is not available on devices without a CAN module.

4: This bit or register is not available on 100-pin devices.

5: Bits 31 and 30 are not available on 64-pin and 100-pin devices; bits 29 through 14 are not available on 64-pin devices.

6: Bits 31, 30, 29, and bits 5 through 0 are not available on 64-pin and 100-pin devices; bit 31 is not available on 124-pin devices; bit 22 is not available on 64-pin devices.

7: This bit or register is not available on devices without a Crypto module.

This bit or register is not available on 124-pin devices. 8:

8.0 OSCILLATOR CONFIGURATION

Note:	This data sheet summarizes the
	features of the PIC32MZ EF family of
	devices. It is not intended to be a
	comprehensive reference source. To
	complement the information in this data
	sheet, refer to Section 42. "Oscillators
	with Enhanced PLL" (DS60001250) in
	the "PIC32 Family Reference Manual",
	which is available from the Microchip
	web site (www.microchip.com/PIC32).

The PIC32MZ EF oscillator system has the following modules and features:

- A total of five external and internal oscillator options as clock sources
- On-Chip PLL with user-selectable input divider, multiplier and output divider to boost operating frequency on select internal and external oscillator sources
- On-Chip user-selectable divisor postscaler on select oscillator sources
- Software-controllable switching between various clock sources
- A Fail-Safe Clock Monitor (FSCM) that detects clock failure and permits safe application recovery or shutdown with dedicated Back-up FRC (BFRC)
- Dedicated On-Chip PLL for USB peripheral
- Flexible reference clock output
- Multiple clock branches for peripherals for better performance flexibility
- · Clock switch/slew control with output divider

A block diagram of the oscillator system is shown in Figure 8-1. The clock distribution is provided in Table 8-1.

Note: Devices that support 252 MHz operation should be configured for SYSCLK <= 200 MHz operation. Adjust the dividers of the PBCLKs, and then increase the SYSCLK to the desired speed.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0					
04.04	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0					
31:24	—	—	—	—	—	—	—	—					
22.16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0					
23:16	—	—	—	—	—	—	—	—					
45.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0					
15:8	CHPDAT<15:8>												
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0					
7:0		CHPDAT<7:0>											

REGISTER 10-18: DCHxDAT: DMA CHANNEL x PATTERN DATA REGISTER

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

bit 15-0 **CHPDAT<15:0>:** Channel Data Register bits <u>Pattern Terminate mode:</u> Data to be matched must be stored in this register to allow terminate on match.

> All other modes: Unused.

REGISTER 11-7: USBIE0CSR3: USB INDEXED ENDPOINT CONTROL STATUS REGISTER 3 (ENDPOINT 0)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	R-x	R-x	R-0	R-x	R-x	R-x	R-1	R-0
31.24	MPRXEN	MPTXEN	BIGEND	HBRXEN	HBTXEN	DYNFIFOS	SOFTCONE	UTMIDWID
22.16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23.10	—		_		—	—	—	
15.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15.0	—	_	_	_	—	—	—	-
7.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
7:0							_	

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31	MPRXEN: Automatic Amalgamation Option bit
--------	--

- 1 = Automatic amalgamation of bulk packets is done
- 0 = No automatic amalgamation
- bit 30 **MPTXEN:** Automatic Splitting Option bit 1 = Automatic splitting of bulk packets is done
 - 0 = No automatic splitting
- bit 29 BIGEND: Byte Ordering Option bit
 - 1 = Big Endian ordering
 - 0 = Little Endian ordering
- bit 28 **HBRXEN:** High-bandwidth RX ISO Option bit 1 = High-bandwidth RX ISO endpoint support is selected 0 = No High-bandwidth RX ISO support
- bit 27 **HBTXEN:** High-bandwidth TX ISO Option bit 1 = High-bandwidth TX ISO endpoint support is selected 0 = No High-bandwidth TX ISO support
- bit 26 **DYNFIFOS:** Dynamic FIFO Sizing Option bit
 - 1 = Dynamic FIFO sizing is supported
 - 0 = No Dynamic FIFO sizing
- bit 25 SOFTCONE: Soft Connect/Disconnect Option bit
 - 1 = Soft Connect/Disconnect is supported
 - 0 = Soft Connect/Disconnect is not supported
- bit 24 UTMIDWID: UTMI+ Data Width Option bit Always '0', indicating 8-bit UTMI+ data width
- bit 23-0 Unimplemented: Read as '0'

SS										E	Bits								
Virtual Addre (BF80_#)	Register Name	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
	10.15	31:16	_	_	_	_	_	_	—	_	—	_	—	—	-	_	_	—	0000
1444	IC4R	15:0	—	—	—	—	—	-	—	—	—	-	—	—		IC4R	<3:0>		0000
	1055	31:16	—	—	—	—	-	_	—	—	—	-	—	—	-	—	_	_	0000
1448	IC5R	15:0		—	—	—	—	—	—	—	—	—	—	—		IC5R	<3:0>		0000
4440	1000	31:16		—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
144C	IC6R	15:0		—	—	—	—	—	—	—	—	—	—	—		IC6R	<3:0>		0000
4.450	1070	31:16		—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
1450	IC/R	15:0	—	—	—	—	—	—	—	—	—	—	—	—		IC7R	<3:0>		0000
	1000	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—		—	0000
1454	IC8R	15:0	—	—	—	—	—	—	—	—	—	—	—	—		IC8R	<3:0>		0000
4.450	1000	31:16			—	—	—	_	—	—	—	_	—	—	_	_	—	—	0000
1458	IC9R	15:0			—	—	—	_	—	—	—	_	—	—		IC9R	<3:0>		0000
4.400	00545	31:16			—	—	—	_	—	—	—	_	—	—	_	_	—	—	0000
1460	OCFAR	15:0			—	—	—	_	—	—	—	_	—	—		OCFA	R<3:0>		0000
		31:16			—	—	—	_	—	—	—	_	—	—	_	_	—	—	0000
1468	UIRXR	15:0			—	—	—	_	—	—	—	_	—	—		U1RX	R<3:0>		0000
	LUCTOR	31:16			—	—	—	_	—	—	—	_	—	—	_	_	—	—	0000
146C	UICISR	15:0			—	—	—	_	—	—	—	_	—	—		U1CTS	SR<3:0>		0000
4.470		31:16			—	—	—	_	—	—	—	_	—	—	_	_	—	—	0000
1470	U2RXR	15:0			—	—	—	_	—	—	—	_	—	—		U2RX	R<3:0>		0000
4 474	LIGOTOD	31:16	—	—	—	—	—	—	_	—	—	—	_	—	—	—	—	-	0000
1474	U2CISR	15:0	—	—	—	—	—	—	_	—	—	—	_	—		U2CTS	SR<3:0>		0000
4.470		31:16	—	—	—	—	—	—	_	—	—	—	_	—	—	—	—	-	0000
1478	UJRXR	15:0	—	—	—	—	—	—	_	—	—	—	_	—		U3RX	R<3:0>		0000
4.470	LIDOTOD	31:16	—	—	—	—	—	—	_	—	—	—	_	—	—	—	—	-	0000
147C	U3CTSR	15:0			—	—	—	_	—	—	—	_	—	—		U3CTS	SR<3:0>		0000
		31:16			—	—	—	_	—	—	—	_	—	—	_	_	—	_	0000
1480	U4RXR	15:0	—	—	—	-	-	-	-	—	—	-	-	—		U4RX	R<3:0>		0000
4.40.4		31:16	—	—	_	—	—	—	—	—	—	—	—	—	—	—	—	_	0000
1484	04CTSR	15:0	_	_	—	_	—	_	_	_	_	_	_	_		U4CTS	SR<3:0>		0000

TABLE 12-22: PERIPHERAL PIN SELECT INPUT REGISTER MAP (CONTINUED)

x = unknown value on Reset; --- = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register is not available on 64-pin devices.

2: This register is not available on devices without a CAN module.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31.24	—	—	—	—	—	—	—	—
00.40	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
23:16	DUI	MMYBYTES.	<2:0>	AI	DDRBYTES<2:	0>	READOPC	CODE<7:6>
45.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
15:8		TYPEDA	\TA<1:0>					
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7:0	TYPEDU	/MY<1:0>	TYPEMC	DE<1:0>	TYPEAD	DR<1:0>	TYPEC	MD<1:0>

REGISTER 20-1: SQI1XCON1: SQI XIP CONTROL REGISTER 1

Legend:

Logonal			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	d as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-24 Unimplemented: Read as '0'

bit 23-21 **DUMMYBYTES<2:0>:** Transmit Dummy Bytes bits

- 111 = Transmit seven dummy bytes after the address bytes
- •
- 011 = Transmit three dummy bytes after the address bytes
- 010 = Transmit two dummy bytes after the address bytes
- 001 = Transmit one dummy bytes after the address bytes
- 000 = Transmit zero dummy bytes after the address bytes

bit 20-18 ADDRBYTES<2:0>: Address Cycle bits

- 111 = Reserved
- •
- •
- 101 = Reserved
- 100 = Four address bytes
- 011 = Three address bytes
- 010 = Two address bytes
- 001 = One address bytes
- 000 = Zero address bytes

bit 17-10 READOPCODE<7:0>: Op code Value for Read Operation bits

These bits contain the 8-bit op code value for read operation.

bit 9-8 TYPEDATA<1:0>: SQI Type Data Enable bits

The boot controller will receive the data in Single Lane, Dual Lane, or Quad Lane.

- 11 = Reserved
- 10 = Quad Lane mode data is enabled
- 01 = Dual Lane mode data is enabled
- 00 = Single Lane mode data is enabled

bit 7-6 **TYPEDUMMY<1:0>:** SQI Type Dummy Enable bits

- The boot controller will send the dummy in Single Lane, Dual Lane, or Quad Lane.
- 11 = Reserved
- 10 = Quad Lane mode dummy is enabled
- 01 = Dual Lane mode dummy is enabled
- 00 = Single Lane mode dummy is enabled

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	
24.24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
31.24				BDADDR	<31:24>				
00.40	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
23:16	BDADDR<23:16>								
45.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
15:8	BDADDR<15:8>								
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
7:0				BDADD	R<7:0>				

REGISTER 20-16: SQI1BDBASEADD: SQI BUFFER DESCRIPTOR BASE ADDRESS REGISTER

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented b	it, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 BDADDR<31:0>: DMA Base Address bits

These bits contain the physical address of the root buffer descriptor. This register should be updated only when the DMA is idle.

REGISTER 20-17: SQI1BDSTAT: SQI BUFFER DESCRIPTOR STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit Bit Bit Bit 29/21/13/5 28/20/12/4 27/19/11/3 26/18/10/		Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	
24.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31.24		—	—	_	—	—	—	_
00.40	U-0	U-0	R-x	R-x	R-x	R-x	R-x	R-x
23:16	—	—		BDSTAT	DMASTART	DMAACTV		
45.0	R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
15.6 BDCON<15:8>								
7.0	R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
7:0				BDCO	N<7:0>			

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit,	read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-22 Unimplemented: Read as '0'

bit 21-18 BDSTATE<3:0>: DMA Buffer Descriptor Processor State Status bits

- These bits return the current state of the buffer descriptor processor:
- 5 = Fetched buffer descriptor is disabled
- 4 = Descriptor is done
- 3 = Data phase
- 2 = Buffer descriptor is loading
- 1 = Descriptor fetch request is pending
- 0 = Idle
- bit 17 DMASTART: DMA Buffer Descriptor Processor Start Status bit
 - 1 = DMA has started
 - 0 = DMA has not started
- bit 16 DMAACTV: DMA Buffer Descriptor Processor Active Status bit
 - 1 = Buffer Descriptor Processor is active
 - 0 = Buffer Descriptor Processor is idle
- bit 15-0 **BDCON<15:0>:** DMA Buffer Descriptor Control Word bits These bits contain the current buffer descriptor control word.

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family

REGISTE	ER 25-2: RTCALRM: REAL-TIME CLOCK ALARM CONTROL REGISTER (CONTINUED)				
bit 7-0	ARPT<7:0>: Alarm Repeat Counter Value bits ⁽²⁾				
	11111111 = Alarm will trigger 256 times				
	•				
	•				
	0000000 = Alarm will trigger one time				
	The counter decrements on any alarm event. The counter only rolls over from $0x00$ to $0xFF$ if CHIME = 1.				
Note 1:	Hardware clears the ALRMEN bit anytime the alarm event occurs, when $ARPT < 7:0 > = 0.0$ and $CHIME = 0.$				
2:	This field should not be written when the RTCC ON bit = '1' (RTCCON<15>) and ALRMSYNC = 1.				

Note: This register is reset only on a Power-on Reset (POR).

26.0 CRYPTO ENGINE

Note: This data sheet summarizes the features of the PIC32MZ EF family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 49. "Crypto Engine (CE) and Random Number Generator (RNG)" (DS60001246) in the "PIC32 Family Reference Manual". which is available from the Microchip web site (www.microchip.com/PIC32).

The Crypto Engine is intended to accelerate applications that need cryptographic functions. By executing these functions in the hardware module, software overhead is reduced and actions, such as encryption, decryption, and authentication can execute much more quickly.

The Crypto Engine uses an internal descriptor-based DMA for efficient programming of the security association data and packet pointers (allowing scatter/ gather data fetching). An intelligent state machine schedules the Crypto Engines based on the protocol selection and packet boundaries. The hardware engines can perform the encryption and authentication in sequence or in parallel.

The following are key features of the Crypto Engine:

- Bulk ciphers and hash engines
- Integrated DMA to off-load processing:
 - Buffer descriptor-based
 - Secure association per buffer descriptor
- Some functions can execute in parallel

Bulk ciphers that are handled by the Crypto Engine include:

- AES:
 - 128-bit, 192-bit, and 256-bit key sizes
 - CBC, ECB, CTR, CFB, and OFB modes
- DES/TDES:
 - CBC, ECB, CFB, and OFB modes

Authentication engines that are available through the Crypto Engine include:

- SHA-1
- SHA-256
- MD-5
- AES-GCM
- HMAC operation (for all authentication engines)

The rate of data that can be processed by the Crypto Engine depends on these factors:

- Which engine is in use
- Whether the engines are used in parallel or in series
- The demands on source and destination memories by other parts of the system (i.e., CPU, DMA, etc.)
- The speed of PBCLK5, which drives the Crypto Engine

Table 26-1 shows typical performance for various engines.

TABLE 26-1: CRYPTO ENGINE PERFORMANCE

Engine/ Algorithm (Mbps/MHz)		Maximum Mbps (PBCLK5 = 100 MHz)
DES	14.4	1440
TDES	6.6	660
AES-128	9.0	900
AES-192	7.9	790
AES-256	7.2	720
MD5	15.6	1560
SHA-1	13.2	1320
SHA-256	9.3	930

FIGURE 26-1: CRYPTO ENGINE BLOCK DIAGRAM



Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
04.04	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0, HS, HC
31:24	AFEN	DATA16EN	DFMODE	C	VRSAM<2:0	AFGIEN	AFRDY	
00.40	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
23:16	—	_	—	CHNLID<4:0>				
15.0	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC					
15.0				FLTRDATA<15:8>				
7.0	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC					
7:0				FLTRDAT	A<7:0>			

REGISTER 28-16: ADCFLTRx: ADC DIGITAL FILTER 'x' REGISTER ('x' = 1 THROUGH 6)

Legend:	HS = Hardware Set	HC = Hardware Cleared
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	0' = Bit is cleared x = Bit is unknown

bit 31 **AFEN:** Digital Filter 'x' Enable bit

- 1 = Digital filter is enabled
- 0 = Digital filter is disabled and the AFRDY status bit is cleared
- bit 30 DATA16EN: Filter Significant Data Length bit
 - 1 = AII 16 bits of the filter output data are significant
 - 0 =Only the first 12 bits are significant, followed by four zeros
 - **Note:** This bit is significant only if DFMODE = 1 (Averaging Mode) and FRACT (ADCCON1<23>) = 1 (Fractional Output Mode).

bit **DFMODE:** ADC Filter Mode bit

- 1 = Filter 'x' works in Averaging mode
- 0 = Filter 'x' works in Oversampling Filter mode (default)

bit 28-26 **OVRSAM<2:0>:** Oversampling Filter Ratio bits

If DFMODE is '0':

- 111 = 128 samples (shift sum 3 bits to right, output data is in 15.1 format)
- 110 = 32 samples (shift sum 2 bits to right, output data is in 14.1 format)
- 101 = 8 samples (shift sum 1 bit to right, output data is in 13.1 format)
- 100 = 2 samples (shift sum 0 bits to right, output data is in 12.1 format)
- 011 = 256 samples (shift sum 4 bits to right, output data is 16 bits)
- 010 = 64 samples (shift sum 3 bits to right, output data is 15 bits)
- 001 = 16 samples (shift sum 2 bits to right, output data is 14 bits)
- 000 = 4 samples (shift sum 1 bit to right, output data is 13 bits)

If DFMODE is '1':

- 111 = 256 samples (256 samples to be averaged)
- 110 = 128 samples (128 samples to be averaged)
- 101 = 64 samples (64 samples to be averaged)
- 100 = 32 samples (32 samples to be averaged)
- 011 = 16 samples (16 samples to be averaged)
- 010 = 8 samples (8 samples to be averaged)
- 001 = 4 samples (4 samples to be averaged)
- 000 = 2 samples (2 samples to be averaged)
- bit 25 **AFGIEN:** Digital Filter 'x' Interrupt Enable bit
 - 1 = Digital filter interrupt is enabled and is generated by the AFRDY status bit
 - 0 = Digital filter is disabled

REGISTE	R 29-15:	CIFLTCON5: CAN FILTER CONTROL REGISTER 5 (CONTINUED)					
bit 15	FLTEN21	: Filter 21 Enable bit					
	1 = Filter is enabled						
	0 = Filter	is disabled					
bit 14-13	MSEL21<	MSEL21<1:0>: Filter 21 Mask Select bits					
	11 = Acce	eptance Mask 3 selected					
	10 = Acce	eptance Mask 2 selected					
	01 = Acce	eptance Mask T selected					
hit 12-8	FSEI 21~	A:D-: FIFO Selection hits					
511 12 0	11111 = 1	Message matching filter is stored in EIEO buffer 31					
	11110 = 1	Message matching filter is stored in FIFO buffer 30					
	•						
	•						
	•						
	00001 = I	Message matching filter is stored in FIFO buffer 1					
	00000 = I	Message matching filter is stored in FIFO buffer 0					
bit 7	FLTEN20	: Filter 20 Enable bit					
	1 = Filter	is enabled					
	0 = Filter	is disabled					
bit 6-5	MSEL20<	:1:0>: Filter 20 Mask Select bits					
	11 = Acce	eptance Mask 3 selected					
	10 = Acce	eptance Mask 2 selected					
	01 = Acce	eptance Mask 1 selected					
hit 1 0							
DIL 4-0	TJEL204	4:0>: FIFO Selection bits					
	11111 = 1	Message matching filter is stored in FIFO buffer 31					
		Message matching interns stored in FIFO buller 50					
	•						
	00001 – I	Message matching filter is stored in EIEO buffer 1					
	00000 = Message matching filter is stored in FIFO buffer 0						
Note:	The bits in	this register can only be modified if the corresponding filter enable (FLTENn) bit is '0'.					

36.0 DEVELOPMENT SUPPORT

The PIC[®] microcontrollers (MCU) and dsPIC[®] digital signal controllers (DSC) are supported with a full range of software and hardware development tools:

- Integrated Development Environment
 - MPLAB[®] X IDE Software
- Compilers/Assemblers/Linkers
 - MPLAB XC Compiler
 - MPASM[™] Assembler
 - MPLINK[™] Object Linker/ MPLIB[™] Object Librarian
 - MPLAB Assembler/Linker/Librarian for Various Device Families
- Simulators
 - MPLAB X SIM Software Simulator
- Emulators
- MPLAB REAL ICE™ In-Circuit Emulator
- In-Circuit Debuggers/Programmers
 - MPLAB ICD 3
 - PICkit[™] 3
- Device Programmers
- MPLAB PM3 Device Programmer
- Low-Cost Demonstration/Development Boards, Evaluation Kits and Starter Kits
- Third-party development tools

36.1 MPLAB X Integrated Development Environment Software

The MPLAB X IDE is a single, unified graphical user interface for Microchip and third-party software, and hardware development tool that runs on Windows[®], Linux and Mac OS[®] X. Based on the NetBeans IDE, MPLAB X IDE is an entirely new IDE with a host of free software components and plug-ins for high-performance application development and debugging. Moving between tools and upgrading from software simulators to hardware debugging and programming tools is simple with the seamless user interface.

With complete project management, visual call graphs, a configurable watch window and a feature-rich editor that includes code completion and context menus, MPLAB X IDE is flexible and friendly enough for new users. With the ability to support multiple tools on multiple projects with simultaneous debugging, MPLAB X IDE is also suitable for the needs of experienced users.

Feature-Rich Editor:

- · Color syntax highlighting
- Smart code completion makes suggestions and provides hints as you type
- Automatic code formatting based on user-defined rules
- Live parsing

User-Friendly, Customizable Interface:

- Fully customizable interface: toolbars, toolbar buttons, windows, window placement, etc.
- · Call graph window

Project-Based Workspaces:

- Multiple projects
- Multiple tools
- Multiple configurations
- · Simultaneous debugging sessions

File History and Bug Tracking:

- · Local file history feature
- Built-in support for Bugzilla issue tracker



FIGURE 37-22: PARALLEL MASTER PORT READ TIMING DIAGRAM

TABLE 37-43: PARALLEL MASTER PORT READ TIMING REQUIREMENTS

АС СНА	AC CHARACTERISTICS			$\begin{tabular}{lllllllllllllllllllllllllllllllllll$				
Param. No.	Symbol	Characteristics ⁽¹⁾	Min.	Тур.	Max.	Units	Conditions	
PM1	TLAT	PMALL/PMALH Pulse Width	—	1 TPBCLK2	_	_	_	
PM2	TADSU	Address Out Valid to PMALL/ PMALH Invalid (address setup time)		2 TPBCLK2	—	_		
PM3	TADHOLD	PMALL/PMALH Invalid to Address Out Invalid (address hold time)		1 TPBCLK2	_	_		
PM4	TAHOLD	PMRD Inactive to Address Out Invalid (address hold time)	5	—	_	ns	_	
PM5	Trd	PMRD Pulse Width	—	1 TPBCLK2	—	—	—	
PM6	TDSU	PMRD or PMENB Active to Data In Valid (data setup time)	15	_		ns		
PM7	TDHOLD	PMRD or PMENB Inactive to Data In Invalid (data hold time)		80		ns		

Note 1: These parameters are characterized, but not tested in manufacturing.

38.2 AC Characteristics and Timing Parameters

The information contained in this section defines PIC32MZ EF device AC characteristics and timing parameters.

TABLE 38-5:	SYSTEM TIMING REQUIREMENTS
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AC CHARACTERISTICS		Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}C \le TA \le +125^{\circ}C$ for Extended					
Param. No.	^{n.} Symbol Characteristics		Min.	Тур.	Max.	Units	Conditions
EOS51	Fsys	System Frequency	DC	—	180	MHz	USB module disabled
			30	_	180	MHz	USB module enabled
EOS55a	Fрв	Peripheral Bus Frequency	DC		90	MHz	For PBCLKx, 'x' \neq 4, 7
EOS55b			DC		180	MHz	For PBCLK4, PBCLK7
EOS56	Fref	Reference Clock Frequency	_		45	MHz	For REFCLKI1, 3, 4 and REFCLKO1, 3, 4 pins

TABLE 38-6: PLL CLOCK TIMING SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions: 2.1V to 3.6V(unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +125^{\circ}C$ for Extended					
Param. No.	Symbol	Characteristics ⁽¹⁾		Min.	Typical	Max.	Units	Conditions
EOS54a	Fpll	PLL Output Frequency Range		10	_	180	MHz	

Note 1: These parameters are characterized, but not tested in manufacturing.

2: This jitter specification is based on clock-cycle by clock-cycle measurements. To get the effective jitter for individual time-bases on communication clocks, use the following formula:

$$EffectiveJitter = \frac{D_{CLK}}{\sqrt{\frac{PBCLK2}{\sqrt{CommunicationClock}}}}$$

For example, if PBCLK2 = 100 MHz and SPI bit rate = 50 MHz, the effective jitter is as follows:

$$EffectiveJitter = \frac{D_{CLK}}{\sqrt{\frac{100}{50}}} = \frac{D_{CLK}}{1.41}$$

39.1 DC Characteristics

TABLE 39-1: OPERATING MIPS VS. VOLTAGE

	VDD Range	Temp. Range	Max. Frequency	Comment
Characteristic	(in volts) (Note 1)	(in °C)	PIC32MZ EF Devices	
MDC5	2.1V-3.6V	-40°C to +85°C	252 MHz	

Note 1: Overall functional device operation at VBORMIN < VDD < VDDMIN is guaranteed, but not characterized. All device Analog modules, such as ADC, etc., will function, but with degraded performance below VDDMIN. Refer to parameter BO10 in Table 37-5 for BOR values.

TABLE 39-2: DC CHARACTERISTICS: OPERATING CURRENT (IDD)

DC CHARA	CTERISTICS		Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial		
Parameter No.	arameter No. Typical ⁽³⁾ Maximum ⁽⁶⁾		Units	Conditions	
Operating Current (IDD) ⁽¹⁾					
MDC27a	156	170	mA	252 MHz (Note 2)	
MDC27b	115	135	mA	252 MHz (Note 4,5)	

Note 1: A device's IDD supply current is mainly a function of the operating voltage and frequency. Other factors, such as PBCLK (Peripheral Bus Clock) frequency, number of peripheral modules enabled, internal code execution pattern, I/O pin loading and switching rate, oscillator type, as well as temperature, can have an impact on the current consumption.

- **2:** The test conditions for IDD measurements are as follows:
 - Oscillator mode is EC+PLL with OSC1 driven by external square wave from rail-to-rail, (OSC1 input clock input over/undershoot < 100 mV required)
 - OSC2/CLKO is configured as an I/O input pin
 - USB PLL is disabled (USBMD = 1), VUSB3V3 is connected to VSS
 - CPU, Program Flash, and SRAM data memory are operational, Program Flash memory Wait states are equal to four
 - L1 Cache and Prefetch modules are enabled
 - No peripheral modules are operating, (ON bit = 0), and the associated PMD bit is set. All clocks are disabled ON bit (PBxDIV<15>) = 0 (x ≠ 1,7)
 - WDT, DMT, Clock Switching, Fail-Safe Clock Monitor, and Secondary Oscillator are disabled
 - All I/O pins are configured as inputs and pulled to Vss
 - MCLR = VDD
 - CPU executing while(1) statement from Flash
 - RTCC and JTAG are disabled
- **3:** Data in "Typical" column is at 3.3V, +25°C at specified operating frequency unless otherwise stated. Parameters are for design guidance only and are not tested.
- 4: This parameter is characterized, but not tested in manufacturing.
- 5: Note 2 applies with the following exceptions: L1 Cache and Prefetch modules are disabled, Program Flash memory Wait states are equal to seven.
- **6:** Data in the "Maximum" column is at 3.3V, +85°C at specified operating frequency, unless otherwise stated. Parameters are for design guidance only and are not tested.

A.4 Resets

The PIC32MZ EF family of devices has updated the resets modules to incorporate the new handling of NMI resets from the WDT, DMT, and the FSCM. In addition, some bits have been moved, as summarized in Table A-5.

TABLE A-5: RESET DIFFERENCES

PIC32MX5XX/6XX/7XX Feature	PIC32MZ EF Feature
Power	Reset
	The VREGS bit, which controls whether the internal regulator is enabled in Sleep mode, has been moved from RCON in PIC32MX5XX/6XX/7XX devices to a new PWRCON register in PIC32MZ EF devices.
VREGS (RCON<8>)	VREGS (PWRCON<0>)
1 = Regulator is enabled and is on during Sleep mode	1 = Voltage regulator will remain active during Sleep
0 = Regulator is disabled and is off during Sleep mode	0 = Voltage regulator will go to Stand-by mode during Sleep
Watchdog	Fimer Reset
On PIC32MX devices, a WDT expiration immediately triggers a device reset.	On PIC32MZ EF devices, the WDT expiration now causes a NMI. The WDTO bit in RNMICON indicates that the WDT caused the NMI. A new timer, NMICNT, runs when the WDT NMI is triggered, and if it expires, the device is reset.
WDT expiration immediately causes a device reset.	WDT expiration causes a NMI, which can then trigger the device reset. WDTO (RNMICON<24>) 1 = WDT time-out has occurred and caused a NMI 0 = WDT time-out has not occurred
	NMICNT<7:0> (RNMICON<7:0>)

A.5 USB

The PIC32MZ EF family of devices has a new Hi-Speed USB module, which requires the updated USB stack from Microchip. In addition, the USB PLL was also updated. See **A.1** "Oscillator and PLL Configuration" for more information and Table A-6 for a list of additional differences.

TABLE A-6: USB DIFFERENCES

PIC32MX5XX/6XX/7XX Feature	PIC32MZ EF Feature	
Debug	I Mode	
On PIC32MX devices, when stopping on a breakpoint during debugging, the USB module can be configured to stop or continue execution from the Freeze Peripherals dialog in MPLAB X IDE.	On PIC32MZ EF devices, the USB module continues operating when stopping on a breakpoint during debugging.	
VBUS	on Pin	
PIC32MX devices feature a VBUSON pin for controlling the external transceiver power supply.	On PIC32MZ EF devices, the VBUSON pin is not available. A port pin can be used to achieve the same functionality.	

B.4

System Bus

two key differences listed in Table B-3.

The system bus on PIC32MZ EF devices is similar to

the system bus on PIC32MZ EC devices. There are

B.3 CPU

The CPU in PIC32MZ EC devices is the microAptiv[™] MPU architecture. The CPU in the PIC32MZ EF devices is the Series 5 Warrior M-Class M5150 MPU architecture. Most PIC32MZ EF M-Class core features are identical to the microAptiv[™] core in PIC32MZ EC devices. The main differences are that in PIC32MZ EF devices, a floating-point unit (FPU) is included for improved math performance, and PC Sampling for performance measurement.

TABLE B-3: SYSTEM BUS DIFFERENCES

PIC32MZ EC Feature	PIC32MZ EF Feature
Permission Gro	oups during NMI
On PIC32MZ EC devices, the permission group in which the CPU is part of is lost during NMI handling, and must be manually restored.	On PIC32MZ EF devices, the prior permission group is preserved, and is restored when the CPU returns from the NMI handler.
DMA A	Access
The DMA can access the peripheral registers on Peripheral Bus 1.	On PIC32MZ EF devices, the DMA no longer has access to registers on Peripheral Bus 1. Refer to Table 4-4 for details on which peripherals are now excluded.

B.5 Flash Controller

The Flash controller on PIC32MZ EF devices adds the ability both to control boot Flash aliasing, and for locking the current swap settings. Table B-4 lists theses differences.

TABLE B-4:FLASH CONTROLLER DIFFERENCES

PIC32MZ EC Feature	PIC32MZ EF Feature
Boot Flas	h Aliasing
On PIC32MZ EC devices, Boot Flash aliasing is done through the DEVSEQ0 register, but no further changes are possible without rebooting the processor.	On PIC32MZ EF devices, the initial Boot Flash aliasing is determined by the DEVSEQ3 register, but the BFSWAP bit (NVMCON<6>) reflects the state of the aliasing, and can be modified to change it during run-time.
	 BFSWAP (NVMCON<6>) 1 = Boot Flash Bank 2 is mapped to the lower boot alias, and Boot Flash bank 1 is mapped to the upper boot alias 0 = Boot Flash Bank 1 is mapped to the lower boot alias, and Boot Flash Bank 2 is mapped to the upper boot alias
PFM and BFM	Swap Locking
On PIC32MZ EC devices, the swapping of PFM is always available.	On PIC32MZ EF devices, a new control, SWAPLOCK<1:0> (NVMCON2<7:6>) allows the locking of PFSWAP and BFSWAP bits, and can restrict any further changes.
	 SWAPLOCK<1:0> (NVMCON2<7:6>) 11 = PFSWAP and BFSWAP are not writable and SWAPLOCK is not writable 10 = PFSWAP and BFSWAP are not writable and SWAPLOCK is writable 01 = PFSWAP and BFSWAP are not writable and SWAPLOCK is writable 00 = PFSWAP and BFSWAP are writable and SWAPLOCK is writable

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