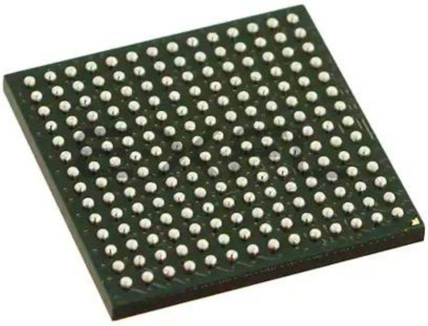

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Details	
Product Status	Obsolete
Core Processor	Coldfire V2
Core Size	32-Bit Single-Core
Speed	66MHz
Connectivity	EBI/EMI, Ethernet, I²C, SPI, UART/USART, USB
Peripherals	DMA, WDT
Number of I/O	32
Program Memory Size	16KB (4K x 32)
Program Memory Type	ROM
EEPROM Size	-
RAM Size	1K x 32
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	-
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	196-LBGA
Supplier Device Package	196-LBGA (15x15)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcf5272vf66

Table of Contents (Continued)

Chapter 17
General Purpose I/O Module

Chapter 18
Pulse-Width Modulation (PWM) Module

Chapter 19
Signal Descriptions

List of Tables (Continued)

Table 2-21. MCF5272 Exceptions (continued)

Exception	Description
Interrupt Exception	Interrupt exception processing, with interrupt recognition and vector fetching, includes uninitialized and spurious interrupts as well as those where the requesting device supplies the 8-bit interrupt vector.
Reset Exception	Asserting the reset input signal ($\overline{\text{RSTI}}$) causes a reset exception. Reset has the highest exception priority; it provides for system initialization and recovery from catastrophic failure. When assertion of $\overline{\text{RSTI}}$ is recognized, current processing is aborted and cannot be recovered. The reset exception places the processor in supervisor mode by setting SR[S] and disables tracing by clearing SR[T]. This exception also clears SR[M] and sets the processor's interrupt priority mask in the SR to the highest level (level 7). Next, the VBR is initialized to 0x0000_0000. Configuration registers controlling the operation of all processor-local memories (cache and RAM modules on the MCF5272) are invalidated, disabling the memories. **Note:** Other implementation-specific supervisor registers are also affected. Refer to each of the modules in this manual for details on these registers. If the processor is not halted and it has ownership of the bus, it initiates the reset exception by performing two longword read bus cycles. The longword at address 0 is loaded into the stack pointer and the longword at address 4 is loaded into the PC. After the initial instruction is fetched from memory, program execution begins at the address in the PC. If an access error or address error occurs before the first instruction executes, the processor enters the fault-on-fault halted state.

If a ColdFire processor encounters any type of fault during the exception processing of another fault, the processor immediately halts execution with the catastrophic fault-on-fault condition. A reset is required to force the processor to exit this halted state.

3.1.3 MAC Instruction Set Summary

The MAC unit supports the integer multiply operations defined by the baseline ColdFire architecture and the new multiply-accumulate instructions. Table 3-1 summarizes the MAC unit instruction set.

Table 3-1. MAC Instruction Summary

Instruction	Mnemonic	Description
Multiply Signed	MULS <ea>y,Dx	Multiplies two signed operands yielding a signed result
Multiply Unsigned	MULU <ea>y,Dx	Multiplies two unsigned operands yielding an unsigned result
Multiply Accumulate	MAC Ry,RxSF MSAC Ry,RxSF	Multiplies two operands, then adds or subtracts the product to/from the accumulator
Multiply Accumulate with Load	MAC Ry,RxSF,Rw MSAC Ry,RxSF,Rw	Multiplies two operands, then adds or subtracts the product to/from the accumulator while loading a register with the memory operand
Load Accumulator	MOV.L {Ry,#imm},ACC	Loads the accumulator with a 32-bit operand
Store Accumulator	MOV.L ACC,Rx	Writes the contents of the accumulator to a register
Load MACSR	MOV.L {Ry,#imm},MACSR	Writes a value to the MACSR
Store MACSR	MOV.L MACSR,Rx	Writes the contents of MACSR to a register
Store MACSR to CCR	MOV.L MACSR,CCR	Writes the contents of MACSR to the processor's CCR register
Load MASK	MOV.L {Ry,#imm},MASK	Writes a value to MASK
Store MASK	MOV.L MASK,Rx	Writes the contents of MASK to a register

3.1.4 Data Representation

The MAC unit supports three basic operand types:

- Two's complement signed integer: In this format, an N-bit operand represents a number within the range $-2^{(N-1)} \leq \text{operand} \leq 2^{(N-1)} - 1$. The binary point is to the right of the least significant bit.
- Two's complement unsigned integer: In this format, an N-bit operand represents a number within the range $0 \leq \text{operand} \leq 2^{N} - 1$. The binary point is to the right of the least significant bit.
- Two's complement, signed fractional: In an N-bit number, the first bit is the sign bit. The remaining bits signify the first N-1 bits after the binary point. Given an N-bit number, $a_{N-1}a_{N-2}a_{N-3}\ldots a_2a_1a_0$, its value is given by the following formula:

$$+ \sum_{i=0}^{N-2} 2^{(i+1-N)} \cdot ai$$

  This format can represent numbers in the range $-1 \leq \text{operand} \leq 1 - 2^{(N-1)}$.

  For words and longwords, the greatest negative number that can be represented is –1, whose internal representation is 0x8000 and 0x0x8000_0000, respectively. The most positive word is 0x7FFF or $(1 - 2^{-15})$; the most positive longword is 0x7FFF_FFFF or $(1 - 2^{-31})$.

3.2 MAC Instruction Execution Timings

For information on MAC instruction execution timings, refer to Section 2.7, "Instruction Timing."

4.3.2.1 SRAM Base Address Register (RAMBAR)

RAMBAR determines the base address location of the internal SRAM module, as well as the definition of the types of accesses allowed for it.

- RAMBAR is a 32-bit write-only supervisor control register. It is accessed in the CPU address space via the MOVEC instruction with an Rc encoding of 0xC04. RAMBAR can be read or written in background debug mode (BDM). At system reset, the V bit is cleared and the remaining bits are uninitialized. To access the SRAM module, RAMBAR must be written with the appropriate base address after system reset.
- The SRAM base address register (RAMBAR) can be accessed only in supervisor mode using the MOVEC instruction with an Rc value of 0xC04.

	31–12	11–9	8	7–6	5	4	3	2	1	0
Field	BA	—	WP	—	C/I	SC	SD	UC	UD	V
Reset	—									0
R/W	W for CPU; R/W for debug									
Address	CPU space + 0xC04									

Figure 4-1. SRAM Base Address Register (RAMBAR)

RAMBAR fields are described in Table 4-2.

Table 4-2. RAMBAR Field Description

Bits	Name	Description
31–12	BA	Base address. SRAM module base address. The SRAM module occupies a 4-Kbyte space defined by BA. SRAM can reside on any 4-Kbyte boundary in the 4-Gbyte address space.
11–9	—	Reserved, should be cleared.
8	WP	Write protect. Controls read/write properties of the SRAM. 0 Allows read and write accesses to the SRAM module. 1 Allows only read accesses to the SRAM module. Any attempted write reference generates an access error exception to the ColdFire processor core.
7–6	—	Reserved, should be cleared.
5–1	C/I, SC, SD, UC, UD	Address space masks (AS*n*). These fields allow certain types of accesses to be masked, or inhibited from accessing the SRAM module. These bits are useful for power management as described in Section 4.3.2.3, “Programming RAMBAR for Power Management.” In particular, C/I is typically set. The address space mask bits are follows: C/I = CPU space/interrupt acknowledge cycle mask. Note that C/I must be set if BA = 0. SC = Supervisor code address space mask SD = Supervisor data address space mask UC = User code address space mask UD = User data address space mask For each AS*n* bit: 0 An access to the SRAM module can occur for this address space 1 Disable this address space from the SRAM module. References to this address space cannot access the SRAM module and are processed like other non-SRAM references.
0	V	Valid. Enables/disables the SRAM module. V is cleared at reset. 0 RAMBAR contents are not valid. 1 RAMBAR contents are valid.

5.5.3.3.5 Dump Memory Block (DUMP)

DUMP is used with the READ command to access large blocks of memory. An initial READ is executed to set up the starting address of the block and to retrieve the first result. If an initial READ is not executed before the first DUMP, an illegal command response is returned. The DUMP command retrieves subsequent operands. The initial address is incremented by the operand size (1, 2, or 4) and saved in a temporary register. Subsequent DUMP commands use this address, perform the memory read, increment it by the current operand size, and store the updated address in the temporary register.

NOTE

DUMP does not check for a valid address; it is a valid command only when preceded by NOP, READ, or another DUMP command. Otherwise, an illegal command response is returned. NOP can be used for intercommand padding without corrupting the address pointer.

The size field is examined each time a DUMP command is processed, allowing the operand size to be dynamically altered.

Command/Result Formats:

		15–12	11–8	7–4	3–0
Byte	Command	0x1	0xD	0x0	0x0
	Result	X X X X	X X X X	D[7:0]	
Word	Command	0x1	0xD	0x4	0x0
	Result	D[15:0]			
Longword	Command	0x1	0xD	0x8	0x0
	Result	D[31:16]			
		D[15:0]			

Figure 5-25. DUMP Command/Result Formats

Command Sequence:

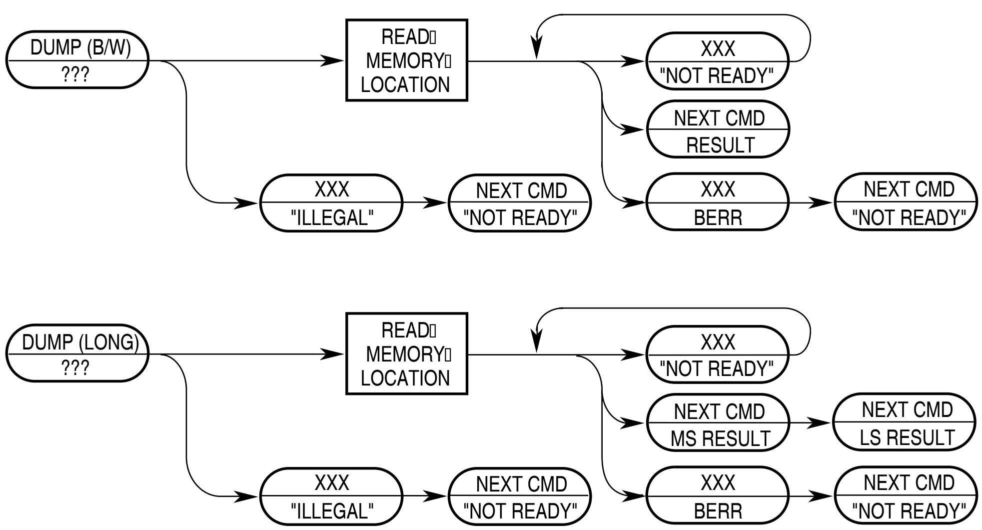

Figure 5-26. DUMP Command Sequence

11.7 Differences between MCF5272 FEC and MPC860T FEC

The MCF5272 features the same FEC as the MPC860T with a few differences. The following list pertains to the MCF5272.

- Limited throughput full-duplex 100 Mbps operation. External bus use is the limiting factor.
- Only big-endian mode is supported for buffer descriptors and buffers.
- Separate interrupt vectors for Rx, Tx and non-time critical interrupts
- Interrupt priority is set in the interrupt controller
- The formula for calculating E_MDC clock frequency differs between MCF5272 and MPC860T:
  — MCF5272: E_MDC_FREQUENCY= system frequency / (4 * MII_SPEED)
  — MPC860T: E_MDC_FREQUENCY= system frequency / (2 * MII_SPEED)

NOTE

MCF5272 ethernet controller signal names are generally identical to those used in the MPC860T, except for a prefix of 'E_'. For example, MDC in the MPC860T corresponds to E_MDC in the MCF5272.

packet size and the EPDP*n* registers are updated in real-time, not just at the end of a packet as with other endpoint types. If the packet size is larger than the FIFO size, the FIFO level interrupt must be used.

Isochronous packets are guaranteed to occur once per USB frame. The SOF and ASOF interrupts are provided in order for the user to synchronize the data flow with the USB. The SOF interrupt occurs every 1 ms provided the USB is active. The ASOF interrupt is generated if the USB module fails to detect a SOF packet within the set timeout period.

It is strongly recommended that interrupts be used rather than polling for isochronous endpoints as isochronous endpoints do not have any error detection or flow-control mechanisms. If the packet size is larger than the FIFO size, using interrupts is required.

12.4.4.2.1 IN Endpoints

The user should write one packet of data to the IN FIFO per frame. If an ASOF interrupt occurs, the user may wish to insert additional data in the data stream if the data for the frame is lost. The following example demonstrates how to handle an isochronous IN packet each frame with a packet size larger than the FIFO size:

1. Wait for the SOF interrupt for synchronization.
2. Write data to the FIFO until filled.
3. Wait for FIFO_LVL interrupt.
4. Read EP*n*DP to determine the number of bytes that can be written to the FIFO.
5. Write data to the FIFO to fill it or until all of the data for the packet has been written.
6. Repeat steps 3–5 until the entire packet has been written to the FIFO.

12.4.4.2.2 OUT Endpoints

The user should read one packet of data from the OUT FIFO per frame. If an ASOF interrupt occurs, the user may wish to discard the data for the frame. The following example demonstrates how to handle an isochronous OUT packet each frame with a packet size larger than the FIFO size:

1. Wait for SOF interrupt for synchronization. The user may want to track that a packet is received for every frame.
2. Wait for the FIFO_LVL interrupt.
3. Read EPDP*n* to determine number of bytes in the FIFO.
4. Read data the indicated number of bytes from the FIFO.
5. Repeat steps 2–4 until entire packet is received.
6. Wait for EOP or SOF interrupt and read any remaining data in the FIFO.
7. An EOT interrupt indicates a short or zero-length packet.

12.4.5 Class- and Vendor-Specific Request Operation

The class- and vendor-specific requests are specific to a particular device class or vendor, and are not processed by the USB request processor. When the USB module receives a class or vendor request, the parameters for the request are written to the DRR1 and DRR2 registers and the user is notified of the

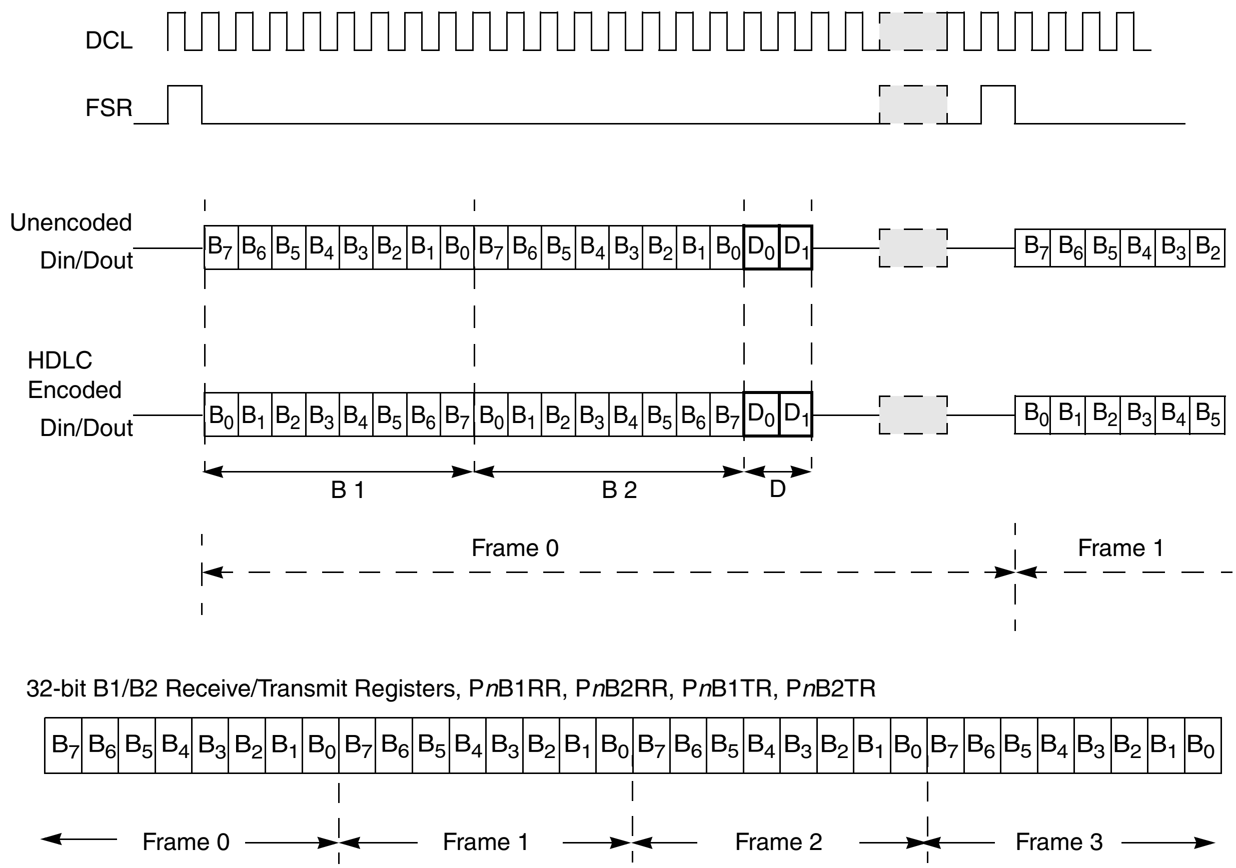

Figure 13-6. B-Channel Unencoded and HDLC Encoded Data

13.2.3.2 B-Channel HDLC Encoded Data

When the incoming B channels contain HDLC encoded data they are presented on the physical line least significant bit (lsb) first. The Soft HDLC expects the first bit received to be aligned in the lsb position of a byte, with the last bit received aligned in the msb position.

Because the presentation of HDLC encoded data on the physical interface is lsb (least significant bit) first for B1 and B2 the lsb is right-aligned in the transmit and receive shift register, that is, the first bit of the B-channel received is aligned in the lsb position through to the last received bit of a byte that is aligned in the msb position.

The ordering of the bytes over four frames within the longword register is as for unencoded data; that is, the first frame is aligned in the MSB through to the fourth frame, which is aligned in the LSB position. See Figure 13-6.

13.2.3.3 D-Channel HDLC Encoded Data

When the incoming D channels contain HDLC-encoded data, they are presented on the physical line lsb first. The Soft HDLC expects the first bit received to be aligned in the lsb position of a byte, with the last bit received aligned in the msb position.

13.5.13 GCI Monitor Channel Transmit Registers (P0GMT–P3GMT)

All bits in these registers are read/write and are cleared on hardware or software reset.

The P*n*GMT registers are 16 bit register containing the control and monitor channel bits to be transmitted for each of the four ports on the MCF5272.

A byte of monitor channel data to be transmitted on a certain port is put into an associated register using the format shown in Figure 13-25. A maskable interrupt is generated when this byte of data has been successfully transmitted.

	15–10	9	8	7–0
Field	—	L	R	M
Reset	0000_0000_0000_0000			
R/W	Read/Write			
Addr	MBAR + 0x368 (P0GMT); 0x36A (P1GMT); 0x36C (P2GMT); 0x36E (P3GMT)			

Figure 13-25. GCI Monitor Channel Transmit Registers (P0GMT–P3GMT)

Table 13-8. P0GMT–P3GMT Field Descriptions

Bits	Name	Description
15–10	—	Reserved, should be cleared.
9	L	Last. 0 Default reset value 1 Set by the CPU. Indicates to the monitor channel controller to transmit the end of message signal on the E bit. Both P*n*GMT[L] and P*n*GMT[R] must be set for the monitor channel controller to send the end of message signal. P*n*GMT[M7:0] are ignored and 0xFF is sent with the end of message condition necessitating sending the monitor channel information using P*n*GMT[R] to control the monitor channel transmitter, followed at the end of the frame by setting P*n*GMT[L] and P*n*GMT[R]. The L bit is automatically cleared by the GCI controller.
8	R	Ready. 0 Default reset value. 1 Set by the CPU. Indicate to the monitor channel controller that a byte of data is ready for transmission. Automatically cleared by the GCI controller when it generates a transmit acknowledge (ACK bit in PGMTS register) or when the L bit is reset.
7–0	M	Monitor channel data byte. Written by the CPU when a byte is ready for transmission.

13.6.3 Example 1: ISDN SOHO PBX with Ports 0, 1, 2, and 3

In this example, all four ports are used to connect an external transceiver and six CODECs. Port 0 and port 1 are programmed in slave mode. An external transceiver, MC145574, is connected to port 0. Port 1, 2, and 3 are used to connect up to six external PCM CODECs.

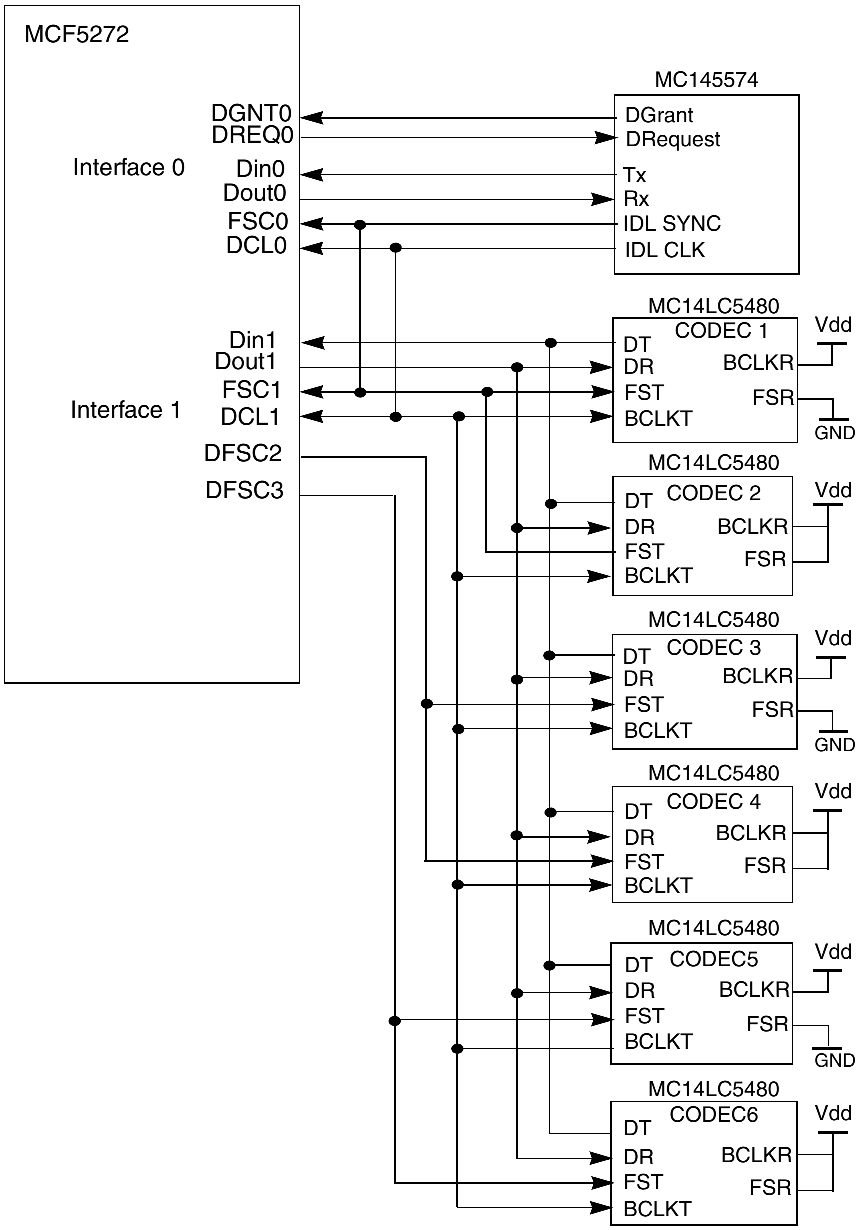

Figure 13-37. ISDN SOHO PABX Example

In the previous example, Freescale's MC14LC5480 CODECs and MC145574 S/T transceiver are shown. The S/T transceiver in this example is connected to port 0 and the FSC0 frame sync signal is used exclusively for synchronizing the data on the transceiver's IDL interface. CODECs 1 and 2 are connected to frame sync 1, FSC1. CODECs 3 and 4 are connected to DFSC2 which is the output of programmable

15.3.5 Timer Event Registers (TER0–TER3)

TERs are used to report events recognized by the timer. On recognition of an event, the timer sets the appropriate TER*n* bit, regardless of the corresponding interrupt enable bits (ORI and CE) in the TMR*n*. Writing a 1 to a bit clears it; writing 0 has no effect. Both bits must be cleared before the timer can negate the request to the interrupt controller. Both bits may be cleared simultaneously.

	15–2	1	0
Field	—	REF	CAP
Reset	0000_0000_0000_0000		
R/W	Read/Write		
Addr	MBAR + 0x210 (TER0); 0x230 (TER1); 0x250 (TER2); 0x270 (TER3)		

Figure 15-6. Timer Event Registers (TER0–TER3)

Table 15-2 describes TER*n* fields.

Table 15-2. TER*n* Field Descriptions

Bits	Name	Description
15–2	—	Reserved, should be cleared.
1	REF	Output reference event. 0 The counter has not reached the TRR value 1 The counter reached the TRR value. TMR[ORI] is used to enable the interrupt request caused by this event. Write a 1 to this bit to clear the event condition.
0	CAP	Capture event. 0 The counter value has not been latched into the TCAP. 1 The counter value is latched in the TCAP. TMR[CE] is used to enable capture and the interrupt request caused by this event. Write a 1 to this bit to clear the event condition.

17.2.3 Port C Control Register

There is no port C control register. Port C is enabled only when the external data bus is 16 bits wide. This is done by holding QSPI_DOUT/WSEL high during reset. When QSPI_DOUT/WSEL is low during reset, the external data bus is 32 bits wide and port C is unavailable.

17.2.4 Port D Control Register (PDCNT)

PDCNT, shown in Table 17-8, is used to configure pins that have multiple functions but no associated GPIO capability. Port D has no data register nor data direction register.

	31–16
Field	—
Reset	—
R/W	—

	15–14	13–12	11–10	9–8	7–6	5–4	3–2	1–0
Field	PDCNT7	PDCNT6	PDCNT5	PDCNT4	PDCNT3	PDCNT2	PDCNT1	PDCNT0
Reset	0000_0000_0000_0000							
R/W	Read/Write							
Addr	MBAR + 0x0098							

Figure 17-3. Port D Control Register (PDCNT)

Table 17-7 describes PDCNT fields. Table 17-8 provides the same information organized by function.

Table 17-7. PDCNT Field Descriptions

Bits	Name	Description
31–16	—	Reserved
15–14	PDCNT7	Configure pin K6. 00 High impedance 01 PWM_OUT2 10 TIN1 11 Reserved
13–12	PDCNT6	Configure pin P5. 00 High impedance 01 PWM_OUT1 10 TOUT1 11 Reserved
11–10	PDCNT5	Configure pin P2. 00 High impedance 01 Reserved 10 DIN3 11 $\overline{\text{INT4}}$
9–8	PDCNT4	Configure pin K1. 00 High impedance 01 DOUT0 10 URT1_TxD 11 Reserved

Table 19-1. Signal Descriptions Sorted by Function (Sheet 4 of 8)

Configured by (see notes)[1]	Pin Functions				Description	Map BGA Pin	I/O	Drive (mA)	Cpf
	0 (Reset)	1	2	3					
	E_MDIO	—	—	—	Management channel serial data (100 base-T only)	N10	I/O	2	
	E_RxCLK	—	—	—	Ethernet Rx clock	N7	I		
	E_RxD0	—	—	—	Ethernet Rx data	P7	I		
	E_RxDV	—	—	—	Ethernet Rx data valid	M7	I		
	E_Tx CLK	—	—	—	Ethernet Tx clock	L7	I		
	E_TxD0	—	—	—	Ethernet Tx data	N6	O	4	30
	E_TxEN	—	—	—	Ethernet Tx enable	P8	O	2	30
	E_TxER	—	—	—	Transmit error (100 base-T Ethernet only)	M10	O	2	30
	FSC1/FSR1/ DFSC1	—	—	—	PLIC port 1 IDL FSR/GCI FSC1/Generated frame sync 1 Out	L4	I/O	2	30
	GND	Ground	—	—		E[7,8] F[7,8] G[6–9] H[6–9] J[7,8]			
Port D Cntl Reg[3]	High Z	DCL0	URT1_CLK	—	Port 0 data clock/UART1 baud clock	J4	I		
Port D Cntl Reg[3]	High Z	DIN0	URT1_RxD	—	IDL/GCI data in/UART1 Rx data	K1	I		
Port D Cntl Reg[3]	High Z	–	$\overline{\text{URT1\_CTS}}$	QSPI_ CS2	UART1 CTS/QSPI_CS2	K2	I/O	2	30
Port D Cntl Reg[3]	High Z	–	URT1_RTS	INT5	UART1 RTS/$\overline{\text{INT5}}$	K3	I/O	2	30
Port D Cntl Reg[3]	High Z	DOUT0	URT1_TxD	—	IDL-GCI data Out/UART1 Tx data	K4	O	2	30
Port D Cntl Reg[3]	High Z	–	DIN3	INT4	Interrupt 4 input/PLIC port 3 data input	P2	I		
Port D Cntl Reg[3]	High Z	PWM_ OUT1	TOUT1	—	PWM output compare 1 /Timer 1 output compare	P5	O	4	30
Port D Cntl Reg[3]	High Z	PWM_ OUT2	TIN1	—	PWM output compare 2 /Timer 1 input	K6	I/O	4	30
	$\overline{\text{INT1}}$/ USB_WOR	—	—	—	Interrupt input 1/USB wake-on-ring	M4	I		
	INT2	—	—	—	Interrupt input 1	P3	I		
	INT3	—	—	—	Interrupt input 3	N3	I		

Table 19-1. Signal Descriptions Sorted by Function (Sheet 7 of 8)

Configured by (see notes)[1]	Pin Functions				Description	Map BGA Pin	I/O	Drive (mA)	Cpf
	0 (Reset)	1	2	3					
	PST3	—	—	—	Internal processor status 3	D3	O	4	30
	PWM_OUT0	—	—	—	PWM output compare 0	N5	O	4	30
	QSPI_CLK/ BUSW1	—	—	—	QSPI serial clock/CS0 bus width bit 1	L5	O	4	30
	QSPI_CS0/ BUSW0	—	—	—	QSPI peripheral chip select 0/$\overline{CS0}$ bus width bit 0	M5	O	2	30
	QSPI_Din	—	—	—	QSPI data input	P4	I		
	QSPI_Dout/ WSEL	—	—	—	QSPI data output/Bus width selection	N4	I/O	4	30
	R/$\overline{W}$	—	—	—	Read/Write	P14	O	10	30
	RAS0	—	—	—	SDRAM row select strobe	A10	O	10	30
	RSTI	—	—	—	Device reset	M12	I		
	RSTO	—	—	—	Reset output strobe	F4	O	4	30
	SDBA0	—	—	—	SDRAM bank 0 select	J14	O	10	30
	SDBA1	—	—	—	SDRAM bank 1 select	H12	O	10	30
	SDCLK	—	—	—	SDRAM (bus) clock, Same frequency as CPU clock	E14	O	10	30
	SDCLKE	—	—	—	SDRAM clock enable	D13	O	10	30
	$\overline{SDCS}$/ $\overline{CS7}$	—	—	—	SDRAM chip select/$\overline{CS7}$	B10	O	10	30
	SDWE	—	—	—	SDRAM write enable	B9	O	10	30
	BYPASS	—	—	—	Bypass internal test mode	M13	O	4	30
MTMOD[4]	TCK	PSTCLK	—	—	JTAG test clock in/ BDM PSTCLK output	C4	I/O	4	30
MTMOD[4]	TDI	DSI	—	—	JTAG test data in/BDM data in	A4	I		
MTMOD[4]	TDO	DSO	—	—	JTAG test data out /BDM data out	D5	O	4	30
	TEA	—	—	—	BDM debug transfer error acknowledge	A3	I		
	TEST	—	—	—	Device test mode enable	E6	I		
	TIN0	—	—	—	Timer 0 input	L6	I		
MTMOD[4]	TMS	BKPT	—	—	JTAG test mode/BDM select breakpoint input	B4	I		

21.4 Boundary Scan Register

The boundary scan register contains bits for all device signal and clock pins and associated control signals. Bidirectional pins include a single scan bit for data (IO.Cell) as shown in Figure 21-6. These bits are controlled by an enable cell, shown in Figure 21-5. The control bit value determines whether the bidirectional pin is an input or an output. One or more bidirectional data bits can be serially connected to a control bit as shown in Figure 21-7. Note that when bidirectional data bits are sampled, bit data can be interpreted only after examining the I/O control bit to determine pin direction.

Open-drain bidirectional bits require separate input and output cells as no direction control is available from which to determine signal direction. Programmable open-drain signals also have an enable cell (XXX.de) to select whether the pin is open drain or push-pull. Signals with pull-up or pull-down resistors have an associated enable cell (XXX.pu); one enable cell can control multiple resistors.

Figure 21-3 to Figure 21-8 show the four MCF5272 cell types.

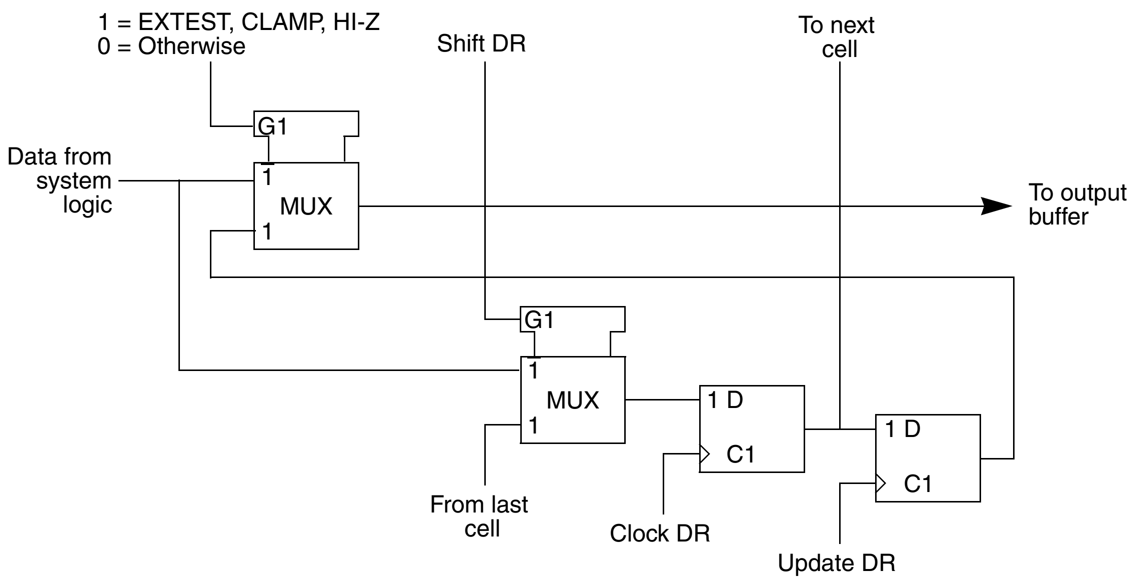

Figure 21-3. Output Cell (O.Cell) (BC–1)

23.6.2 MII Transmit Signal Timing (E_TxD[3:0], E_TxEN, E_TxER, E_TxCLK)

Table 23-12 lists MII transmit channel timings.

The transmitter functions correctly up to a E_TxCLK maximum frequency of 25 MHz +1%. There is no minimum frequency requirement. In addition, the processor clock frequency must exceed twice the E_TxCLK frequency.

The transmit outputs (E_TxD[3:0], E_TxEN, E_TxER) can be programmed to transition from either the rising or falling edge of E_TxCLK, and the timing is the same in either case. This options allows the use of non-compliant MII PHYs.

Refer to the Ethernet chapter for details of this option and how to enable it.

Table 23-12. MII Transmit Signal Timing

Num	Characteristic[1]	Min	Max	Unit
M5	E_TxCLK to E_TxD[3:0], E_TxEN, E_TxER invalid	5	—	nS
M6	E_TxCLK to E_TxD[3:0], E_TxEN, E_TxER valid	—	25	nS
M7	E_TxCLK pulse-width high	35%	65%	E_TxCLK period
M8	E_TxCLK pulse-width low	35%	65%	E_TxCLK period

[1] E_TxCLK, ETxD0, and E_TxEN have the same timing in 10 Mbit 7-wire interface mode.

Figure 23-12 shows MII transmit signal timings listed in Table 23-12.

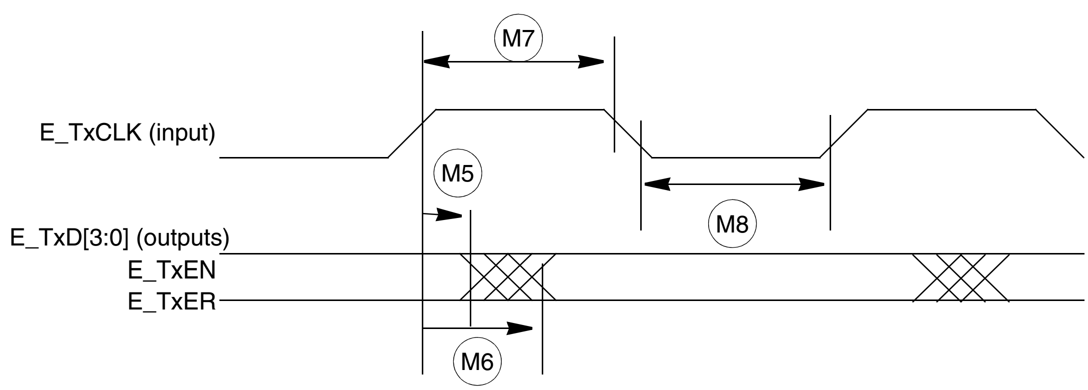

Figure 23-12. MII Transmit Signal Timing Diagram

Table A-10. UART0 Module Memory Map

MBAR Offset	[31:24]	[23:16]	[15:8]	[7:0]
0x0100	UART0 Mode Register 1/2 (U0MR1/U0MR2)	Reserved		
0x0104	UART0 Status (U0SR)	Reserved		
0x0104	UART0 Clock Select Register (U0CSR)	Reserved		
0x0108	UART0 Command Register (U0CR)	Reserved		
0x010C	UART0 Receive Buffer (U0RxB)	Reserved		
0x010C	UART0 Transmit Buffer (U0TxB)	Reserved		
0x0110	UART0 CTS Change Register (U0CCR)	Reserved		
0x0110	UART0 Auxiliary Control Register (U0ACR)	Reserved		
0x0114	UART0 Interrupt Status Register (U0ISR)	Reserved		
0x0114	UART0 Interrupt Mask Register (U0IMR)	Reserved		
0x0118	UART0 Baud Prescaler MSB (U0BG1)	Reserved		
0x011C	UART0 Baud Prescaler LSB (U0BG2)	Reserved		
0x0120	UART0 AutoBaud MSB Register (U0ABR1)	Reserved		
0x0124	UART0 AutoBaud LSB Register (U0ABR2)	Reserved		
0x0128	UART0 TxFIFO Control/Status Register (U0TxFCSR)	Reserved		
0x012C	UART0 RxFIFO Control/Status Register (U0RxFCSR)	Reserved		
0x130	UART0 Fractional Precision Divider Control Registers (UFPDn)	Reserved		
0x0134	UART0 CTS Unlatched Input (U0IP)	Reserved		
0x0138	UART0 RTS O/P Bit Set Command Register (U0OP1)	Reserved		
0x013C	UART0 RTS O/P Bit Reset Command Register (U0OP0)	Reserved		

Table A-14. PLIC Module Memory Map

MBAR Offset	[31:24]	[23:16]	[15:8]	[7:0]
0x0300	Port0 B1 Data Receive (P0B1RR)			
0x0304	Port1 B1 Data Receive (P1B1RR)			
0x0308	Port2 B1 Data Receive (P2B1RR)			
0x030C	Port3 B1 Data Receive (P3B1RR)			
0x0310	Port0 B2 Data Receive (P0B2RR)			
0x0314	Port1 B2 Data Receive (P1B2RR)			
0x0318	Port2 B2 Data Receive (P2B2RR)			
0x031C	Port3 B2 Data Receive (P3B2RR)			
0x0320	Port 0 D Data Receive (P0DRR)	Port 1 D Data Receive (P1DRR)	Port 2 D Data Receive (P2DRR)	Port 3 D Data Receive (P3DRR)
0x0328	Port0 B1 Data Transmit (P0B1TR)			
0x032C	Port1 B1 Data Transmit (P1B1TR)			
0x0330	Port2 B1 Data Transmit (P2B1TR)			
0x0334	Port3 B1 Data Transmit (P3B1TR)			
0x0338	Port0 B2 Data Transmit (P0B2TR)			
0x033C	Port1 B2 Data Transmit (P1B2TR)			
0x0340	Port2 B2 Data Transmit (P2B2TR)			
0x0344	Port3 B2 Data Transmit (P3B2TR)			
0x0348	Port 0 D Data Transmit (P0DTR)	Port 1 D Data Transmit (P1DTR)	Port 2 D Data Transmit (P2DTR)	Port 3 D Data Transmit (P3DTR)
0x0350	Port0 GCI/IDL Configuration Register (P0CR)		Port1 GCI/IDL Configuration Register (P1CR)	
0x0354	Port2 GCI/IDL Configuration Register (P2CR)		Port3 GCI/IDL Configuration Register (P3CR)	
0x0358	Port0 Interrupt Configuration Register (P0ICR)		Port1 Interrupt Configuration Register (P1ICR)	
0x035C	Port2 Interrupt Configuration Register (P2ICR)		Port3 Interrupt Configuration Register (P3ICR)	
0x0360	Port0 GCI Monitor RX (P0GMR)		Port1 GCI Monitor RX (P1GMR)	
0x0364	Port2 GCI Monitor RX (P2GMR)		Port3 GCI Monitor RX (P3GMR)	
0x0368	Port0 GCI Monitor TX (P0GMT)		Port1 GCI Monitor TX (P1GMT)	
0x036C	Port2 GCI Monitor TX (P2GMT)		Port3 GCI Monitor TX (P3GMT)	
0x0370	Reserved	GCI Monitor TX Status (PGMTS)	GCI Monitor TX abort (PGMTA)	Reserved
0x0374	Port0 GCI C/I RX (P0GCIR)	Port1 GCI C/I RX (P1GCIR)	Port2 GCI C/I RX (P2GCIR)	Port3 GCI C/I RX (P3GCIR)
0x0378	Port0 GCI C/I TX (P0GCIT)	Port1 GCI C/I TX (P1GCIT)	Port2 GCI C/I TX (P2GCIT)	Port3 GCI C/I TX (P3GCIT)
0x037C	Reserved			GCI C/I TX Status (PGCITSR)
0x0383	Reserved			GCI D-Channel Status (PDCSR)
0x0384	Port0 Periodic Status (P0PSR)		Port1 Periodic Status (P1PSR)	
0x0388	Port2 Periodic Status (P2PSR)		Port3 Periodic Status (P3PSR)	

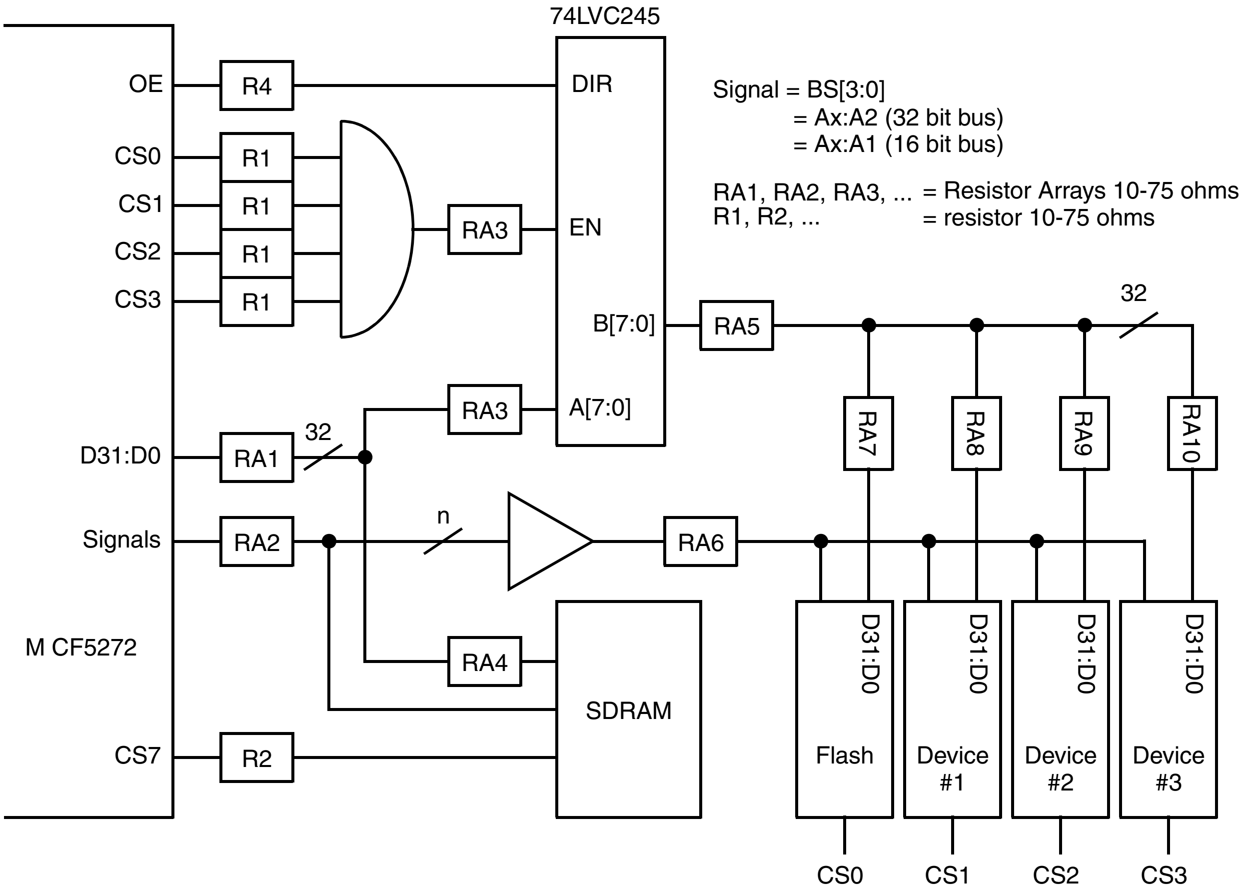

Figure B-1. Buffering and Termination