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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Fixed Point
Interface	Host Interface, SSI, SCI
Clock Rate	100MHz
Non-Volatile Memory	ROM (576B)
On-Chip RAM	24kB
Voltage - I/O	3.30V
Voltage - Core	3.30V
Operating Temperature	-40°C ~ 105°C (TJ)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spakdsp303ag100

Table 3-2. DSP56303 TQFP Signal Identification by Name (Continued)

Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.
$\overline{RAS0}$	70	SRD1	1	V_{CCC}	57
$\overline{RAS1}$	69	STD0	10	V_{CCC}	65
$\overline{RAS2}$	51	STD1	2	V_{CCD}	103
$\overline{RAS3}$	50	$\overline{TA}$	62	V_{CCD}	111
$\overline{RD}$	68	TCK	141	V_{CCD}	119
$\overline{RESET}$	44	TDI	140	V_{CCD}	129
RXD	13	TDO	139	V_{CCH}	38
SC00	12	TIO0	29	V_{CCP}	45
SC01	4	TIO1	28	V_{CCQ}	18
SC02	3	TIO2	27	V_{CCQ}	56
SC10	11	TMS	142	V_{CCQ}	91
SC11	144	$\overline{TRST}$	138	V_{CCQ}	126
SC12	143	TXD	14	V_{CCS}	8
SCK0	17	V_{CCA}	74	V_{CCS}	25
SCK1	16	V_{CCA}	80	$\overline{WR}$	67
SCLK	15	V_{CCA}	86	XTAL	53
SRD0	7	V_{CCA}	95		

Table 3-3. DSP56303 MAP-BGA Signal Identification by Pin Number (Continued)

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
L14	A4	N2	H7, HAD7, or PB7	P4	H1, HAD1, or PB1
M1	HA1, HA8, or PB9	N3	H4, HAD4, or PB4	P5	PCAP
M2	HA2, HA9, or PB10	N4	H2, HAD2, or PB2	P6	GND_{P1}
M3	HA0, $\overline{HAS}$/HAS, or PB8	N5	$\overline{RESET}$	P7	AA2/$\overline{RAS2}$
M4	V_{CCH}	N6	GND_P	P8	XTAL
M5	H0, HAD0, or PB0	N7	AA3/$\overline{RAS3}$	P9	V_{CCC}
M6	V_{CCP}	N8	$\overline{CAS}$	P10	$\overline{TA}$
M7	NC	N9	V_{CCQ}	P11	$\overline{BB}$
M8	EXTAL	N10	BCLK	P12	AA1/$\overline{RAS1}$
M9	CLKOUT	N11	$\overline{BR}$	P13	$\overline{BG}$
M10	$\overline{BCLK}$	N12	V_{CCC}	P14	NC
M11	$\overline{WR}$	N13	AA0/$\overline{RAS0}$		
M12	$\overline{RD}$	N14	A0		

Notes: Signal names are based on configured functionality. Most connections supply a single signal. Some connections provide a signal with dual functionality, such as the MODx/IRQx pins that select an operating mode after $\overline{RESET}$ is deasserted but act as interrupt lines during operation. Some signals have configurable polarity; these names are shown with and without overbars, such as $\overline{HAS}$/HAS. Some connections have two or more configurable functions; names assigned to these connections indicate the function for a specific configuration. For example, connection N2 is data line H7 in non-multiplexed bus mode, data/address line HAD7 in multiplexed bus mode, or GPIO line PB7 when the GPIO function is enabled for this pin. Unlike in the TQFP package, most of the GND pins are connected internally in the center of the connection array and act as heat sink for the chip. Therefore, except for GND_P and GND_{P1} that support the PLL, other GND signals do not support individual subsystems in the chip.

Table 3-4. DSP56303 MAP-BGA Signal Identification by Name (Continued)

Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.
GND	F8	GND	J9	H4	N3
GND	F9	GND	J10	H5	P2
GND	F10	GND	J11	H6	N1
GND	F11	GND	K4	H7	N2
GND	G4	GND	K5	HA0	M3
GND	G5	GND	K6	HA1	M1
GND	G6	GND	K7	HA10	L1
GND	G7	GND	K8	HA2	M2
GND	G8	GND	K9	HA8	M1
GND	G9	GND	K10	HA9	M2
GND	G10	GND	K11	$\overline{\text{HACK}}$/HACK	J1
GND	G11	GND	L4	HAD0	M5
GND	H4	GND	L5	HAD1	P4
GND	H5	GND	L6	HAD2	N4
GND	H6	GND	L7	HAD3	P3
GND	H7	GND	L8	HAD4	N3
GND	H8	GND	L9	HAD5	P2
GND	H9	GND	L10	HAD6	N1
GND	H10	GND	L11	HAD7	N2
GND	H11	GND_P	N6	$\overline{\text{HAS}}$/HAS	M3
GND	J4	GND_{P1}	P6	$\overline{\text{HCS}}$/HCS	L1
GND	J5	H0	M5	$\overline{\text{HDS}}$/HDS	J3
GND	J6	H1	P4	$\overline{\text{HRD}}$/HRD	J2
GND	J7	H2	N4	$\overline{\text{HREQ}}$/HREQ	K2
GND	J8	H3	P3	$\overline{\text{HRRQ}}$/HRRQ	J1

Table 3-4. DSP56303 MAP-BGA Signal Identification by Name (Continued)

Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.
TDO	A4	V_{CCA}	K12	V_{CCP}	M6
TIO0	L3	V_{CCA}	L12	V_{CCQ}	C7
TIO1	L2	V_{CCC}	N12	V_{CCQ}	G13
TIO2	K3	V_{CCC}	P9	V_{CCQ}	H2
TMS	A3	V_{CCD}	A7	V_{CCQ}	N9
$\overline{TRST}$	B4	V_{CCD}	C9	V_{CCS}	E2
TXD	G3	V_{CCD}	C11	V_{CCS}	K1
V_{CCA}	F12	V_{CCD}	D14	$\overline{WR}$	M11
V_{CCA}	H12	V_{CCH}	M4	XTAL	P8

A complicating factor is the existence of three common ways to determine the junction-to-case thermal resistance in plastic packages.

To minimize temperature variation across the surface, the thermal resistance is measured from the junction to the outside surface of the package (case) closest to the chip mounting area when that surface has a proper heat sink.

To define a value approximately equal to a junction-to-board thermal resistance, the thermal resistance is measured from the junction to the point at which the leads attach to the case.

If the temperature of the package case (T_T) is determined by a thermocouple, thermal resistance is computed from the value obtained by the equation $(T_J \quad T_T)/P_D$.

As noted earlier, the junction-to-case thermal resistances quoted in this data sheet are determined using the first definition. From a practical standpoint, that value is also suitable to determine the junction temperature from a case thermocouple reading in forced convection environments. In natural convection, the use of the junction-to-case thermal resistance to estimate junction temperature from a thermocouple reading on the case of the package will yield an estimate of a junction temperature slightly higher than actual temperature. Hence, the new thermal metric, thermal characterization parameter or Ψ_{JT}, has been defined to be $(T_J \quad T_T)/P_D$. This value gives a better estimate of the junction temperature in natural convection when the surface temperature of the package is used. Remember that surface temperature readings of packages are subject to significant errors caused by inadequate attachment of the sensor to the surface and to errors caused by heat loss to the sensor. The recommended technique is to attach a 40-gauge thermocouple wire and bead to the top center of the package with thermally conductive epoxy.

4.2 Electrical Design Considerations

CAUTION

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, normal precautions are advised to avoid application of any voltages higher than maximum rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for example, either GND or V_{CC}).

4.4 PLL Performance Issues

The following explanations should be considered as general observations on expected PLL behavior. There is no test that replicates these exact numbers. These observations were measured on a limited number of parts and were not verified over the entire temperature and voltage ranges.

4.4.1 Phase Skew Performance

The phase skew of the PLL is defined as the time difference between the falling edges of EXTAL and CLKOUT for a given capacitive load on CLKOUT, over the entire process, temperature and voltage ranges. As defined in **Figure 2-2**, External Clock Timing on page 2-5 for input frequencies greater than 15 MHz and the MF ≤ 4, this skew is greater than or equal to 0.0 ns and less than 1.8 ns; otherwise, this skew is not guaranteed. However, for MF < 10 and input frequencies greater than 10 MHz, this skew is between –1.4 ns and +3.2 ns.

4.4.2 Phase Jitter Performance

The phase jitter of the PLL is defined as the variations in the skew between the falling edges of EXTAL and CLKOUT for a given device in specific temperature, voltage, input frequency, MF, and capacitive load on CLKOUT. These variations are a result of the PLL locking mechanism. For input frequencies greater than 15 MHz and MF ≤ 4, this jitter is less than ±0.6 ns; otherwise, this jitter is not guaranteed. However, for MF < 10 and input frequencies greater than 10 MHz, this jitter is less than ±2 ns.

4.4.3 Frequency Jitter Performance

The frequency jitter of the PLL is defined as the variation of the frequency of CLKOUT. For small MF (MF < 10) this jitter is smaller than 0.5 percent. For mid-range MF (10 < MF < 500) this jitter is between 0.5 percent and approximately 2 percent. For large MF (MF > 500), the frequency jitter is 2 3 percent.

4.5 Input (EXTAL) Jitter Requirements

The allowed jitter on the frequency of EXTAL is 0.5 percent. If the rate of change of the frequency of EXTAL is slow (that is, it does not jump between the minimum and maximum values in one cycle) or the frequency of the jitter is fast (that is, it does not stay at an extreme value for a long time), then the allowed jitter can be 2 percent. The phase and frequency jitter performance results are valid only if the input jitter is less than the prescribed values.

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M_TLR0 EQU  $FFFF8E      ; TIMER0 Load Reg
M_TCPR0 EQU $FFFF8D        ; TIMER0 Compare Register
M_TCR0 EQU  $FFFF8C     ; TIMER0 Count Register

;       Register Addresses Of TIMER1

M_TCSR1 EQU $FFFF8B       ; TIMER1 Control/Status Register
M_TLR1 EQU  $FFFF8A      ; TIMER1 Load Reg
M_TCPR1 EQU $FFFF89        ; TIMER1 Compare Register
M_TCR1 EQU  $FFFF88      ; TIMER1 Count Register


;       Register Addresses Of TIMER2

M_TCSR2 EQU $FFFF87       ; TIMER2 Control/Status Register
M_TLR2 EQU  $FFFF86      ; TIMER2 Load Reg
M_TCPR2 EQU $FFFF85       ; TIMER2 Compare Register
M_TCR2 EQU  $FFFF84      ; TIMER2 Count Register
M_TPLR EQU  $FFFF83      ; TIMER Prescaler Load Register
M_TPCR EQU  $FFFF82      ; TIMER Prescalar Count Register


;       Timer Control/Status Register Bit Flags

M_TE EQU 0                  ; Timer Enable
M_TOIE EQU 1                ; Timer Overflow Interrupt Enable
M_TCIE EQU 2                ; Timer Compare Interrupt Enable
M_TC EQU $F0                ; Timer Control Mask (TC0-TC3)
M_INV EQU 8                 ; Inverter Bit
M_TRM EQU 9                 ; Timer Restart Mode
M_DIR EQU 11                ; Direction Bit
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