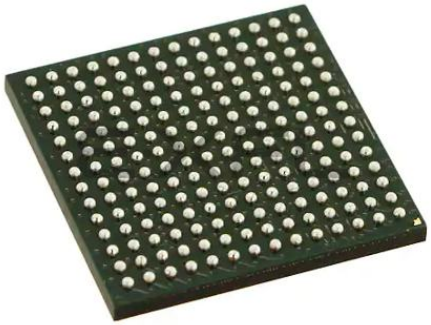

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Fixed Point
Interface	Host Interface, SSI, SCI
Clock Rate	100MHz
Non-Volatile Memory	ROM (576B)
On-Chip RAM	24kB
Voltage - I/O	3.30V
Voltage - Core	3.30V
Operating Temperature	-40°C ~ 105°C (TJ)
Mounting Type	Surface Mount
Package / Case	196-LBGA
Supplier Device Package	196-LBGA (15x15)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spakdsp303vf100

1.1 Signal Groupings

The DSP56303 input and output signals are organized into functional groups as shown in **Table 1-1**. **Figure 1-1** diagrams the DSP56303 signals by functional group. The remainder of this chapter describes the signal pins in each functional group.

Table 1-1. DSP56303 Functional Signal Groupings

Functional Group		Number of Signals	
		TQFP	MAP-BGA
Power (V_{CC})		18	18
Ground (GND)		19	66
Clock		2	2
PLL		3	3
Address bus	Port A[1]	18	18
Data bus		24	24
Bus control		13	13
Interrupt and mode control		5	5
Host interface (HI08)	Port B[2]	16	16
Enhanced synchronous serial interface (ESSI)	Ports C and D[3]	12	12
Serial communication interface (SCI)	Port E[4]	3	3
Timer		3	3
OnCE/JTAG Port		6	6

Notes:
1. Port A signals define the external memory interface port, including the external address bus, data bus, and control signals.
2. Port B signals are the HI08 port signals multiplexed with the GPIO signals.
3. Port C and D signals are the two ESSI port signals multiplexed with the GPIO signals.
4. Port E signals are the SCI port signals multiplexed with the GPIO signals.
5. There are 2 signal connections in the TQFP package and 7 signal connections in the MAP-BGA package that are not used. These are designated as no connect (NC) in the package description (see **Chapter 3**).

Note: This chapter refers to a number of configuration registers used to select individual multiplexed signal functionality. Refer to the *DSP56303 User's Manual* for details on these configuration registers.

Table 1-11. Host Interface (Continued)

Signal Name	Type	State During Reset[1,2]	Signal Description
HA0	Input	Ignored Input	**Host Address Input 0**—When the HI08 is programmed to interface with a nonmultiplexed host bus and the HI function is selected, this signal is line 0 of the host address input bus.
$\overline{\text{HAS}}$/HAS	Input		**Host Address Strobe—**When the HI08 is programmed to interface with a multiplexed host bus and the HI function is selected, this signal is the host address strobe (HAS) Schmitt-trigger input. The polarity of the address strobe is programmable but is configured active-low ($\overline{\text{HAS}}$) following reset.
PB8	Input or Output		**Port B 8**—When the HI08 is configured as GPIO through the HI08 Port Control Register, this signal is individually programmed as an input or output through the HI08 Data Direction Register.
HA1	Input	Ignored Input	**Host Address Input 1**—When the HI08 is programmed to interface with a nonmultiplexed host bus and the HI function is selected, this signal is line 1 of the host address (HA1) input bus.
HA8	Input		**Host Address 8**—When the HI08 is programmed to interface with a multiplexed host bus and the HI function is selected, this signal is line 8 of the host address (HA8) input bus.
PB9	Input or Output		**Port B 9**—When the HI08 is configured as GPIO through the HI08 Port Control Register, this signal is individually programmed as an input or output through the HI08 Data Direction Register.
HA2	Input	Ignored Input	**Host Address Input 2**—When the HI08 is programmed to interface with a nonmultiplexed host bus and the HI function is selected, this signal is line 2 of the host address (HA2) input bus.
HA9	Input		**Host Address 9**—When the HI08 is programmed to interface with a multiplexed host bus and the HI function is selected, this signal is line 9 of the host address (HA9) input bus.
PB10	Input or Output		**Port B 10**—When the HI08 is configured as GPIO through the HI08 Port Control Register, this signal is individually programmed as an input or output through the HI08 Data Direction Register.
$\overline{\text{HCS}}$/HCS	Input	Ignored Input	**Host Chip Select**—When the HI08 is programmed to interface with a nonmultiplexed host bus and the HI function is selected, this signal is the host chip select (HCS) input. The polarity of the chip select is programmable but is configured active-low ($\overline{\text{HCS}}$) after reset.
HA10	Input		**Host Address 10**—When the HI08 is programmed to interface with a multiplexed host bus and the HI function is selected, this signal is line 10 of the host address (HA10) input bus.
PB13	Input or Output		**Port B 13**—When the HI08 is configured as GPIO through the HI08 Port Control Register, this signal is individually programmed as an input or output through the HI08 Data Direction Register.

Table 1-13. Enhanced Serial Synchronous Interface 1 (Continued)

Signal Name	Type	State During Reset[1,2]	Signal Description
SC12	Input/Output	Ignored Input	**Serial Control Signal 2**—The frame sync for both the transmitter and receiver in synchronous mode and for the transmitter only in asynchronous mode. When configured as an output, this signal is the internally generated frame sync signal. When configured as an input, this signal receives an external frame sync signal for the transmitter (and the receiver in synchronous operation).
PD2	Input or Output		**Port D 2**—The default configuration following reset is GPIO input PD2. When configured as PD2, signal direction is controlled through the Port D Direction Register. The signal can be configured as an ESSI signal SC12 through the Port D Control Register.
SCK1	Input/Output	Ignored Input	**Serial Clock**—Provides the serial bit rate clock for the ESSI. The SCK1 is a clock input or output used by both the transmitter and receiver in synchronous modes or by the transmitter in asynchronous modes. Although an external serial clock can be independent of and asynchronous to the DSP system clock, it must exceed the minimum clock cycle time of 6T (that is, the system clock frequency must be at least three times the external ESSI clock frequency). The ESSI needs at least three DSP phases inside each half of the serial clock.
PD3	Input or Output		**Port D 3**—The default configuration following reset is GPIO input PD3. When configured as PD3, signal direction is controlled through the Port D Direction Register. The signal can be configured as an ESSI signal SCK1 through the Port D Control Register.
SRD1	Input	Ignored Input	**Serial Receive Data**—Receives serial data and transfers the data to the ESSI Receive Shift Register. SRD1 is an input when data is being received.
PD4	Input or Output		**Port D 4**—The default configuration following reset is GPIO input PD4. When configured as PD4, signal direction is controlled through the Port D Direction Register. The signal can be configured as an ESSI signal SRD1 through the Port D Control Register.
STD1	Output	Ignored Input	**Serial Transmit Data**—Transmits data from the Serial Transmit Shift Register. STD1 is an output when data is being transmitted.
PD5	Input or Output		**Port D 5**—The default configuration following reset is GPIO input PD5. When configured as PD5, signal direction is controlled through the Port D Direction Register. The signal can be configured as an ESSI signal STD1 through the Port D Control Register.

Notes:
1. In the Stop state, the signal maintains the last state as follows:
- If the last state is input, the signal is an ignored input.
- If the last state is output, the signal is tri-stated.

2. The Wait processing state does not affect the signal state.
3. All inputs are 5 V tolerant.

2.6 AC Electrical Characteristics

The timing waveforms shown in the AC electrical characteristics section are tested with a V_{IL} maximum of 0.3 V and a V_{IH} minimum of 2.4 V for all pins except EXTAL, which is tested using the input levels shown in Note 6 of the previous table. AC timing specifications, which are referenced to a device input signal, are measured in production with respect to the 50 percent point of the respective input signal transition. DSP56303 output levels are measured with the production test machine V_{OL} and V_{OH} reference levels set at 0.4 V and 2.4 V, respectively.

Note: Although the minimum value for the frequency of EXTAL is 0 MHz, the device AC test conditions are 15 MHz and rated speed.

2.6.1 Internal Clocks

Table 2-4. Internal Clocks, CLKOUT

Characteristics	Symbol	Expression[1, 2]		
		Min	Typ	Max
Internal operation frequency and CLKOUT with PLL enabled	f	—	(Ef × MF)/ (PDF × DF)	—
Internal operation frequency and CLKOUT with PLL disabled	f	—	Ef/2	—
Internal clock and CLKOUT high period • With PLL disabled • With PLL enabled and MF ≤ 4 • With PLL enabled and MF > 4	T_H	 — 0.49 × ET_C × PDF × DF/MF 0.47 × ET_C × PDF × DF/MF	 ET_C — —	 — 0.51 × ET_C × PDF × DF/MF 0.53 × ET_C × PDF × DF/MF
Internal clock and CLKOUT low period • With PLL disabled • With PLL enabled and MF ≤ 4 • With PLL enabled and MF > 4	T_L	 — 0.49 × ET_C × PDF × DF/MF 0.47 × ET_C × PDF × DF/MF	 ET_C — —	 — 0.51 × ET_C × PDF × DF/MF 0.53 × ET_C × PDF × DF/MF
Internal clock and CLKOUT cycle time with PLL enabled	T_C	—	ET_C × PDF × DF/MF	—
Internal clock and CLKOUT cycle time with PLL disabled	T_C	—	2 × ET_C	—
Instruction cycle time	I_{CYC}	—	T_C	—

Notes: **1.** DF = Division Factor; Ef = External frequency; ET_C = External clock cycle; MF = Multiplication Factor; PDF = Predivision Factor; T_C = internal clock cycle

2. See the PLL and Clock Generation section in the *DSP56300 Family Manual* for a detailed discussion of the PLL.

Table 2-7. Reset, Stop, Mode Select, and Interrupt Timing[6] (Continued)

No.	Characteristics	Expression	100 MHz		Unit
			Min	Max	

Notes:

1. When fast interrupts are used and $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$, $\overline{\text{IRQC}}$, and $\overline{\text{IRQD}}$ are defined as level-sensitive, timings 19 through 21 apply to prevent multiple interrupt service. To avoid these timing restrictions, the deasserted Edge-triggered mode is recommended when fast interrupts are used. Long interrupts are recommended for Level-sensitive mode.

2. This timing depends on several settings:
- For PLL disable, using internal oscillator (PLL Control Register (PCTL) Bit 16 = 0) and oscillator disabled during Stop (PCTL Bit 17 = 0), a stabilization delay is required to assure that the oscillator is stable before programs are executed. Resetting the Stop delay (Operating Mode Register Bit 6 = 0) provides the proper delay. While Operating Mode Register Bit 6 = 1 can be set, it is not recommended, and these specifications do not guarantee timings for that case.
- For PLL disable, using internal oscillator (PCTL Bit 16 = 0) and oscillator enabled during Stop (PCTL Bit 17=1), no stabilization delay is required and recovery is minimal (Operating Mode Register Bit 6 setting is ignored).
- For PLL disable, using external clock (PCTL Bit 16 = 1), no stabilization delay is required and recovery time is defined by the PCTL Bit 17 and Operating Mode Register Bit 6 settings.
- For PLL enable, if PCTL Bit 17 is 0, the PLL is shutdown during Stop. Recovering from Stop requires the PLL to get locked. The PLL lock procedure duration, PLL Lock Cycles (PLC), may be in the range of 0 to 1000 cycles. This procedure occurs in parallel with the stop delay counter, and stop recovery ends when the last of these two events occurs. The stop delay counter completes count or PLL lock procedure completion.
- PLC value for PLL disable is 0.
- The maximum value for ET_C is 4096 (maximum MF) divided by the desired internal frequency (that is, for 66 MHz it is 4096/66 MHz = 62 µs). During the stabilization period, T_C, T_H, and T_L is not constant, and their width may vary, so timing may vary as well.

3. Periodically sampled and not 100 percent tested.

4. Value depends on clock source:
- For an external clock generator, $\overline{\text{RESET}}$ duration is measured while $\overline{\text{RESET}}$ is asserted, V_{CC} is valid, and the EXTAL input is active and valid.
- For an internal oscillator, $\overline{\text{RESET}}$ duration is measured while $\overline{\text{RESET}}$ is asserted and V_{CC} is valid. The specified timing reflects the crystal oscillator stabilization time after power-up. This number is affected both by the specifications of the crystal and other components connected to the oscillator and reflects worst case conditions.
- When the V_{CC} is valid, but the other "required $\overline{\text{RESET}}$ duration" conditions (as specified above) have not been yet met, the device circuitry is in an uninitialized state that can result in significant power consumption and heat-up. Designs should minimize this state to the shortest possible duration.

5. If PLL does not lose lock.

6. V_{CC} = 3.3 V ± 0.3 V; T_J = –40°C to +100°C, C_L = 50 pF.

7. WS = number of wait states (measured in clock cycles, number of T_C).

8. Use the expression to compute a maximum value.

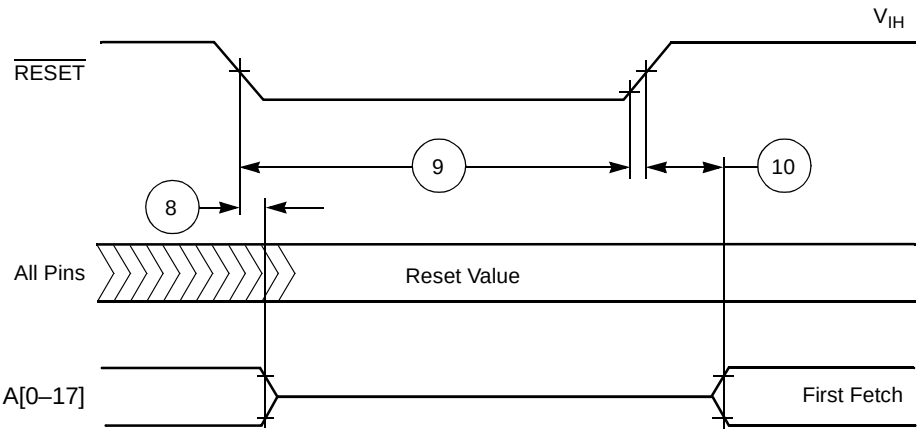
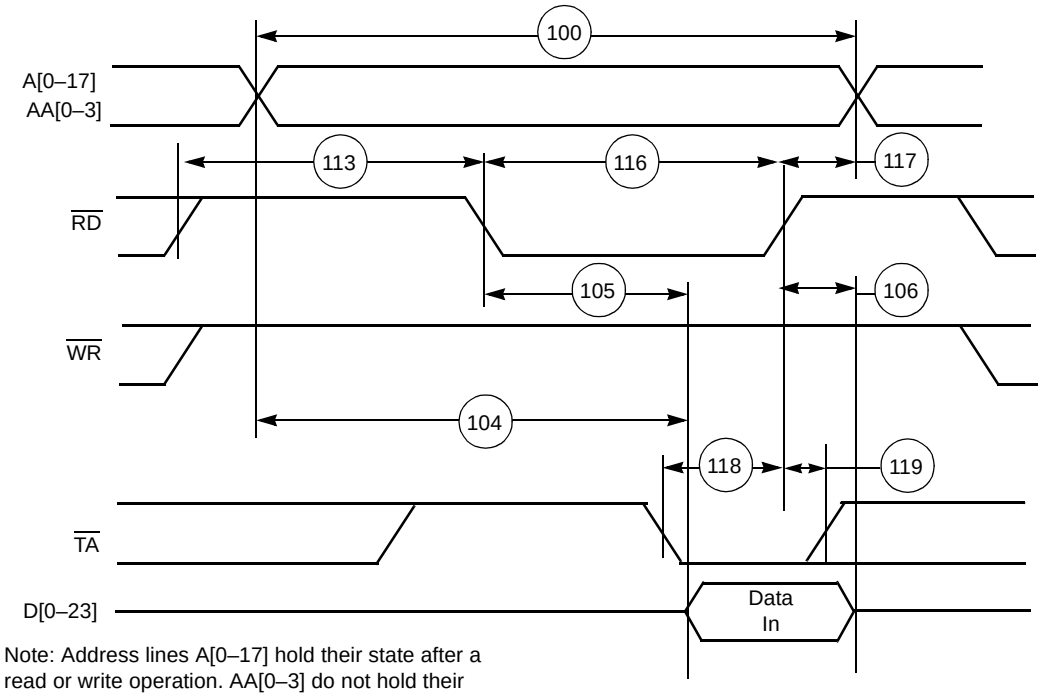
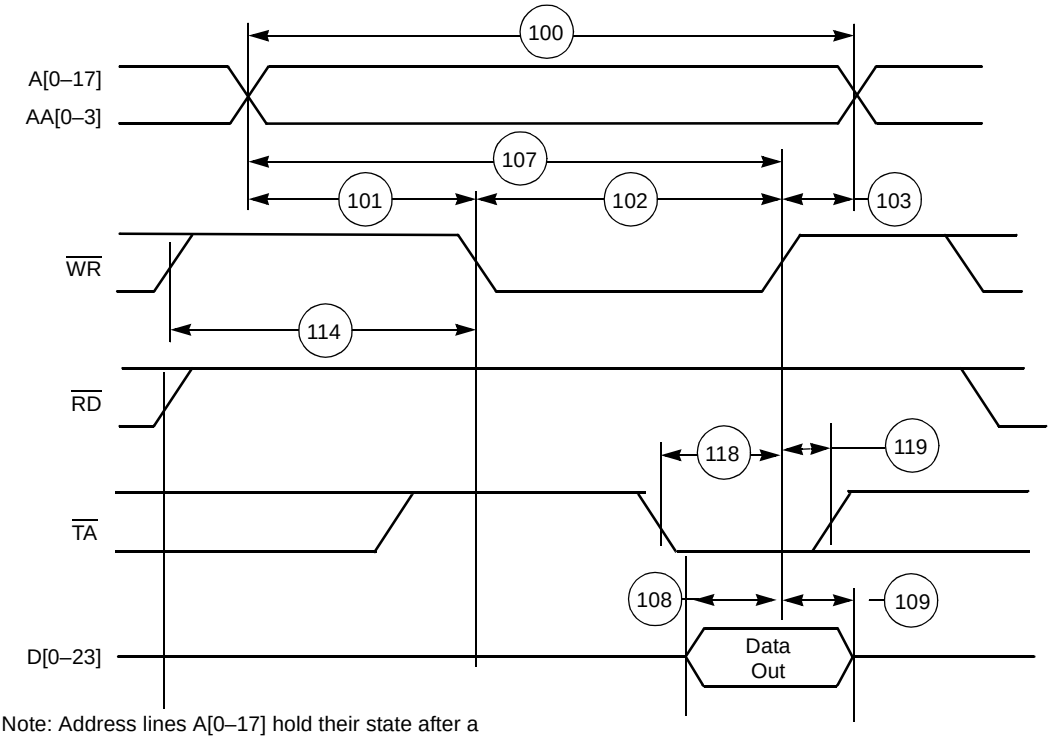


Figure 2-3. Reset Timing



Note: Address lines A[0–17] hold their state after a read or write operation. AA[0–3] do not hold their state after a read or write operation.

Figure 2-12. SRAM Read Access



Note: Address lines A[0–17] hold their state after a read or write operation. AA[0–3] do not hold their state after a read or write operation.

Figure 2-13. SRAM Write Access

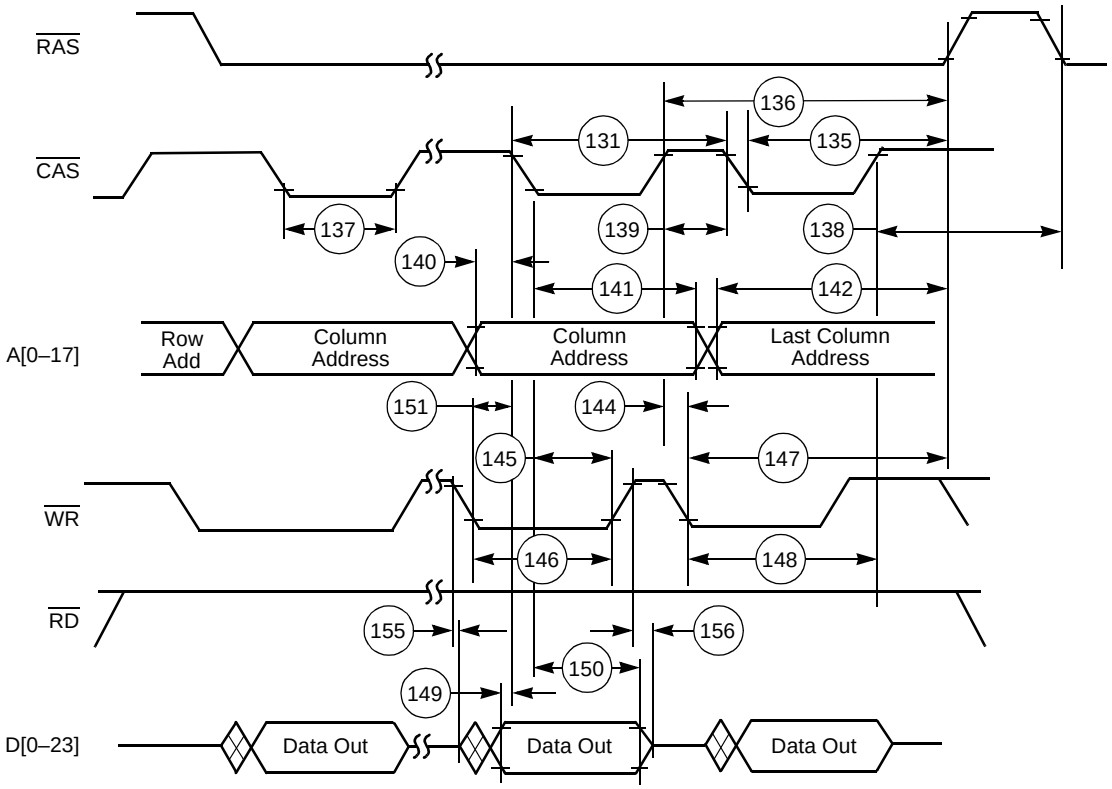


Figure 2-15. DRAM Page Mode Write Accesses

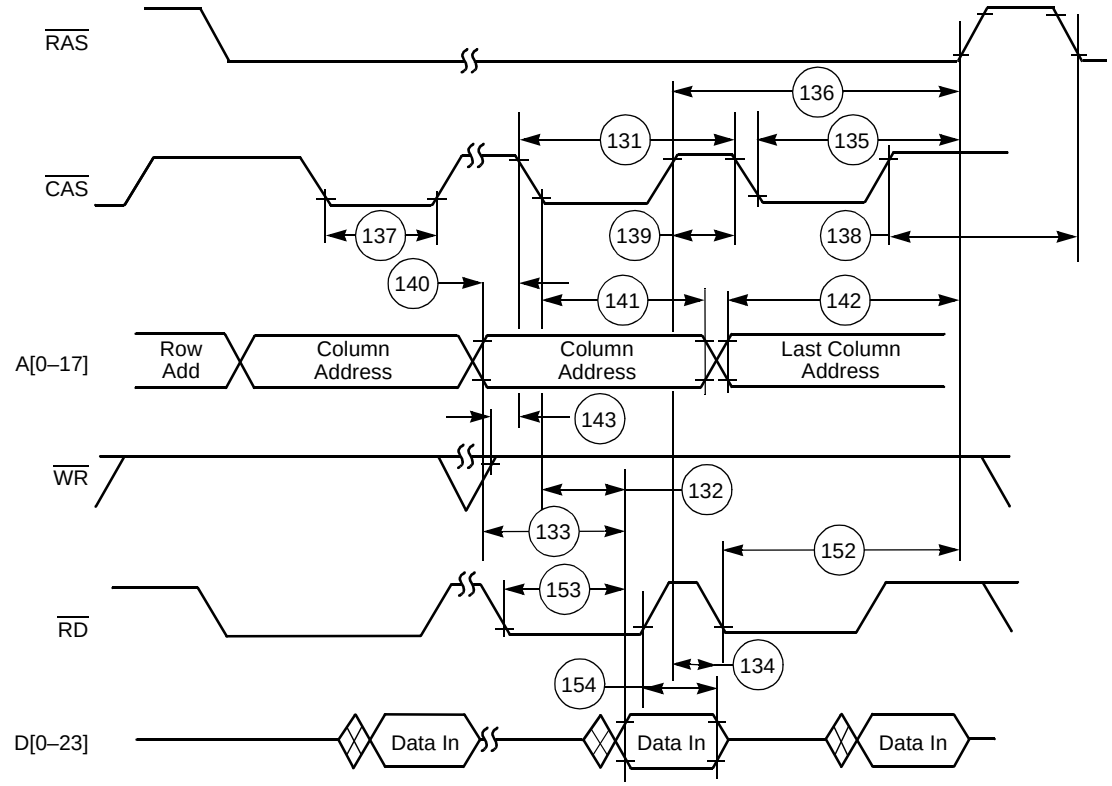


Figure 2-16. DRAM Page Mode Read Accesses

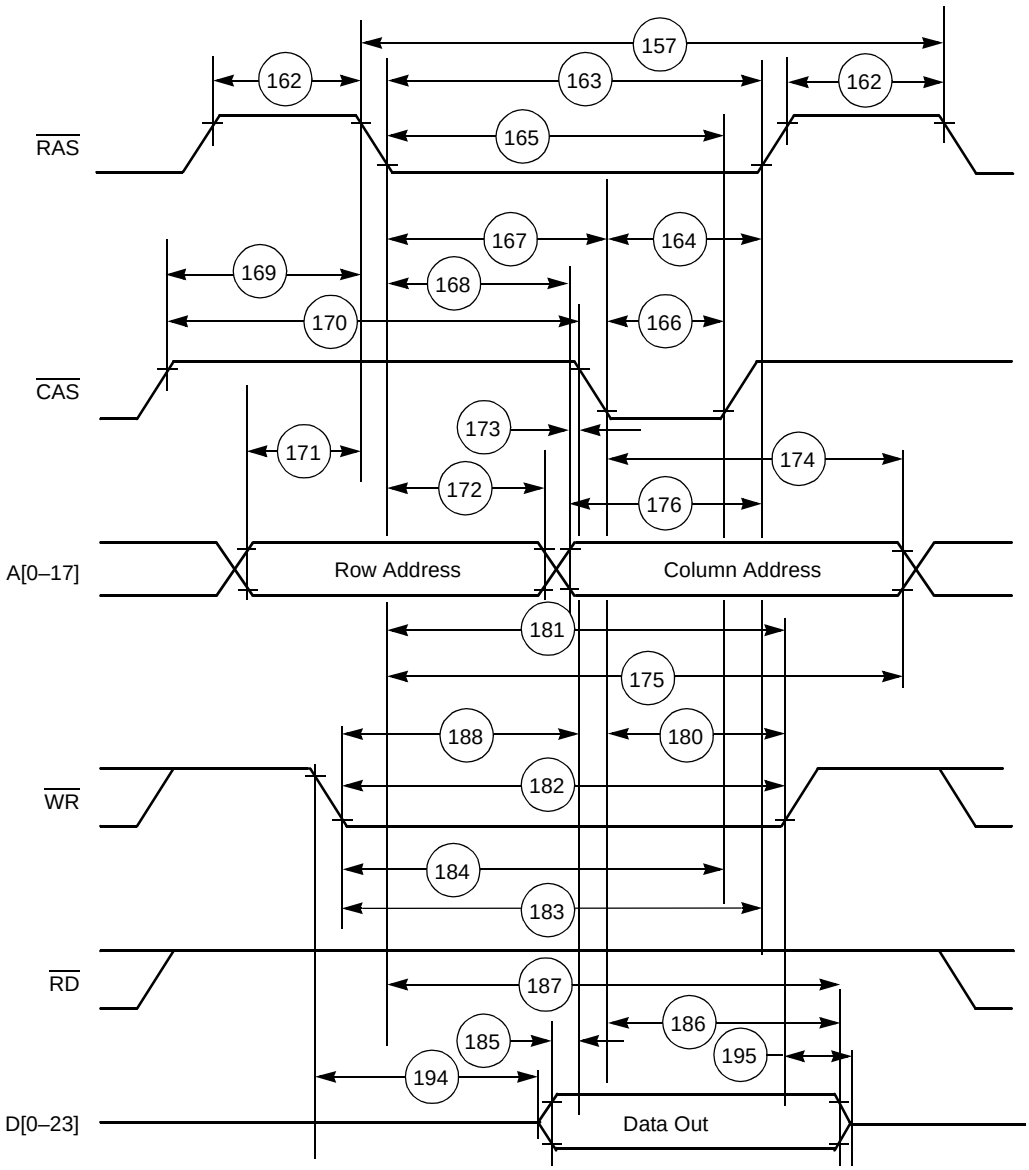


Figure 2-19. DRAM Out-of-Page Write Access

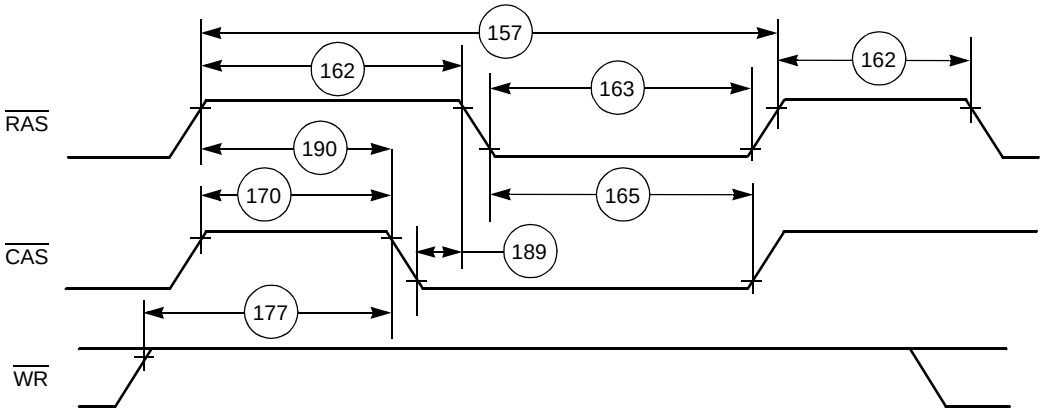
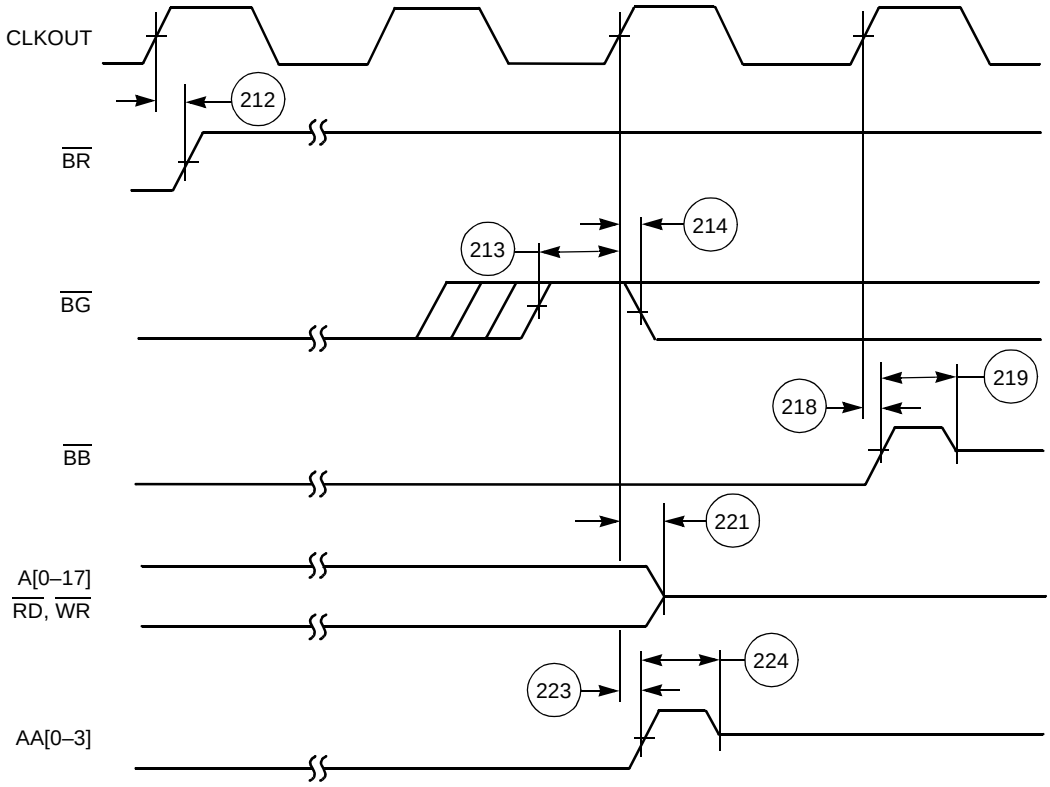


Figure 2-20. DRAM Refresh Access



Note: Address lines A[0–17] hold their state after a read or write operation. AA[0–3] do not hold their state after a read or write operation.

Figure 2-25. Bus Release Timings Case 2 (BRT Bit in Operating Mode Register Set)

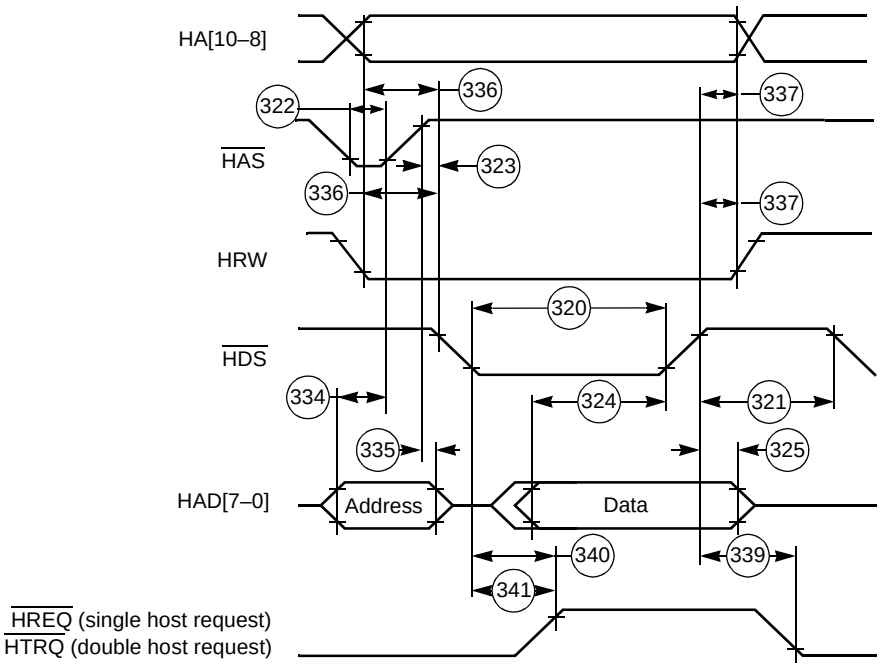


Figure 2-34. Write Timing Diagram, Multiplexed Bus, Single Data Strobe

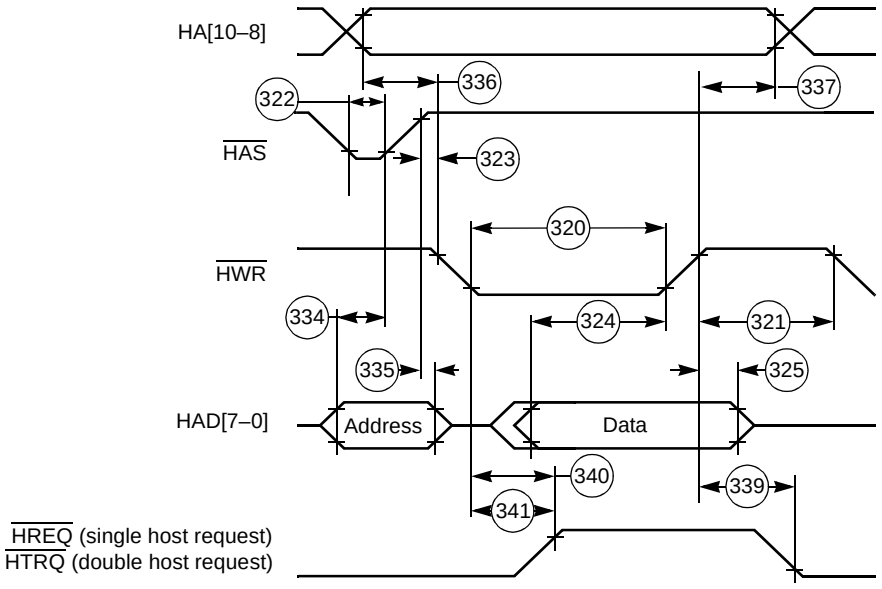


Figure 2-35. Write Timing Diagram, Multiplexed Bus, Double Data Strobe

2.6.7 SCI Timing

Table 2-17. SCI Timings

No.	Characteristics[1]	Symbol	Expression	100 MHz		Unit
				Min	Max	
400	Synchronous clock cycle	t_{SCC}[2]	$8 \times T_C$	53.3	—	ns
401	Clock low period		$t_{SCC}/2 - 10.0$	16.7	—	ns
402	Clock high period		$t_{SCC}/2 - 10.0$	16.7	—	ns
403	Output data setup to clock falling edge (internal clock)		$t_{SCC}/4 + 0.5 \times T_C - 17.0$	8.0	—	ns
404	Output data hold after clock rising edge (internal clock)		$t_{SCC}/4 - 0.5 \times T_C$	15.0	—	ns
405	Input data setup time before clock rising edge (internal clock)		$t_{SCC}/4 + 0.5 \times T_C + 25.0$	50.0	—	ns
406	Input data not valid before clock rising edge (internal clock)		$t_{SCC}/4 + 0.5 \times T_C - 5.5$	—	19.5	ns
407	Clock falling edge to output data valid (external clock)			—	32.0	ns
408	Output data hold after clock rising edge (external clock)		$T_C + 8.0$	18.0	—	ns
409	Input data setup time before clock rising edge (external clock)			0.0	—	ns
410	Input data hold time after clock rising edge (external clock)			9.0	—	ns
411	Asynchronous clock cycle	t_{ACC}[3]	$64 \times T_C$	640.0	—	ns
412	Clock low period		$t_{ACC}/2 - 10.0$	310.0	—	ns
413	Clock high period		$t_{ACC}/2 - 10.0$	310.0	—	ns
414	Output data setup to clock rising edge (internal clock)		$t_{ACC}/2 - 30.0$	290.0	—	ns
415	Output data hold after clock rising edge (internal clock)		$t_{ACC}/2 - 30.0$	290.0	—	ns

Notes:
1. $V_{CC} = 3.3\ V \pm 0.3\ V$; $T_J = -40°C$ to $+100\ °C$, $C_L = 50\ pF$.
2. t_{SCC} = synchronous clock cycle time (for internal clock, t_{SCC} is determined by the SCI clock control register and T_C).
3. t_{ACC} = asynchronous clock cycle time; value given for 1X Clock mode (for internal clock, t_{ACC} is determined by the SCI clock control register and T_C).
4. An expression is used to compute the number listed as the minimum or maximum value as appropriate.

2.6.9 Timer Timing

Table 2-19. Timer Timing[1]

No.	Characteristics	Expression[2]	100 MHz		Unit
			Min	Max	
480	TIO Low	$2 \times T_C + 2.0$	22.0	—	ns
481	TIO High	$2 \times T_C + 2.0$	22.0	—	ns
482	Timer set-up time from TIO (Input) assertion to CLKOUT rising edge		9.0	10.0	ns
483	Synchronous timer delay time from CLKOUT rising edge to the external memory access address out valid caused by first interrupt instruction execution	$10.25 \times T_C + 1.0$	103.5	—	ns
484	CLKOUT rising edge to TIO (Output) assertion • Minimum • Maximum	 $0.5 \times T_C + 0.5$ $0.5 \times T_C + 19.8$	 5.5 —	 — 24.8	 ns ns
485	CLKOUT rising edge to TIO (Output) deassertion • Minimum • Maximum	 $0.5 \times T_C + 0.5$ $0.5 \times T_C + 19.8$	 5.5 —	 — 24.8	 ns ns

Notes: **1.** V_{CC} = 3.3 V ± 0.3 V; T_J = –40°C to +100 °C, C_L = 50 pF
2. An expression is used to compute the number listed as the minimum or maximum value as appropriate.

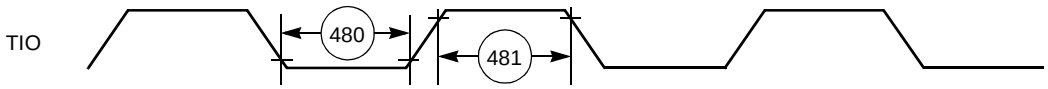


Figure 2-40. TIO Timer Event Input Restrictions

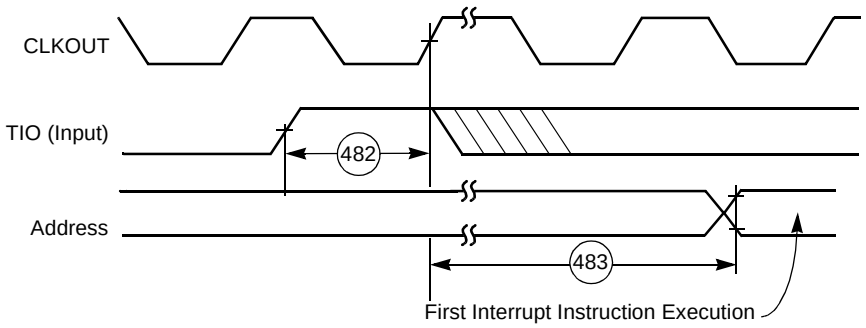


Figure 2-41. Timer Interrupt Generation

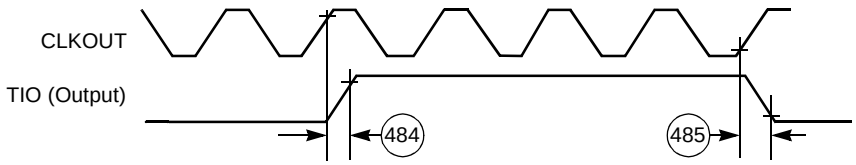
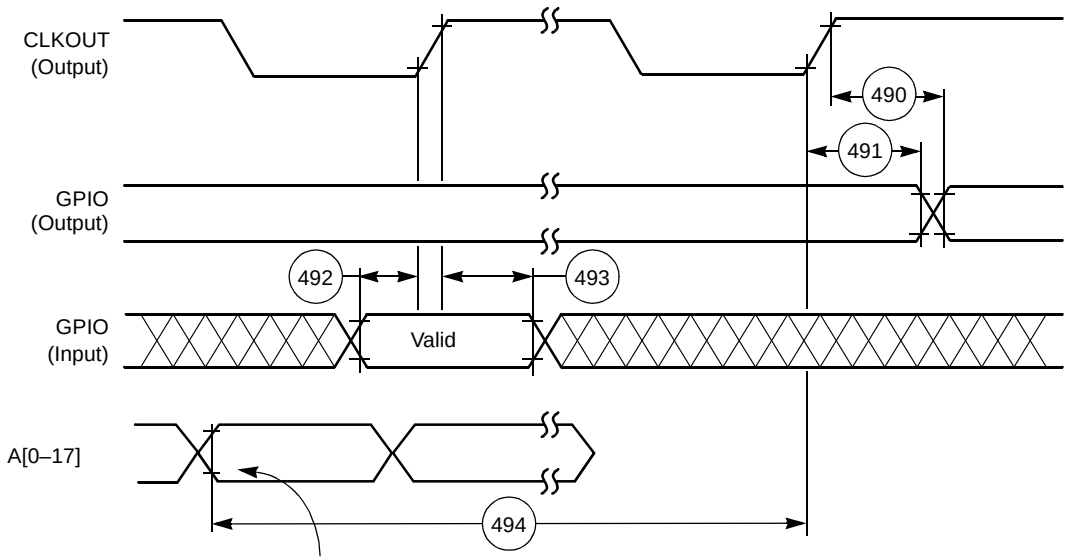


Figure 2-42. External Pulse Generation

2.6.10 GPIO Timing

Table 2-20. GPIO Timing

No.	Characteristics	Expression	100 MHz		Unit
			Min	Max	
490	CLKOUT edge to GPIO out valid (GPIO out delay time)		—	8.5	ns
491	CLKOUT edge to GPIO out not valid (GPIO out hold time)		0.0	—	ns
492	GPIO In valid to CLKOUT edge (GPIO in set-up time)		8.5	—	ns
493	CLKOUT edge to GPIO in not valid (GPIO in hold time)		0.0	—	ns
494	Fetch to CLKOUT edge before GPIO change	Minimum: $6.75 \times T_C$	67.5	—	ns
Note:	$V_{CC} = 3.3\ V \pm 0.3\ V$; $T_J = -40°C$ to $+100\ °C$, $C_L = 50\ pF$				



Fetch the instruction MOVE X0,X:(R0); X0 contains the new value of GPIO and R0 contains the address of the GPIO data register.

Figure 2-43. GPIO Timing

Chapter 3

Packaging

3.1 Pin-Out and Package Information

This section includes diagrams of the DSP56303 package pin-outs and tables showing how the signals described in **Chapter 1** are allocated for each package.

The DSP56303 is available in two package types:

- 144-pin Thin Quad Flat Pack (TQFP)
- 196-pin Molded Array Process-Ball Grid Array (MAP-BGA)

Table 3-2. DSP56303 TQFP Signal Identification by Name (Continued)

Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.
H1	42	$\overline{\text{HRD}}$/HRD	22	PB2	41
H2	41	$\overline{\text{HREQ}}$/HREQ	24	PB3	40
H3	40	$\overline{\text{HRRQ}}$/HRRQ	23	PB4	37
H4	37	HRW	22	PB5	36
H5	36	$\overline{\text{HTRQ}}$/HTRQ	24	PB6	35
H6	35	$\overline{\text{HWR}}$/HWR	21	PB7	34
H7	34	$\overline{\text{IRQA}}$	137	PB8	33
HA0	33	$\overline{\text{IRQB}}$	136	PB9	32
HA1	32	$\overline{\text{IRQC}}$	135	PC0	12
HA10	30	$\overline{\text{IRQD}}$	134	PC1	4
HA2	31	MODA	137	PC2	3
HA8	32	MODB	136	PC3	17
HA9	31	MODC	135	PC4	7
$\overline{\text{HACK}}$/HACK	23	MODD	134	PC5	10
HAD0	43	NC	20	PCAP	46
HAD1	42	NMI	6	PD0	11
HAD2	41	NC	49	PD1	144
HAD3	40	PB0	43	PD2	143
HAD4	37	PB1	42	PD3	16
HAD5	36	PB10	31	PD4	1
HAD6	35	PB11	22	PD5	2
HAD7	34	PB12	21	PE0	13
$\overline{\text{HAS}}$/HAS	33	PB13	30	PE1	14
$\overline{\text{HCS}}$/HCS	30	PB14	24	PE2	15
$\overline{\text{HDS}}$/HDS	21	PB15	23	PINIT	6

MAP-BGA Package Mechanical Drawing

4.4 PLL Performance Issues

The following explanations should be considered as general observations on expected PLL behavior. There is no test that replicates these exact numbers. These observations were measured on a limited number of parts and were not verified over the entire temperature and voltage ranges.

4.4.1 Phase Skew Performance

The phase skew of the PLL is defined as the time difference between the falling edges of EXTAL and CLKOUT for a given capacitive load on CLKOUT, over the entire process, temperature and voltage ranges. As defined in **Figure 2-2**, *External Clock Timing*, on page 2-5 for input frequencies greater than 15 MHz and the MF ≤ 4, this skew is greater than or equal to 0.0 ns and less than 1.8 ns; otherwise, this skew is not guaranteed. However, for MF < 10 and input frequencies greater than 10 MHz, this skew is between –1.4 ns and +3.2 ns.

4.4.2 Phase Jitter Performance

The phase jitter of the PLL is defined as the variations in the skew between the falling edges of EXTAL and CLKOUT for a given device in specific temperature, voltage, input frequency, MF, and capacitive load on CLKOUT. These variations are a result of the PLL locking mechanism. For input frequencies greater than 15 MHz and MF ≤ 4, this jitter is less than ±0.6 ns; otherwise, this jitter is not guaranteed. However, for MF < 10 and input frequencies greater than 10 MHz, this jitter is less than ±2 ns.

4.4.3 Frequency Jitter Performance

The frequency jitter of the PLL is defined as the variation of the frequency of CLKOUT. For small MF (MF < 10) this jitter is smaller than 0.5 percent. For mid-range MF (10 < MF < 500) this jitter is between 0.5 percent and approximately 2 percent. For large MF (MF > 500), the frequency jitter is 2–3 percent.

4.5 Input (EXTAL) Jitter Requirements

The allowed jitter on the frequency of EXTAL is 0.5 percent. If the rate of change of the frequency of EXTAL is slow (that is, it does not jump between the minimum and maximum values in one cycle) or the frequency of the jitter is fast (that is, it does not stay at an extreme value for a long time), then the allowed jitter can be 2 percent. The phase and frequency jitter performance results are valid only if the input jitter is less than the prescribed values.

Appendix A

Power Consumption Benchmark

The following benchmark program evaluates DSP56303 power use in a test situation. It enables the PLL, disables the external clock, and uses repeated multiply-accumulate (MAC) instructions with a set of synthetic DSP application data to emulate intensive sustained DSP operation.

```
;*************************************************************************
;*************************************************************************
;*                                                                       *
;* CHECKS   Typical Power Consumption                                    *
;*                                                                       *
;*************************************************************************

        page    200,55,0,0,0
        nolist

I_VEC EQU $000000; Interrupt vectors for program debug only
START EQU $8000; MAIN (external) program starting address
INT_PROG  EQU $100 ; INTERNAL program memory starting address
INT_XDAT  EQU $0; INTERNAL X-data memory starting address
INT_YDAT  EQU $0; INTERNAL Y-data memory starting address

        INCLUDE "ioequ.asm"
        INCLUDE "intequ.asm"

        list

        org     P:START
;
        movep #$0243FF,x:M_BCR ;; BCR: Area 3 = 2 w.s (SRAM)
; Default: 2w.s (SRAM)
;
        movep   #$0d0000,x:M_PCTL       ; XTAL disable
                                        ; PLL enable
                                        ; CLKOUT disable
;
; Load the program
;
        move    #INT_PROG,r0
        move    #PROG_START,r1
        do      #(PROG_END-PROG_START),PLOAD_LOOP
        move    p:(r1)+,x0
        move    x0,p:(r0)+
        nop
PLOAD_LOOP
;
; Load the X-data
;
        move    #INT_XDAT,r0
        move    #XDAT_START,r1
        do      #(XDAT_END-XDAT_START),XLOAD_LOOP
        move    p:(r1)+,x0
        move    x0,x:(r0)+
XLOAD_LOOP
;
; Load the Y-data
;
        move    #INT_YDAT,r0
        move    #YDAT_START,r1
        do      #(YDAT_END-YDAT_START),YLOAD_LOOP
        move    p:(r1)+,x0
        move    x0,y:(r0)+
YLOAD_LOOP
;

        jmp     INT_PROG

PROG_START
        move    #$0,r0
        move    #$0,r4
        move    #$3f,m0
        move    #$3f,m4
;
        clr     a
```

```
M_TLR0 EQU  $FFFF8E    ; TIMER0 Load Reg
M_TCPR0 EQU $FFFF8D        ; TIMER0 Compare Register
M_TCR0 EQU  $FFFF8C    ; TIMER0 Count Register

;       Register Addresses Of TIMER1

M_TCSR1 EQU $FFFF8B    ; TIMER1 Control/Status Register
M_TLR1 EQU  $FFFF8A    ; TIMER1 Load Reg
M_TCPR1 EQU $FFFF89        ; TIMER1 Compare Register
M_TCR1 EQU  $FFFF88    ; TIMER1 Count Register


;       Register Addresses Of TIMER2

M_TCSR2 EQU $FFFF87        ; TIMER2 Control/Status Register
M_TLR2 EQU  $FFFF86    ; TIMER2 Load Reg
M_TCPR2 EQU $FFFF85    ; TIMER2 Compare Register
M_TCR2 EQU  $FFFF84    ; TIMER2 Count Register
M_TPLR EQU  $FFFF83    ; TIMER Prescaler Load Register
M_TPCR EQU  $FFFF82    ; TIMER Prescalar Count Register


;       Timer Control/Status Register Bit Flags

M_TE EQU 0             ; Timer Enable
M_TOIE EQU 1           ; Timer Overflow Interrupt Enable
M_TCIE EQU 2           ; Timer Compare Interrupt Enable
M_TC EQU $F0           ; Timer Control Mask (TC0-TC3)
M_INV EQU 8            ; Inverter Bit
M_TRM EQU 9            ; Timer Restart Mode
M_DIR EQU 11           ; Direction Bit
M_DI EQU 12            ; Data Input
M_DO EQU 13            ; Data Output
M_PCE EQU  15          ; Prescaled Clock Enable
M_TOF EQU 20           ; Timer Overflow Flag
M_TCF EQU 21           ; Timer Compare Flag

;       Timer Prescaler Register Bit Flags

M_PS EQU  $600000      ; Prescaler Source Mask
M_PS0 EQU  21
M_PS1 EQU  22

;      Timer Control Bits
M_TC0 EQU 4            ; Timer Control 0
M_TC1 EQU 5            ; Timer Control 1
M_TC2 EQU 6            ; Timer Control 2
M_TC3 EQU 7            ; Timer Control 3


;--------------------------------------------------------------------------
;
;       EQUATES for Direct Memory Access (DMA)
;
;--------------------------------------------------------------------------

;       Register Addresses Of DMA
M_DSTR EQU FFFFF4              ; DMA Status Register
M_DOR0 EQU $FFFFF3 ; DMA Offset Register 0
M_DOR1 EQU $FFFFF2 ; DMA Offset Register 1
M_DOR2 EQU $FFFFF1 ; DMA Offset Register 2
M_DOR3 EQU $FFFFF0 ; DMA Offset Register 3


;       Register Addresses Of DMA0

M_DSR0 EQU $FFFFEF ; DMA0 Source Address Register
M_DDR0 EQU $FFFFEE ; DMA0 Destination Address Register
M_DCO0 EQU $FFFFED ; DMA0 Counter
M_DCR0 EQU $FFFFEC ; DMA0 Control Register

;       Register Addresses Of DMA1

M_DSR1 EQU $FFFFEB ; DMA1 Source Address Register
M_DDR1 EQU $FFFFEA ; DMA1 Destination Address Register
M_DCO1 EQU $FFFFE9 ; DMA1 Counter
M_DCR1 EQU $FFFFE8 ; DMA1 Control Register

;       Register Addresses Of DMA2

M_DSR2 EQU $FFFFE7 ; DMA2 Source Address Register
```