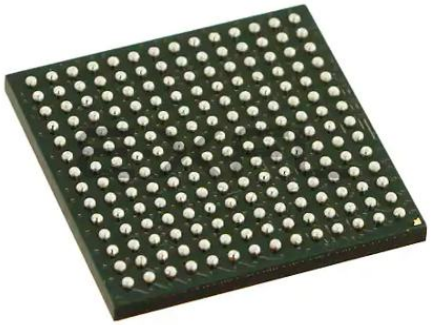

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Fixed Point
Interface	Host Interface, SSI, SCI
Clock Rate	100MHz
Non-Volatile Memory	ROM (576B)
On-Chip RAM	24kB
Voltage - I/O	3.30V
Voltage - Core	3.30V
Operating Temperature	-40°C ~ 105°C (TJ)
Mounting Type	Surface Mount
Package / Case	196-LBGA
Supplier Device Package	196-LBGA (15x15)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spakdsp303vl100

1.4 Clock

Table 1-4. Clock Signals

Signal Name	Type	State During Reset	Signal Description
EXTAL	Input	Input	**External Clock/Crystal Input**—Interfaces the internal crystal oscillator input to an external crystal or an external clock.
XTAL	Output	Chip-driven	**Crystal Output**—Connects the internal crystal oscillator output to an external crystal. If an external clock is used, leave XTAL unconnected.

1.5 PLL

Table 1-5. Phase-Locked Loop Signals

Signal Name	Type	State During Reset	Signal Description
CLKOUT	Output	Chip-driven	**Clock Output—**Provides an output clock synchronized to the internal core clock phase. If the PLL is enabled and both the multiplication and division factors equal one, then CLKOUT is also synchronized to EXTAL. If the PLL is disabled, the CLKOUT frequency is half the frequency of EXTAL.
PCAP	Input	Input	**PLL Capacitor**—An input connecting an off-chip capacitor to the PLL filter. Connect one capacitor terminal to PCAP and the other terminal to V_{CCP}. If the PLL is not used, PCAP can be tied to V_{CC}, GND, or left floating.
PINIT $\overline{\text{NMI}}$	Input Input	Input	**PLL Initial**—During assertion of $\overline{\text{RESET}}$, the value of PINIT is written into the PLL enable (PEN) bit of the PLL control (PCTL) register, determining whether the PLL is enabled or disabled. **Nonmaskable Interrupt**—After $\overline{\text{RESET}}$ deassertion and during normal instruction processing, this Schmitt-trigger input is the negative-edge-triggered NMI request internally synchronized to CLKOUT. **Note**: PINIT/$\overline{\text{NMI}}$ can tolerate 5 V.

1.8 Host Interface (HI08)

The HI08 provides a fast, 8-bit, parallel data port that connects directly to the host bus. The HI08 supports a variety of standard buses and connects directly to a number of industry-standard microcomputers, microprocessors, DSPs, and DMA hardware.

1.8.4 Host Port Usage Considerations

Careful synchronization is required when the system reads multiple-bit registers that are written by another asynchronous system. This is a common problem when two asynchronous systems are connected (as they are in the Host port). The considerations for proper operation are discussed in **Table 1-10**.

Table 1-10. Host Port Usage Considerations

Action	Description
Asynchronous read of receive byte registers	When reading the receive byte registers, Receive register High (RXH), Receive register Middle (RXM), or Receive register Low (RXL), the host interface programmer should use interrupts or poll the Receive register Data Full (RXDF) flag that indicates data is available. This assures that the data in the receive byte registers is valid.
Asynchronous write to transmit byte registers	The host interface programmer should not write to the transmit byte registers, Transmit register High (TXH), Transmit register Middle (TXM), or Transmit register Low (TXL), unless the Transmit register Data Empty (TXDE) bit is set indicating that the transmit byte registers are empty. This guarantees that the transmit byte registers transfer valid data to the Host Receive (HRX) register.
Asynchronous write to host vector	The host interface programmer must change the Host Vector (HV) register only when the Host Command bit (HC) is clear. This practice guarantees that the DSP interrupt control logic receives a stable vector.

1.8.5 Host Port Configuration

HI08 signal functions vary according to the programmed configuration of the interface as determined by the 16 bits in the HI08 Port Control Register.

Table 1-11. Host Interface

Signal Name	Type	State During Reset[1,2]	Signal Description
H[0–7]	Input/Output	Ignored Input	**Host Data—**When the HI08 is programmed to interface with a non-multiplexed host bus and the HI function is selected, these signals are lines 0–7 of the bidirectional Data bus.
HAD[0–7]	Input/Output		**Host Address—**When the HI08 is programmed to interface with a multiplexed host bus and the HI function is selected, these signals are lines 0–7 of the bidirectional multiplexed Address/Data bus.
PB[0–7]	Input or Output		**Port B 0–7—**When the HI08 is configured as GPIO through the HI08 Port Control Register, these signals are individually programmed as inputs or outputs through the HI08 Data Direction Register.

Table 1-11. Host Interface (Continued)

Signal Name	Type	State During Reset[1,2]	Signal Description
HRW	Input	Ignored Input	**Host Read/Write**—When the HI08 is programmed to interface with a single-data-strobe host bus and the HI function is selected, this signal is the Host Read/Write (HRW) input.
$\overline{\text{HRD}}$/HRD	Input		**Host Read Data**—When the HI08 is programmed to interface with a double-data-strobe host bus and the HI function is selected, this signal is the HRD strobe Schmitt-trigger input. The polarity of the data strobe is programmable but is configured as active-low ($\overline{\text{HRD}}$) after reset.
PB11	Input or Output		**Port B 11**—When the HI08 is configured as GPIO through the HI08 Port Control Register, this signal is individually programmed as an input or output through the HI08 Data Direction Register.
$\overline{\text{HDS}}$/HDS	Input	Ignored Input	**Host Data Strobe**—When the HI08 is programmed to interface with a single-data-strobe host bus and the HI function is selected, this signal is the host data strobe (HDS) Schmitt-trigger input. The polarity of the data strobe is programmable but is configured as active-low ($\overline{\text{HDS}}$) following reset.
$\overline{\text{HWR}}$/HWR	Input		**Host Write Data**—When the HI08 is programmed to interface with a double-data-strobe host bus and the HI function is selected, this signal is the host write data strobe (HWR) Schmitt-trigger input. The polarity of the data strobe is programmable but is configured as active-low ($\overline{\text{HWR}}$) following reset.
PB12	Input or Output		**Port B 12**—When the HI08 is configured as GPIO through the HI08 Port Control Register, this signal is individually programmed as an input or output through the HI08 Data Direction Register.
$\overline{\text{HREQ}}$/HREQ	Output	Ignored Input	**Host Request**—When the HI08 is programmed to interface with a single host request host bus and the HI function is selected, this signal is the host request (HREQ) output. The polarity of the host request is programmable but is configured as active-low ($\overline{\text{HREQ}}$) following reset. The host request may be programmed as a driven or open-drain output.
$\overline{\text{HTRQ}}$/HTRQ	Output		**Transmit Host Request**—When the HI08 is programmed to interface with a double host request host bus and the HI function is selected, this signal is the transmit host request (HTRQ) output. The polarity of the host request is programmable but is configured as active-low ($\overline{\text{HTRQ}}$) following reset. The host request may be programmed as a driven or open-drain output.
PB14	Input or Output		**Port B 14**—When the HI08 is configured as GPIO through the HI08 Port Control Register, this signal is individually programmed as an input or output through the HI08 Data Direction Register.

Table 1-11. Host Interface (Continued)

Signal Name	Type	State During Reset[1,2]	Signal Description
$\overline{\text{HACK}}$/HACK	Input	Ignored Input	**Host Acknowledge**—When the HI08 is programmed to interface with a single host request host bus and the HI function is selected, this signal is the host acknowledge (HACK) Schmitt-trigger input. The polarity of the host acknowledge is programmable but is configured as active-low ($\overline{\text{HACK}}$) after reset.
$\overline{\text{HRRQ}}$/HRRQ	Output		**Receive Host Request**—When the HI08 is programmed to interface with a double host request host bus and the HI function is selected, this signal is the receive host request (HRRQ) output. The polarity of the host request is programmable but is configured as active-low ($\overline{\text{HRRQ}}$) after reset. The host request may be programmed as a driven or open-drain output.
PB15	Input or Output		**Port B 15**—When the HI08 is configured as GPIO through the HI08 Port Control Register, this signal is individually programmed as an input or output through the HI08 Data Direction Register.

Notes:
1. In the Stop state, the signal maintains the last state as follows:
- If the last state is input, the signal is an ignored input.
- If the last state is output, the signal is tri-stated.

2. The Wait processing state does not affect the signal state.
3. All inputs are 5 V tolerant.

Chapter 2

Specifications

2.1 Introduction

The DSP56303 is fabricated in high-density CMOS with Transistor-Transistor Logic (TTL) compatible inputs and outputs.

2.2 Maximum Ratings

CAUTION

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, normal precautions should be taken to avoid exceeding maximum voltage ratings. Reliability is enhanced if unused inputs are tied to an appropriate logic voltage level (for example, either GND or V_{CC}).

Note: In the calculation of timing requirements, adding a maximum value of one specification to a minimum value of another specification does not yield a reasonable sum. A maximum specification is calculated using a worst case variation of process parameter values in one direction. The minimum specification is calculated using the worst case for the same parameters in the opposite direction. Therefore, a "maximum" value for a specification never occurs in the same device that has a "minimum" value for another specification; adding a maximum to a minimum represents a condition that can never exist.

2.5 DC Electrical Characteristics

Table 2-3. DC Electrical Characteristics[6]

Characteristics	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	3.0	3.3	3.6	V
Input high voltage					
• D[0–23], $\overline{BG}$, $\overline{BB}$, $\overline{TA}$	V_{IH}	2.0	—	V_{CC}	V
• MOD[1]/$\overline{IRQ}$[1], $\overline{RESET}$, PINIT/$\overline{NMI}$ and all JTAG/ESSI/SCI/Timer/HI08 pins	V_{IHP}	2.0	—	5.25	V
• EXTAL[8]	V_{IHX}	$0.8 \times V_{CC}$	—	V_{CC}	V
Input low voltage					
• D[0–23], $\overline{BG}$, $\overline{BB}$, $\overline{TA}$, MOD[1]/$\overline{IRQ}$[1], $\overline{RESET}$, PINIT	V_{IL}	–0.3	—	0.8	V
• All JTAG/ESSI/SCI/Timer/HI08 pins	V_{ILP}	–0.3	—	0.8	V
• EXTAL[8]	V_{ILX}	–0.3	—	$0.2 \times V_{CC}$	V
Input leakage current	I_{IN}	–10	—	10	µA
High impedance (off-state) input current (@ 2.4 V / 0.4 V)	I_{TSI}	–10	—	10	µA
Output high voltage	V_{OH}				
• TTL (I_{OH} = –0.4 mA)[5,7]		2.4	—	—	V
• CMOS (I_{OH} = –10 µA)[5]		V_{CC} – 0.01	—	—	V
Output low voltage	V_{OL}				
• TTL (I_{OL} = 1.6 mA, open-drain pins I_{OL} = 6.7 mA)[5,7]		—	—	0.4	V
• CMOS (I_{OL} = 10 µA)[5]		—	—	0.01	V
Internal supply current[2]:					
• In Normal mode	I_{CCI}	—	127	—	mA
• In Wait mode[3]	I_{CCW}	—	7.5	—	mA
• In Stop mode[4]	I_{CCS}	—	100	—	µA
PLL supply current		—	1	2.5	mA
Input capacitance[5]	C_{IN}	—	—	10	pF

Notes:
1. Refers to MODA/$\overline{IRQA}$, MODB/$\overline{IRQB}$, MODC/$\overline{IRQC}$, and MODD/$\overline{IRQD}$ pins.
2. **Power Consumption Considerations** on page Section 4-3 provides a formula to compute the estimated current requirements in Normal mode. In order to obtain these results, all inputs must be terminated (that is, not allowed to float). Measurements are based on synthetic intensive DSP benchmarks (see **Appendix A**). The power consumption numbers in this specification are 90 percent of the measured results of this benchmark. This reflects typical DSP applications. Typical internal supply current is measured with V_{CC} = 3.3 V at T_J = 100°C.
3. In order to obtain these results, all inputs must be terminated (that is, not allowed to float).
4. In order to obtain these results, all inputs that are not disconnected at Stop mode must be terminated (that is, not allowed to float). PLL and XTAL signals are disabled during Stop state.
5. Periodically sampled and not 100 percent tested.
6. V_{CC} = 3.3 V ± 0.3 V; T_J = –40°C to +100 °C, C_L = 50 pF
7. This characteristic does not apply to XTAL and PCAP.
8. Driving EXTAL to the low V_{IHX} or the high V_{ILX} value may cause additional power consumption (DC current). To minimize power consumption, the minimum V_{IHX} should be no lower than $0.9 \times V_{CC}$ and the maximum V_{ILX} should be no higher than $0.1 \times V_{CC}$.

2.6 AC Electrical Characteristics

The timing waveforms shown in the AC electrical characteristics section are tested with a V_{IL} maximum of 0.3 V and a V_{IH} minimum of 2.4 V for all pins except EXTAL, which is tested using the input levels shown in Note 6 of the previous table. AC timing specifications, which are referenced to a device input signal, are measured in production with respect to the 50 percent point of the respective input signal transition. DSP56303 output levels are measured with the production test machine V_{OL} and V_{OH} reference levels set at 0.4 V and 2.4 V, respectively.

Note: Although the minimum value for the frequency of EXTAL is 0 MHz, the device AC test conditions are 15 MHz and rated speed.

2.6.1 Internal Clocks

Table 2-4. Internal Clocks, CLKOUT

Characteristics	Symbol	Expression[1, 2]		
		Min	Typ	Max
Internal operation frequency and CLKOUT with PLL enabled	f	—	(Ef × MF)/ (PDF × DF)	—
Internal operation frequency and CLKOUT with PLL disabled	f	—	Ef/2	—
Internal clock and CLKOUT high period • With PLL disabled • With PLL enabled and MF ≤ 4 • With PLL enabled and MF > 4	T_H	 — 0.49 × ET_C × PDF × DF/MF 0.47 × ET_C × PDF × DF/MF	 ET_C — —	 — 0.51 × ET_C × PDF × DF/MF 0.53 × ET_C × PDF × DF/MF
Internal clock and CLKOUT low period • With PLL disabled • With PLL enabled and MF ≤ 4 • With PLL enabled and MF > 4	T_L	 — 0.49 × ET_C × PDF × DF/MF 0.47 × ET_C × PDF × DF/MF	 ET_C — —	 — 0.51 × ET_C × PDF × DF/MF 0.53 × ET_C × PDF × DF/MF
Internal clock and CLKOUT cycle time with PLL enabled	T_C	—	ET_C × PDF × DF/MF	—
Internal clock and CLKOUT cycle time with PLL disabled	T_C	—	2 × ET_C	—
Instruction cycle time	I_{CYC}	—	T_C	—

Notes: **1.** DF = Division Factor; Ef = External frequency; ET_C = External clock cycle; MF = Multiplication Factor; PDF = Predivision Factor; T_C = internal clock cycle

2. See the PLL and Clock Generation section in the *DSP56300 Family Manual* for a detailed discussion of the PLL.

Table 2-7. Reset, Stop, Mode Select, and Interrupt Timing[6] (Continued)

No.	Characteristics	Expression	100 MHz		Unit
			Min	Max	

Notes:

1. When fast interrupts are used and $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$, $\overline{\text{IRQC}}$, and $\overline{\text{IRQD}}$ are defined as level-sensitive, timings 19 through 21 apply to prevent multiple interrupt service. To avoid these timing restrictions, the deasserted Edge-triggered mode is recommended when fast interrupts are used. Long interrupts are recommended for Level-sensitive mode.

2. This timing depends on several settings:
- For PLL disable, using internal oscillator (PLL Control Register (PCTL) Bit 16 = 0) and oscillator disabled during Stop (PCTL Bit 17 = 0), a stabilization delay is required to assure that the oscillator is stable before programs are executed. Resetting the Stop delay (Operating Mode Register Bit 6 = 0) provides the proper delay. While Operating Mode Register Bit 6 = 1 can be set, it is not recommended, and these specifications do not guarantee timings for that case.
- For PLL disable, using internal oscillator (PCTL Bit 16 = 0) and oscillator enabled during Stop (PCTL Bit 17=1), no stabilization delay is required and recovery is minimal (Operating Mode Register Bit 6 setting is ignored).
- For PLL disable, using external clock (PCTL Bit 16 = 1), no stabilization delay is required and recovery time is defined by the PCTL Bit 17 and Operating Mode Register Bit 6 settings.
- For PLL enable, if PCTL Bit 17 is 0, the PLL is shutdown during Stop. Recovering from Stop requires the PLL to get locked. The PLL lock procedure duration, PLL Lock Cycles (PLC), may be in the range of 0 to 1000 cycles. This procedure occurs in parallel with the stop delay counter, and stop recovery ends when the last of these two events occurs. The stop delay counter completes count or PLL lock procedure completion.
- PLC value for PLL disable is 0.
- The maximum value for ET_C is 4096 (maximum MF) divided by the desired internal frequency (that is, for 66 MHz it is 4096/66 MHz = 62 µs). During the stabilization period, T_C, T_H, and T_L is not constant, and their width may vary, so timing may vary as well.

3. Periodically sampled and not 100 percent tested.

4. Value depends on clock source:
- For an external clock generator, $\overline{\text{RESET}}$ duration is measured while $\overline{\text{RESET}}$ is asserted, V_{CC} is valid, and the EXTAL input is active and valid.
- For an internal oscillator, $\overline{\text{RESET}}$ duration is measured while $\overline{\text{RESET}}$ is asserted and V_{CC} is valid. The specified timing reflects the crystal oscillator stabilization time after power-up. This number is affected both by the specifications of the crystal and other components connected to the oscillator and reflects worst case conditions.
- When the V_{CC} is valid, but the other "required $\overline{\text{RESET}}$ duration" conditions (as specified above) have not been yet met, the device circuitry is in an uninitialized state that can result in significant power consumption and heat-up. Designs should minimize this state to the shortest possible duration.

5. If PLL does not lose lock.

6. V_{CC} = 3.3 V ± 0.3 V; T_J = –40°C to +100°C, C_L = 50 pF.

7. WS = number of wait states (measured in clock cycles, number of T_C).

8. Use the expression to compute a maximum value.

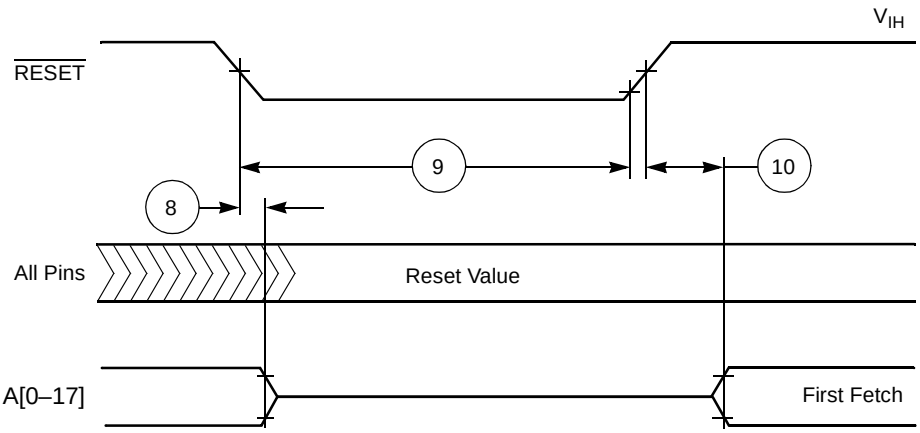


Figure 2-3. Reset Timing

Table 2-8. SRAM Read and Write Accesses (Continued)

No.	Characteristics	Symbol	Expression[1]	100 MHz		Unit
				Min	Max	
111	$\overline{WR}$ deassertion to data high impedance	—	$0.25 \times T_C + 0.2$ [1 ≤ WS ≤ 3]	—	2.7	ns
			$1.25 \times TC + 0.2$ [4 ≤ WS ≤ 7]	—	12.7	ns
			$2.25 \times T_C + 0.2$ [WS > 8]	—	22.7	ns
112	Previous $\overline{RD}$ deassertion to data active (write)	—	$1.25 \times T_C - 4.0$ [1 ≤ WS ≤ 3]	8.5	—	ns
			$2.25 \times T_C - 4.0$ [4 ≤ WS ≤ 7]	18.5	—	ns
			$3.25 \times T_C - 4.0$ [WS > 8]	28.5	—	ns
113	$\overline{RD}$ deassertion time	—	$0.75 \times T_C - 4.0$ [1 ≤ WS ≤ 3]	3.5	—	ns
			$1.75 \times T_C - 4.0$ [4 ≤ WS ≤ 7]	13.5	—	ns
			$2.75 \times T_C - 4.0$ [WS ≥ 8]	23.5	—	ns
114	$\overline{WR}$ deassertion time	—	$0.5 \times T_C - 4.0$ [WS = 1]	1.0	—	ns
			$T_C - 4.0$ [2 ≤ WS ≤ 3]	6.0	—	ns
			$2.5 \times T_C - 4.0$ [4 ≤ WS ≤ 7]	21.0	—	ns
			$3.5 \times T_C - 4.0$ [WS ≥ 8]	31.0	—	ns
115	Address valid to $\overline{RD}$ assertion	—	$0.5 \times T_C - 4.0$	1.0	—	ns
116	$\overline{RD}$ assertion pulse width	—	$(WS + 0.25) \times T_C - 4.0$	8.5	—	ns
117	$\overline{RD}$ deassertion to address not valid	—	$0.25 \times T_C - 2.0$ [1 ≤ WS ≤ 3]	0.5	—	ns
			$1.25 \times T_C - 2.0$ [4 ≤ WS ≤ 7]	10.5	—	ns
			$2.25 \times T_C - 2.0$ [WS ≥ 8]	20.5	—	ns
118	$\overline{TA}$ setup before $\overline{RD}$ or $\overline{WR}$ deassertion[4]	—	$0.25 \times T_C + 2.0$	4.5	—	ns
119	$\overline{TA}$ hold after $\overline{RD}$ or $\overline{WR}$ deassertion	—	—	0	—	ns

Notes:
1. WS is the number of wait states specified in the BCR. An expression is used to compute the number listed as the minimum or maximum value, as appropriate.
2. Timings 100, 107 are guaranteed by design, not tested.
3. All timings for 100 MHz are measured from $0.5 \times Vcc$ to $0.5 \times Vcc$.
4. Timing 118 is relative to the deassertion edge of $\overline{RD}$ or $\overline{WR}$ even if $\overline{TA}$ remains asserted.
5. V_{CC} = 3.3 V ± 0.3 V; T_J = –40°C to +100°C, C_L = 50 pF

Table 2-12. DRAM Out-of-Page and Refresh Timings, Fifteen Wait States[1,2] (Continued)

No.	Characteristics	Symbol	Expression[3]	100 MHz		Unit
				Min	Max	

Notes:
1. The number of wait states for an out-of-page access is specified in the DRAM Control Register.
2. The refresh period is specified in the DRAM Control Register.
3. Use the expression to compute the maximum or minimum value listed (or both if the expression includes ±).
4. Either t_{RCH} or t_{RRH} must be satisfied for read cycles.
5. $\overline{RD}$ deassertion always occurs after $\overline{CAS}$ deassertion; therefore, the restricted timing is t_{OFF} and not t_{GZ}.

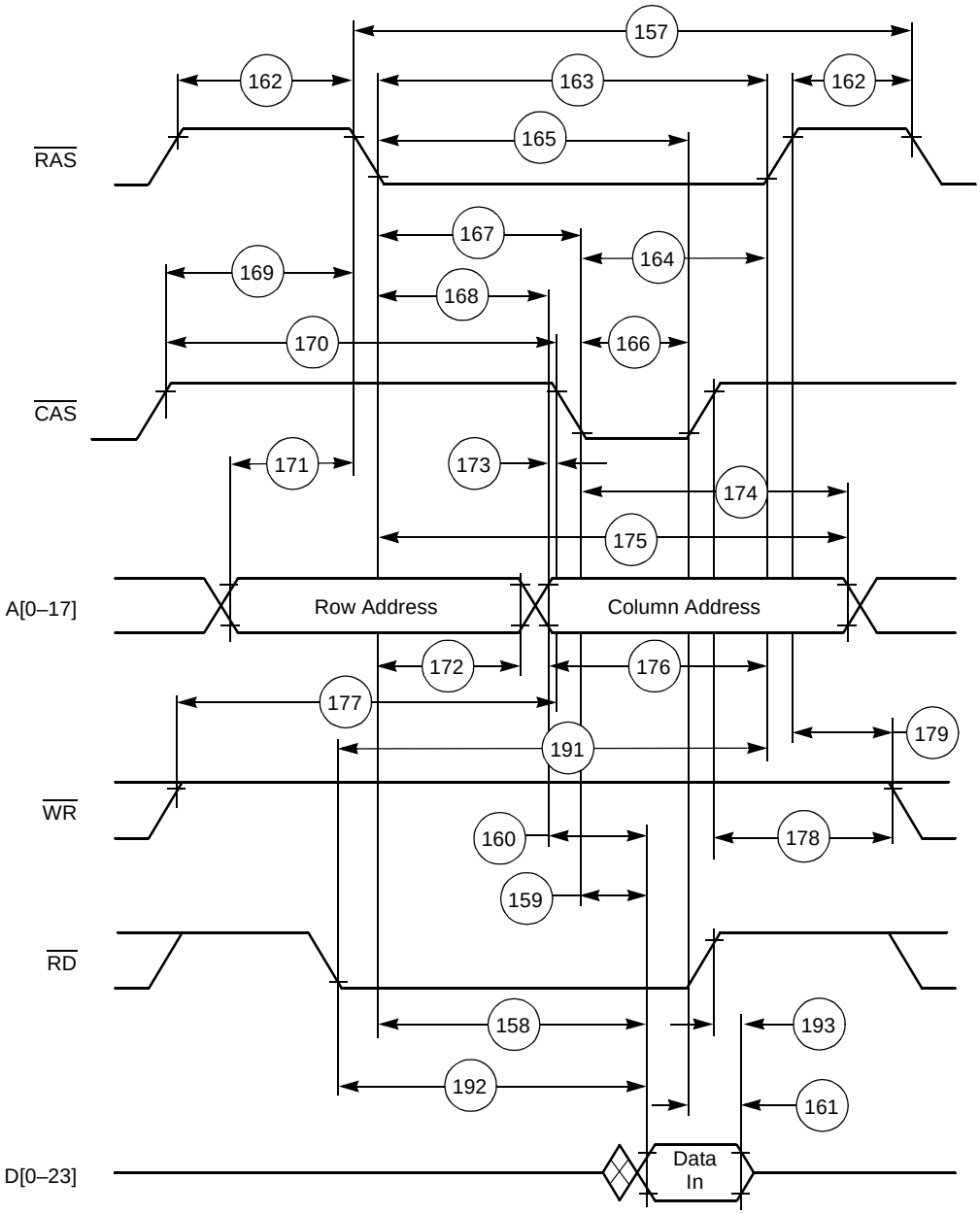


Figure 2-18. DRAM Out-of-Page Read Access

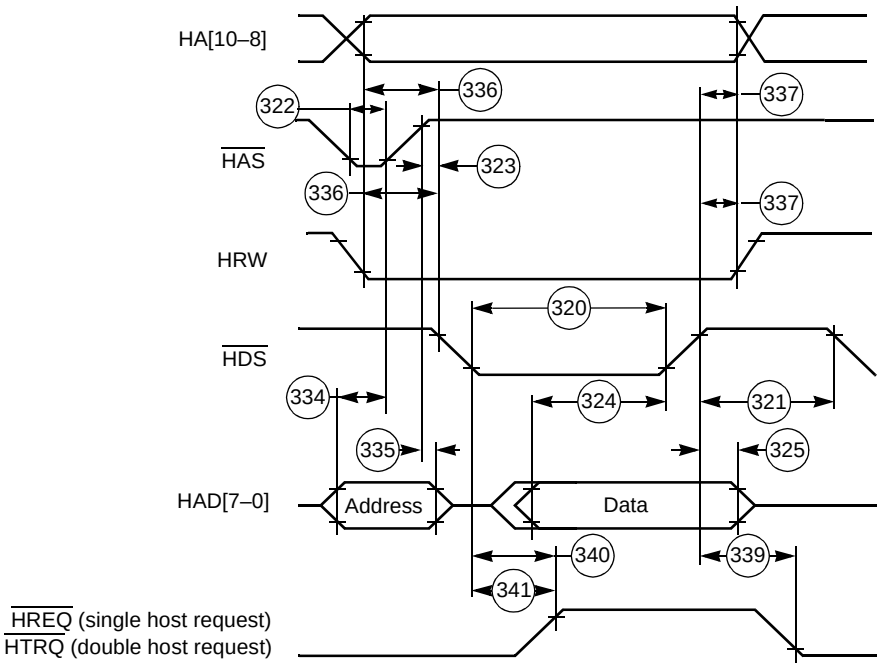


Figure 2-34. Write Timing Diagram, Multiplexed Bus, Single Data Strobe

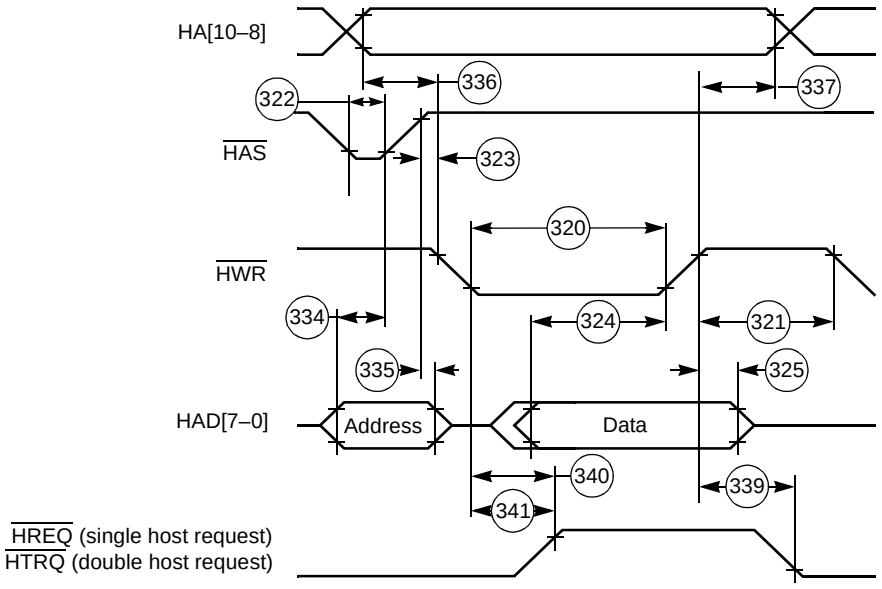
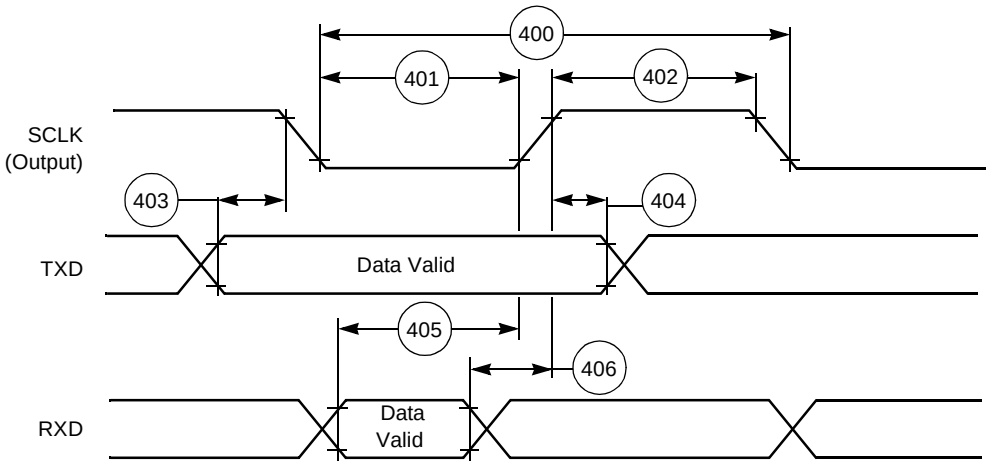
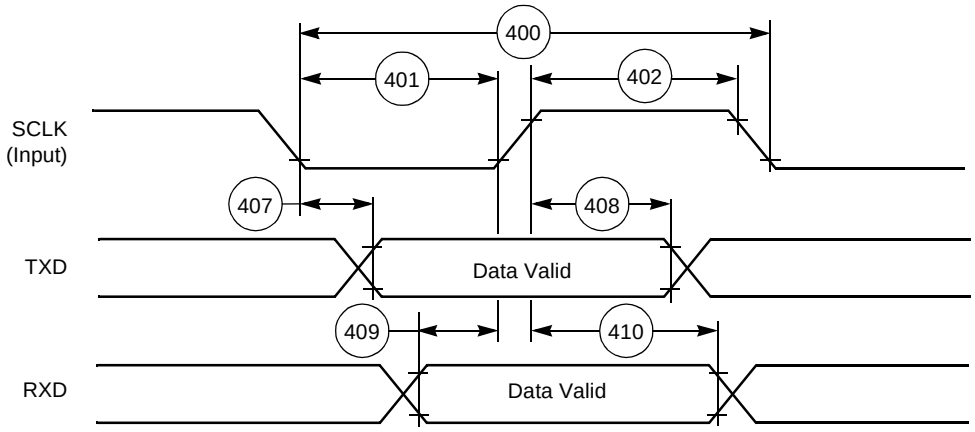


Figure 2-35. Write Timing Diagram, Multiplexed Bus, Double Data Strobe



a) Internal Clock



b) External Clock

Figure 2-36. SCI Synchronous Mode Timing

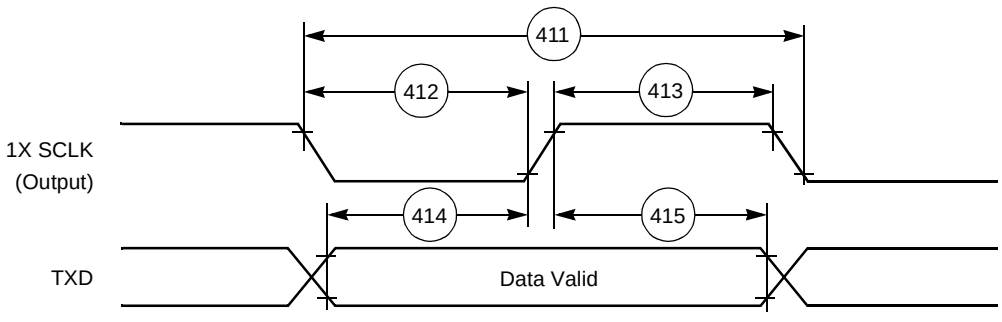


Figure 2-37. SCI Asynchronous Mode Timing

2.6.8 ESSI0/ESSI1 Timing

Table 2-18. ESSI Timings

No.	Characteristics[4, 5, 7]	Symbol	Expression[9]	100 MHz		Cond-ition[5]	Unit
				Min	Max		
430	Clock cycle[1]	t_{SSICC}	$3 \times T_C$ $4 \times T_C$	30.0 40.0	— —	x ck i ck	ns
431	Clock high period • For internal clock • For external clock		 $2 \times T_C$ - 10.0 $1.5 \times T_C$	 10.0 15.0	 — —		 ns ns
432	Clock low period • For internal clock • For external clock		 $2 \times T_C$ – 10.0 $1.5 \times T_C$	 10.0 15.0	 — —		 ns ns
433	RXC rising edge to FSR out (bit-length) high			— —	37.0 22.0	x ck i ck a	ns
434	RXC rising edge to FSR out (bit-length) low			— —	37.0 22.0	x ck i ck a	ns
435	RXC rising edge to FSR out (word-length-relative) high[2]			— —	39.0 37.0	x ck i ck a	ns
436	RXC rising edge to FSR out (word-length-relative) low[2]			— —	39.0 37.0	x ck i ck a	ns
437	RXC rising edge to FSR out (word-length) high			— —	36.0 21.0	x ck i ck a	ns
438	RXC rising edge to FSR out (word-length) low			— —	37.0 22.0	x ck i ck a	ns
439	Data in setup time before RXC (SCK in Synchronous mode) falling edge			10.0 19.0	— —	x ck i ck	ns
440	Data in hold time after RXC falling edge			5.0 3.0	— —	x ck i ck	ns
441	FSR input (bl, wr) high before RXC falling edge[2]			1.0 23.0	— —	x ck i ck a	ns
442	FSR input (wl) high before RXC falling edge			3.5 23.0	— —	x ck i ck a	ns
443	FSR input hold time after RXC falling edge			3.0 0.0	— —	x ck i ck a	ns
444	Flags input setup before RXC falling edge			5.5 19.0	— —	x ck i ck s	ns
445	Flags input hold time after RXC falling edge			6.0 0.0	— —	x ck i ck s	ns
446	TXC rising edge to FST out (bit-length) high			— —	29.0 15.0	x ck i ck	ns
447	TXC rising edge to FST out (bit-length) low			— —	31.0 17.0	x ck i ck	ns
448	TXC rising edge to FST out (word-length-relative) high[2]			— —	31.0 17.0	x ck i ck	ns
449	TXC rising edge to FST out (word-length-relative) low[2]			— —	33.0 19.0	x ck i ck	ns

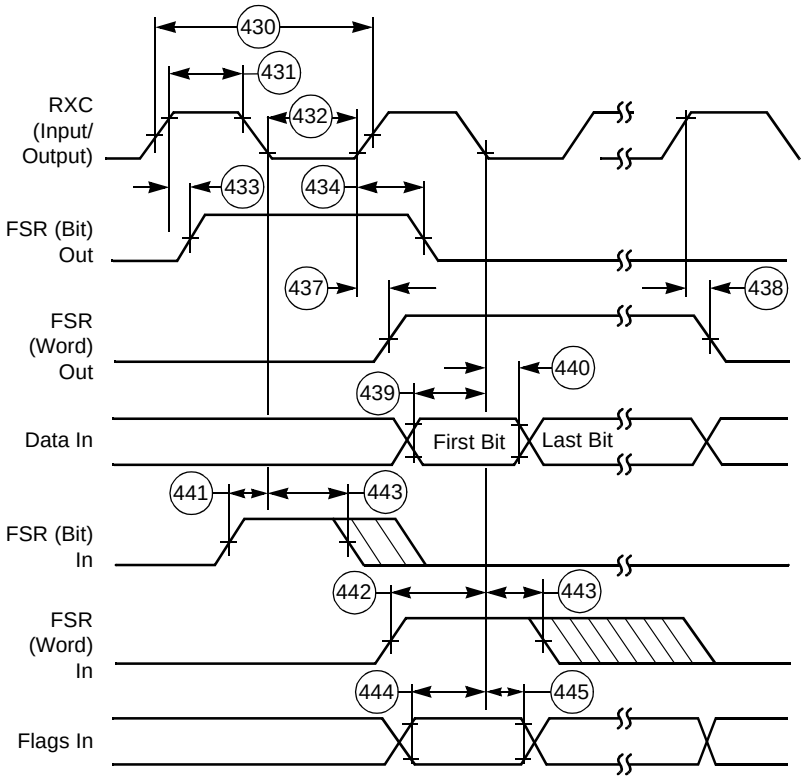
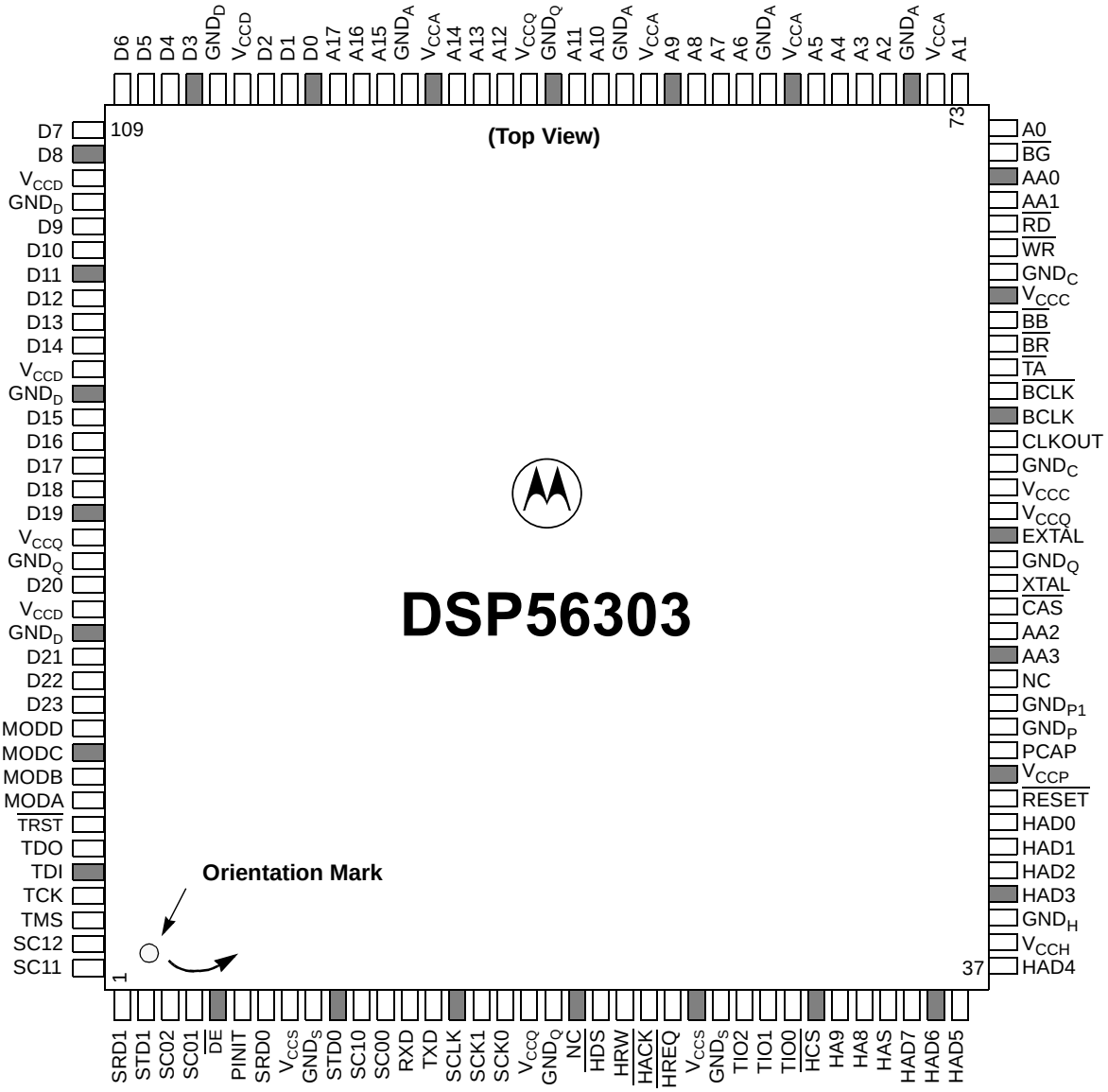


Figure 2-39. ESSI Receiver Timing

3.2 TQFP Package Description

Top and bottom views of the TQFP package are shown in **Figure 3-1** and **Figure 3-2** with their pin-outs.



Notes: Because of size constraints in this figure, only one name is shown for multiplexed pins. Refer to **Table 3-1** and **Table 3-2** for detailed information about pin functions and signal names.

Figure 3-1. DSP56303 Thin Quad Flat Pack (TQFP), Top View

Table 3-2. DSP56303 TQFP Signal Identification by Name

Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.
A0	72	$\overline{BG}$	71	D7	109
A1	73	$\overline{BR}$	63	D8	110
A10	88	$\overline{CAS}$	52	D9	113
A11	89	CLKOUT	59	$\overline{DE}$	5
A12	92	D0	100	EXTAL	55
A13	93	D1	101	GND_A	75
A14	94	D10	114	GND_A	81
A15	97	D11	115	GND_A	87
A16	98	D12	116	GND_A	96
A17	99	D13	117	GND_C	58
A2	76	D14	118	GND_C	66
A3	77	D15	121	GND_D	104
A4	78	D16	122	GND_D	112
A5	79	D17	123	GND_D	120
A6	82	D18	124	GND_D	130
A7	83	D19	125	GND_H	39
A8	84	D2	102	GND_P	47
A9	85	D20	128	GND_{P1}	48
AA0	70	D21	131	GND_Q	19
AA1	69	D22	132	GND_Q	54
AA2	51	D23	133	GND_Q	90
AA3	50	D3	105	GND_Q	127
$\overline{BB}$	64	D4	106	GND_S	9
BCLK	60	D5	107	GND_S	26
$\overline{BCLK}$	61	D6	108	H0	43

Table 3-2. DSP56303 TQFP Signal Identification by Name (Continued)

Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.
$\overline{\text{RAS0}}$	70	SRD1	1	V_{CCC}	57
$\overline{\text{RAS1}}$	69	STD0	10	V_{CCC}	65
$\overline{\text{RAS2}}$	51	STD1	2	V_{CCD}	103
$\overline{\text{RAS3}}$	50	$\overline{\text{TA}}$	62	V_{CCD}	111
$\overline{\text{RD}}$	68	TCK	141	V_{CCD}	119
$\overline{\text{RESET}}$	44	TDI	140	V_{CCD}	129
RXD	13	TDO	139	V_{CCH}	38
SC00	12	TIO0	29	V_{CCP}	45
SC01	4	TIO1	28	V_{CCQ}	18
SC02	3	TIO2	27	V_{CCQ}	56
SC10	11	TMS	142	V_{CCQ}	91
SC11	144	$\overline{\text{TRST}}$	138	V_{CCQ}	126
SC12	143	TXD	14	V_{CCS}	8
SCK0	17	V_{CCA}	74	V_{CCS}	25
SCK1	16	V_{CCA}	80	$\overline{\text{WR}}$	67
SCLK	15	V_{CCA}	86	XTAL	53
SRD0	7	V_{CCA}	95		

4.4 PLL Performance Issues

The following explanations should be considered as general observations on expected PLL behavior. There is no test that replicates these exact numbers. These observations were measured on a limited number of parts and were not verified over the entire temperature and voltage ranges.

4.4.1 Phase Skew Performance

The phase skew of the PLL is defined as the time difference between the falling edges of EXTAL and CLKOUT for a given capacitive load on CLKOUT, over the entire process, temperature and voltage ranges. As defined in **Figure 2-2**, *External Clock Timing*, on page 2-5 for input frequencies greater than 15 MHz and the MF ≤ 4, this skew is greater than or equal to 0.0 ns and less than 1.8 ns; otherwise, this skew is not guaranteed. However, for MF < 10 and input frequencies greater than 10 MHz, this skew is between –1.4 ns and +3.2 ns.

4.4.2 Phase Jitter Performance

The phase jitter of the PLL is defined as the variations in the skew between the falling edges of EXTAL and CLKOUT for a given device in specific temperature, voltage, input frequency, MF, and capacitive load on CLKOUT. These variations are a result of the PLL locking mechanism. For input frequencies greater than 15 MHz and MF ≤ 4, this jitter is less than ±0.6 ns; otherwise, this jitter is not guaranteed. However, for MF < 10 and input frequencies greater than 10 MHz, this jitter is less than ±2 ns.

4.4.3 Frequency Jitter Performance

The frequency jitter of the PLL is defined as the variation of the frequency of CLKOUT. For small MF (MF < 10) this jitter is smaller than 0.5 percent. For mid-range MF (10 < MF < 500) this jitter is between 0.5 percent and approximately 2 percent. For large MF (MF > 500), the frequency jitter is 2–3 percent.

4.5 Input (EXTAL) Jitter Requirements

The allowed jitter on the frequency of EXTAL is 0.5 percent. If the rate of change of the frequency of EXTAL is slow (that is, it does not jump between the minimum and maximum values in one cycle) or the frequency of the jitter is fast (that is, it does not stay at an extreme value for a long time), then the allowed jitter can be 2 percent. The phase and frequency jitter performance results are valid only if the input jitter is less than the prescribed values.

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Ordering Information

Consult a Motorola Semiconductor sales office or authorized distributor to determine product availability and place an order.

Part	Supply Voltage	Package Type	Pin Count	Core Frequency (MHz)	Order Number
DSP56303	3.3 V I/O	Thin Quad Flat Pack (TQFP)	144	100	DSP56303PV100
		Molded Array Process-Ball Grid Array (MAP-BGA)	196	100	DSP56303VF100

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