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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Fixed Point
Interface	Host Interface, SSI, SCI
Clock Rate	100MHz
Non-Volatile Memory	ROM (576B)
On-Chip RAM	24kB
Voltage - I/O	3.30V
Voltage - Core	3.30V
Operating Temperature	-40°C ~ 105°C (TJ)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spakxc309ag100a

Table 1-11. Host Interface (Continued)

Signal Name	Type	State During Reset[1,2]	Signal Description
HA0	Input	Ignored Input	**Host Address Input 0**—When the HI08 is programmed to interface with a nonmultiplexed host bus and the HI function is selected, this signal is line 0 of the host address input bus.
$\overline{\text{HAS}}$/HAS	Input		**Host Address Strobe—**When the HI08 is programmed to interface with a multiplexed host bus and the HI function is selected, this signal is the host address strobe (HAS) Schmitt-trigger input. The polarity of the address strobe is programmable but is configured active-low ($\overline{\text{HAS}}$) following reset.
PB8	Input or Output		**Port B 8**—When the HI08 is configured as GPIO through the HI08 Port Control Register, this signal is individually programmed as an input or output through the HI08 Data Direction Register.
HA1	Input	Ignored Input	**Host Address Input 1**—When the HI08 is programmed to interface with a nonmultiplexed host bus and the HI function is selected, this signal is line 1 of the host address (HA1) input bus.
HA8	Input		**Host Address 8**—When the HI08 is programmed to interface with a multiplexed host bus and the HI function is selected, this signal is line 8 of the host address (HA8) input bus.
PB9	Input or Output		**Port B 9**—When the HI08 is configured as GPIO through the HI08 Port Control Register, this signal is individually programmed as an input or output through the HI08 Data Direction Register.
HA2	Input	Ignored Input	**Host Address Input 2**—When the HI08 is programmed to interface with a nonmultiplexed host bus and the HI function is selected, this signal is line 2 of the host address (HA2) input bus.
HA9	Input		**Host Address 9**—When the HI08 is programmed to interface with a multiplexed host bus and the HI function is selected, this signal is line 9 of the host address (HA9) input bus.
PB10	Input or Output		**Port B 10**—When the HI08 is configured as GPIO through the HI08 Port Control Register, this signal is individually programmed as an input or output through the HI08 Data Direction Register.
$\overline{\text{HCS}}$/HCS	Input	Ignored Input	**Host Chip Select**—When the HI08 is programmed to interface with a nonmultiplexed host bus and the HI function is selected, this signal is the host chip select (HCS) input. The polarity of the chip select is programmable but is configured active-low ($\overline{\text{HCS}}$) after reset.
HA10	Input		**Host Address 10**—When the HI08 is programmed to interface with a multiplexed host bus and the HI function is selected, this signal is line 10 of the host address (HA10) input bus.
PB13	Input or Output		**Port B 13**—When the HI08 is configured as GPIO through the HI08 Port Control Register, this signal is individually programmed as an input or output through the HI08 Data Direction Register.

Table 2-5. Clock Operation

No.	Characteristics	Symbol	100 MHz	
			Min	Max
1	Frequency of EXTAL (EXTAL Pin Frequency) The rise and fall time of this external clock should be 3 ns maximum.	Ef	0	100.0
2	EXTAL input high[1, 2] • With PLL disabled (46.7%–53.3% duty cycle[6]) • With PLL enabled (42.5%–57.5% duty cycle[6])	ET_H	 4.67 ns 4.25 ns	 ∞ 157.0 µs
3	EXTAL input low[1, 2] • With PLL disabled (46.7%–53.3% duty cycle[6]) • With PLL enabled (42.5%–57.5% duty cycle[6])	ET_L	 4.67 ns 4.25 ns	 ∞ 157.0 µs
4	EXTAL cycle time[2] • With PLL disabled • With PLL enabled	ET_C	 10.00 ns 10.00 ns	 ∞ 273.1 µs
5	Internal clock change from EXTAL fall with PLL disabled		4.3 ns	11.0 ns
6	a.Internal clock rising edge from EXTAL rising edge with PLL enabled (MF = 1 or 2 or 4, PDF = 1, Ef > 15 MHz)[3,5] b. Internal clock falling edge from EXTAL falling edge with PLL enabled (MF ≤ 4, PDF ≠ 1, Ef / PDF > 15 MHz)[3,5]		0.0 ns 0.0 ns	1.8 ns 1.8 ns
7	Instruction cycle time = $I_{CYC} = T_C$[4] (see **Table 2-4**) (46.7%–53.3% duty cycle) • With PLL disabled • With PLL enabled	I_{CYC}	 20.0 ns 10.00 ns	 ∞ 8.53 µs

Notes:
1. Measured at 50 percent of the input transition.
2. The maximum value for PLL enabled is given for minimum VCO frequency (see **Table 2-4**) and maximum MF.
3. Periodically sampled and not 100 percent tested.
4. The maximum value for PLL enabled is given for minimum VCO frequency and maximum DF.
5. The skew is not guaranteed for any other MF value.
6. The indicated duty cycle is for the specified maximum frequency for which a part is rated. The minimum clock high or low time required for correction operation, however, remains the same at lower operating frequencies; therefore, when a lower clock frequency is used, the signal symmetry may vary from the specified duty cycle as long as the minimum high time and low time requirements are met.

2.6.3 Phase Lock Loop (PLL) Characteristics

Table 2-6. PLL Characteristics

Characteristics	100 MHz		Unit
	Min	Max	
Voltage Controlled Oscillator (VCO) frequency when PLL enabled (MF × E_f × 2/PDF)	30	200	MHz
PLL external capacitor (PCAP pin to V_{CCP}) (C_{PCAP}[1]) • @ MF ≤ 4 • @ MF > 4	 (580 × MF) – 100 830 × MF	 (780 × MF) – 140 1470 × MF	 pF pF

Note: C_{PCAP} is the value of the PLL capacitor (connected between the PCAP pin and V_{CCP}) computed using the appropriate expression listed above.

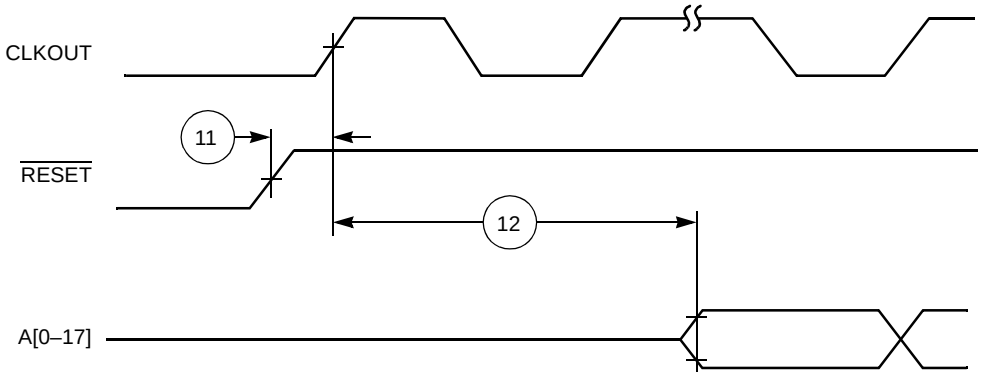
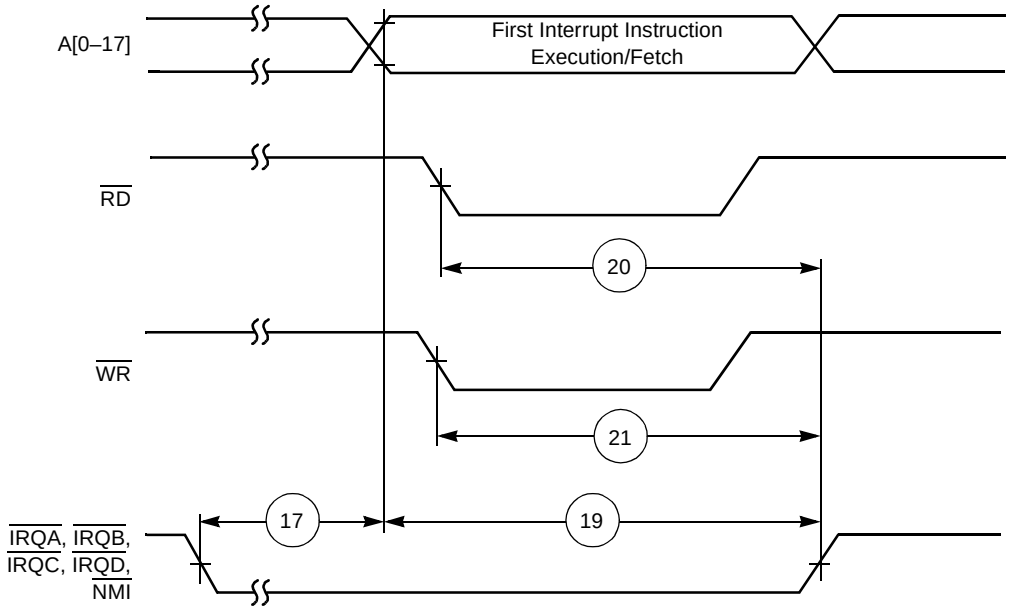
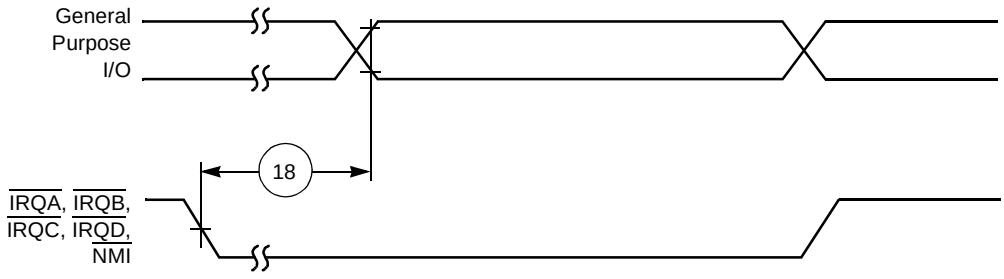


Figure 2-4. Synchronous Reset Timing



a) First Interrupt Instruction Execution



b) General-Purpose I/O

Figure 2-5. External Fast Interrupt Timing

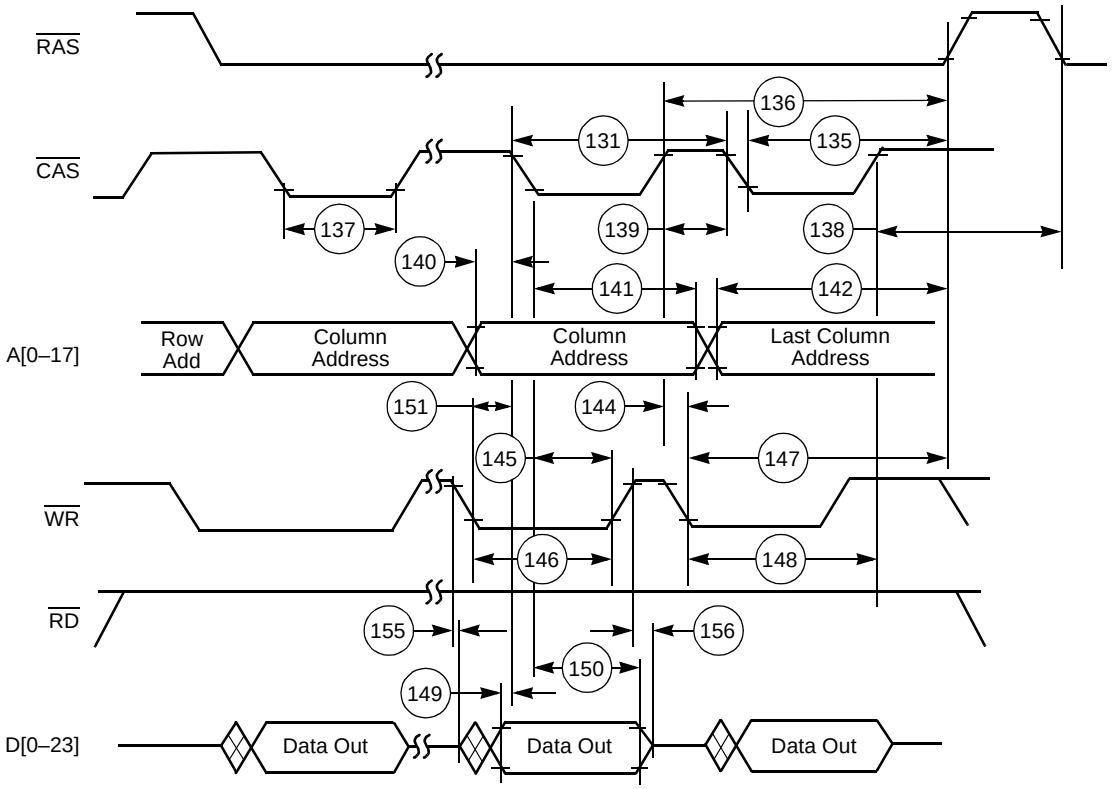


Figure 2-15. DRAM Page Mode Write Accesses

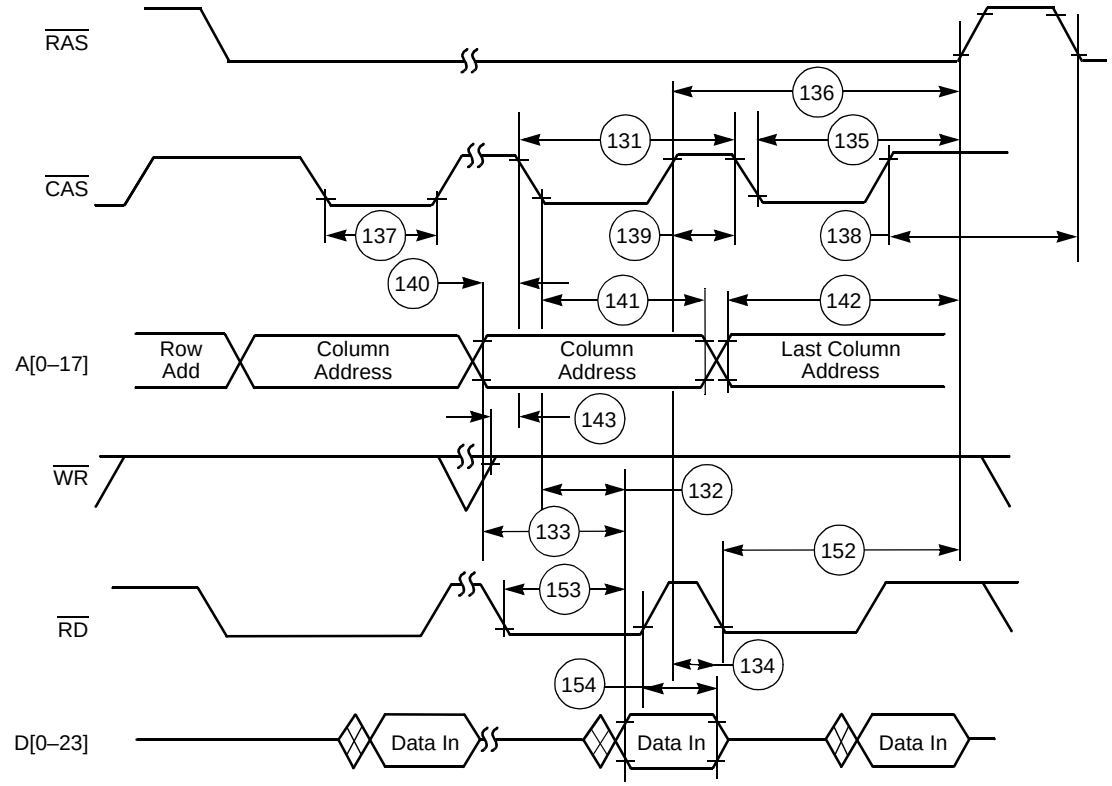


Figure 2-16. DRAM Page Mode Read Accesses

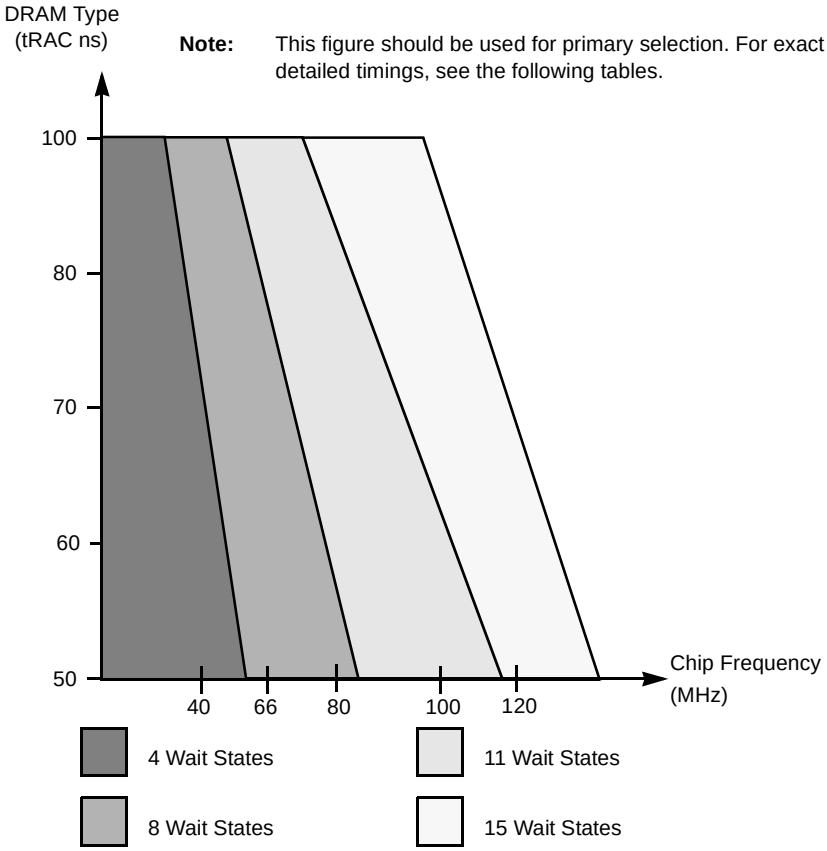


Figure 2-17. DRAM Out-of-Page Wait State Selection Guide

Table 2-11. DRAM Out-of-Page and Refresh Timings, Eleven Wait States[1,2]

No.	Characteristics	Symbol	Expression[3]	100 MHz		Unit
				Min	Max	
157	Random read or write cycle time	t_{RC}	$12 \times T_C$	120.0	—	ns
158	$\overline{RAS}$ assertion to data valid (read)	t_{RAC}	$6.25 \times T_C - 7.0$	—	55.5	ns
159	$\overline{CAS}$ assertion to data valid (read)	t_{CAC}	$3.75 \times T_C - 7.0$	—	30.5	ns
160	Column address valid to data valid (read)	t_{AA}	$4.5 \times T_C - 7.0$	—	38.0	ns
161	$\overline{CAS}$ deassertion to data not valid (read hold time)	t_{OFF}		0.0	—	ns
162	$\overline{RAS}$ deassertion to $\overline{RAS}$ assertion	t_{RP}	$4.25 \times T_C - 4.0$	38.5	—	ns
163	$\overline{RAS}$ assertion pulse width	t_{RAS}	$7.75 \times T_C - 4.0$	73.5	—	ns
164	$\overline{CAS}$ assertion to $\overline{RAS}$ deassertion	t_{RSH}	$5.25 \times T_C - 4.0$	48.5	—	ns
165	$\overline{RAS}$ assertion to $\overline{CAS}$ deassertion	t_{CSH}	$6.25 \times T_C - 4.0$	58.5	—	ns
166	$\overline{CAS}$ assertion pulse width	t_{CAS}	$3.75 \times T_C - 4.0$	33.5	—	ns
167	$\overline{RAS}$ assertion to $\overline{CAS}$ assertion	t_{RCD}	$2.5 \times T_C \pm 4.0$	21.0	29.0	ns
168	$\overline{RAS}$ assertion to column address valid	t_{RAD}	$1.75 \times T_C \pm 4.0$	13.5	21.5	ns
169	$\overline{CAS}$ deassertion to $\overline{RAS}$ assertion	t_{CRP}	$5.75 \times T_C - 4.0$	53.5	—	ns
170	$\overline{CAS}$ deassertion pulse width	t_{CP}	$4.25 \times T_C - 6.0$	36.5	—	ns

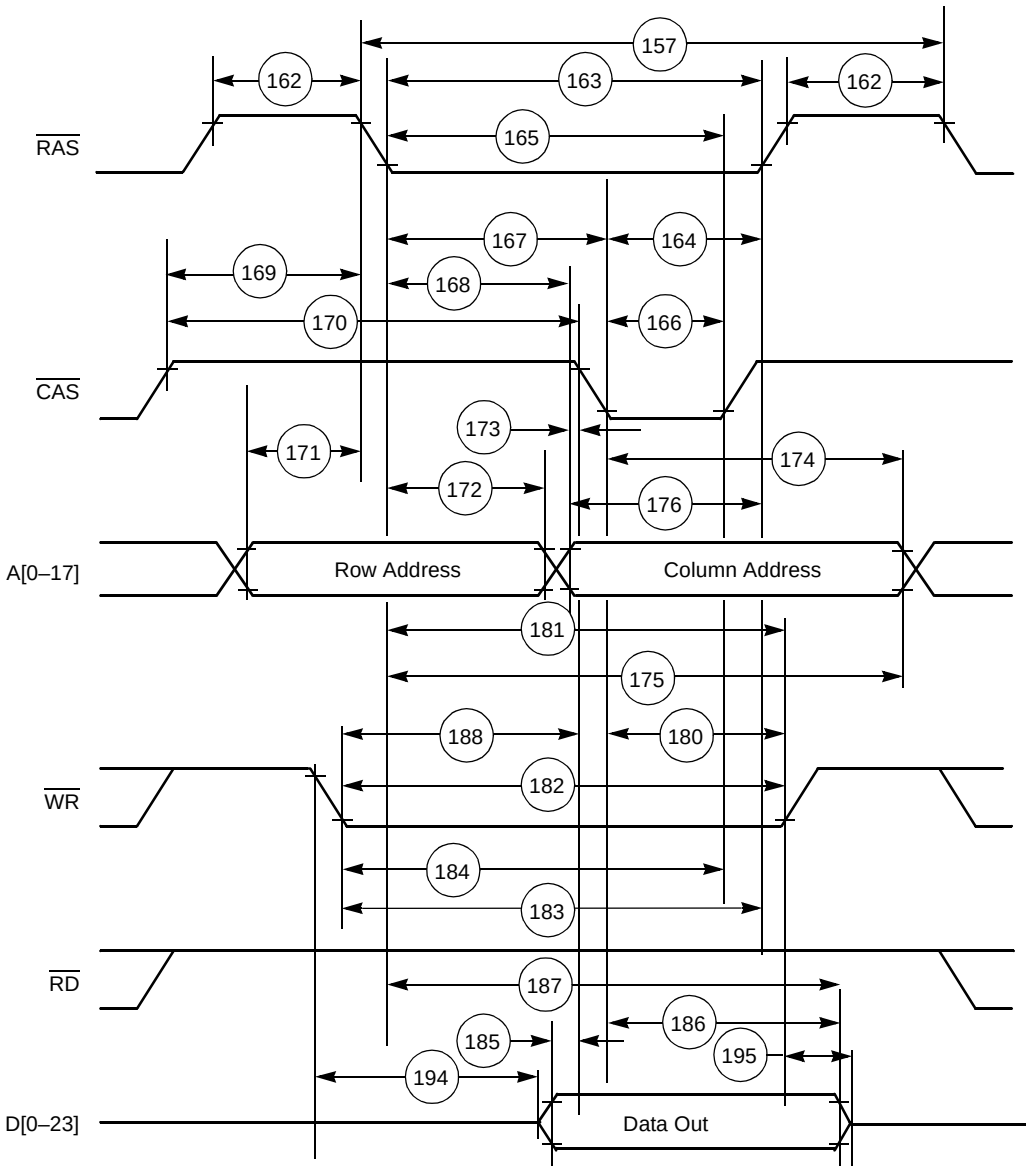


Figure 2-19. DRAM Out-of-Page Write Access

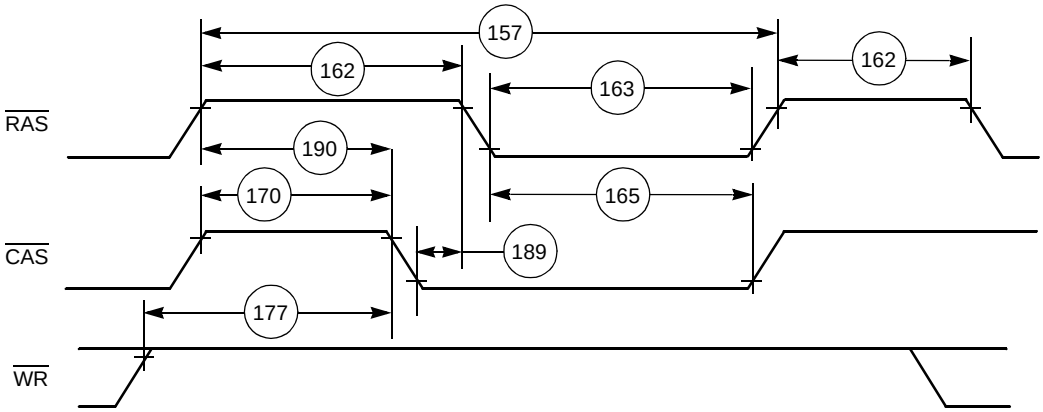


Figure 2-20. DRAM Refresh Access

2.6.5.3 Synchronous Timings

Table 2-13. External Bus Synchronous Timings[1,2]

No.	Characteristics	Expression[3,4,5]	100 MHz		Unit
			Min	Max	
198	CLKOUT high to address, and AA valid[6]	$0.25 \times T_C + 4.0$	—	6.5	ns
199	CLKOUT high to address, and AA invalid[6]	$0.25 \times T_C$	2.5	—	ns
200	$\overline{TA}$ valid to CLKOUT high (set-up time)		4.0	—	ns
201	CLKOUT high to $\overline{TA}$ invalid (hold time)		0.0	—	ns
202	CLKOUT high to data out active	$0.25 \times T_C$	2.5	—	ns
203	CLKOUT high to data out valid	$0.25 \times T_C + 4.0$	—	6.5	ns
204	CLKOUT high to data out invalid	$0.25 \times T_C$	2.5	—	ns
205	CLKOUT high to data out high impedance	$0.25 \times T_C$	—	2.5	ns
206	Data in valid to CLKOUT high (set-up)		4.0	—	ns
207	CLKOUT high to data in invalid (hold)		0.0	—	ns
208	CLKOUT high to $\overline{RD}$ assertion	maximum: $0.75 \times T_C + 2.5$	6.7	10.0	ns
209	CLKOUT high to $\overline{RD}$ deassertion		0.0	4.0	ns
210	CLKOUT high to $\overline{WR}$ assertion[2]	maximum: $0.5 \times T_C + 4.3$ for WS = 1 or WS ≥ 4 for 2 ≤ WS ≤ 3	5.0 0.0	9.3 4.3	ns ns
211	CLKOUT high to $\overline{WR}$ deassertion		0.0	3.8	ns

Notes:
1. Use external bus synchronous timings only for reference to the clock and *not* for relative timings.
2. Synchronous Bus Arbitration is not recommended. Use Asynchronous mode whenever possible.
3. WS is the number of wait states specified in the BCR.
4. If WS > 1, $\overline{WR}$ assertion refers to the next rising edge of CLKOUT.
5. Use the expression to compute the maximum or minimum value listed, as appropriate. For timing 210, the minimum is an absolute value.
6. T198 and T199 are valid for Address Trace mode if the ATE bit in the Operating Mode Register is set. when this mode is enabled, use the status of $\overline{BR}$ (See T212) to determine whether the access referenced by A[0–17] is internal or external.

2.6.5.4 Arbitration Timings

Table 2-14. Arbitration Bus Timings[1]

No.	Characteristics	Expression[2]	100 MHz		Unit
			Min	Max	
212	CLKOUT high to $\overline{BR}$ assertion/deassertion[3]		0.0	4.0	ns
213	$\overline{BG}$ asserted/deasserted to CLKOUT high (setup)		4.0	—	ns
214	CLKOUT high to $\overline{BG}$ deasserted/asserted (hold)		0.0	—	ns
215	$\overline{BB}$ deassertion to CLKOUT high (input set-up)		4.0	—	ns
216	CLKOUT high to $\overline{BB}$ assertion (input hold)		0.0	—	ns
217	CLKOUT high to $\overline{BB}$ assertion (output)		0.0	4.0	ns
218	CLKOUT high to $\overline{BB}$ deassertion (output)		0.0	4.0	ns
219	$\overline{BB}$ high to $\overline{BB}$ high impedance (output)		—	4.5	ns
220	CLKOUT high to address and controls active	$0.25 \times T_C$	2.5	—	ns
221	CLKOUT high to address and controls high impedance	$0.75 \times T_C$	—	7.5	ns
222	CLKOUT high to AA active	$0.25 \times T_C$	2.5	—	ns
223	CLKOUT high to AA deassertion	maximum: $0.25 \times T_C + 4.0$	2.0	6.5	ns
224	CLKOUT high to AA high impedance	$0.75 \times T_C$	—	7.5	ns

Notes:
1. Synchronous Bus Arbitration is not recommended. Use Asynchronous mode whenever possible.
2. An expression is used to compute the maximum or minimum value listed, as appropriate. For timing 223, the minimum is an absolute value.
3. T212 is valid for Address Trace mode when the ATE bit in the Operating Mode Register is set. $\overline{BR}$ is deasserted for internal accesses and asserted for external accesses.

2.6.5.5 Asynchronous Bus Arbitration Timings

Table 2-15. Asynchronous Bus Timings[1, 2]

No.	Characteristics	Expression[3]	100 MHz[4]		Unit
			Min	Max	
250	$\overline{BB}$ assertion window from $\overline{BG}$ input deassertion[5]	2.5 × Tc + 5	—	30	ns
251	Delay from $\overline{BB}$ assertion to $\overline{BG}$ assertion[5]	2 × Tc + 5	25	—	ns

Notes:
1. Bit 13 in the Operating Mode Register must be set to enter Asynchronous Arbitration mode.
2. If Asynchronous Arbitration mode is active, none of the timings in **Table 2-14** is required.
3. An expression is used to compute the maximum or minimum value listed, as appropriate.
4. Asynchronous Arbitration mode is recommended for operation at 100 MHz.
5. In order to guarantee timings 250, and 251, BG inputs must be asserted to different DSP56300 devices on the same bus in the non-overlap manner shown in **Figure 2-26**.

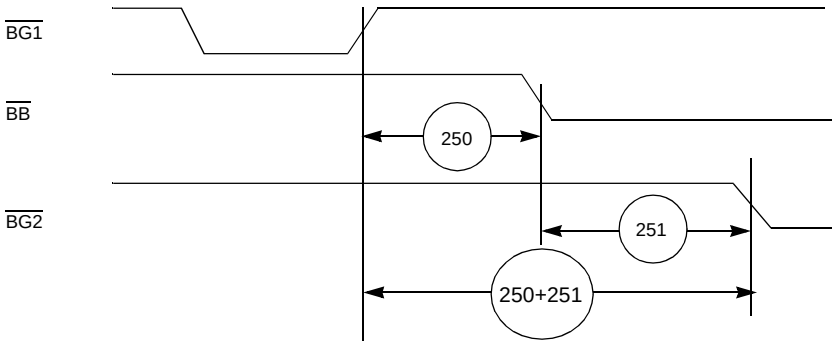


Figure 2-26. Asynchronous Bus Arbitration Timing

The asynchronous bus arbitration is enabled by internal synchronization circuits on $\overline{BG}$ and $\overline{BB}$ inputs. These synchronization circuits add delay from the external signal until it is exposed to internal logic. As a result of this delay, a DSP56300 part may assume mastership and assert $\overline{BB}$, for some time after $\overline{BG}$ is deasserted. This is the reason for timing 250.

Once $\overline{BB}$ is asserted, there is a synchronization delay from $\overline{BB}$ assertion to the time this assertion is exposed to other DSP56300 components that are potential masters on the same bus. If $\overline{BG}$ input is asserted before that time, and $\overline{BG}$ is asserted and $\overline{BB}$ is deasserted, another DSP56300 component may assume mastership at the same time. Therefore, some non-overlap period between one $\overline{BG}$ input active to another $\overline{BG}$ input active is required. Timing 251 ensures that overlaps are avoided.

2.6.7 SCI Timing

Table 2-17. SCI Timings

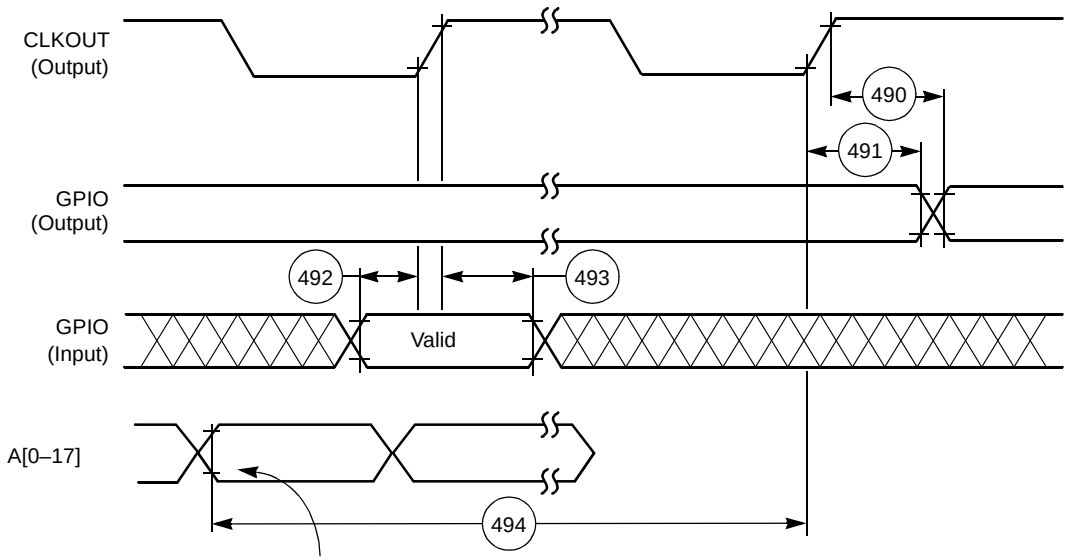
No.	Characteristics[1]	Symbol	Expression	100 MHz		Unit
				Min	Max	
400	Synchronous clock cycle	t_{SCC}[2]	$8 \times T_C$	53.3	—	ns
401	Clock low period		$t_{SCC}/2 - 10.0$	16.7	—	ns
402	Clock high period		$t_{SCC}/2 - 10.0$	16.7	—	ns
403	Output data setup to clock falling edge (internal clock)		$t_{SCC}/4 + 0.5 \times T_C - 17.0$	8.0	—	ns
404	Output data hold after clock rising edge (internal clock)		$t_{SCC}/4 - 0.5 \times T_C$	15.0	—	ns
405	Input data setup time before clock rising edge (internal clock)		$t_{SCC}/4 + 0.5 \times T_C + 25.0$	50.0	—	ns
406	Input data not valid before clock rising edge (internal clock)		$t_{SCC}/4 + 0.5 \times T_C - 5.5$	—	19.5	ns
407	Clock falling edge to output data valid (external clock)			—	32.0	ns
408	Output data hold after clock rising edge (external clock)		$T_C + 8.0$	18.0	—	ns
409	Input data setup time before clock rising edge (external clock)			0.0	—	ns
410	Input data hold time after clock rising edge (external clock)			9.0	—	ns
411	Asynchronous clock cycle	t_{ACC}[3]	$64 \times T_C$	640.0	—	ns
412	Clock low period		$t_{ACC}/2 - 10.0$	310.0	—	ns
413	Clock high period		$t_{ACC}/2 - 10.0$	310.0	—	ns
414	Output data setup to clock rising edge (internal clock)		$t_{ACC}/2 - 30.0$	290.0	—	ns
415	Output data hold after clock rising edge (internal clock)		$t_{ACC}/2 - 30.0$	290.0	—	ns

Notes:
1. $V_{CC} = 3.3\ V \pm 0.3\ V$; $T_J = -40°C$ to $+100\ °C$, $C_L = 50\ pF$.
2. t_{SCC} = synchronous clock cycle time (for internal clock, t_{SCC} is determined by the SCI clock control register and T_C).
3. t_{ACC} = asynchronous clock cycle time; value given for 1X Clock mode (for internal clock, t_{ACC} is determined by the SCI clock control register and T_C).
4. An expression is used to compute the number listed as the minimum or maximum value as appropriate.

2.6.10 GPIO Timing

Table 2-20. GPIO Timing

No.	Characteristics	Expression	100 MHz		Unit
			Min	Max	
490	CLKOUT edge to GPIO out valid (GPIO out delay time)		—	8.5	ns
491	CLKOUT edge to GPIO out not valid (GPIO out hold time)		0.0	—	ns
492	GPIO In valid to CLKOUT edge (GPIO in set-up time)		8.5	—	ns
493	CLKOUT edge to GPIO in not valid (GPIO in hold time)		0.0	—	ns
494	Fetch to CLKOUT edge before GPIO change	Minimum: $6.75 \times T_C$	67.5	—	ns
Note:	$V_{CC} = 3.3\ V \pm 0.3\ V$; $T_J = -40°C$ to $+100\ °C$, $C_L = 50\ pF$				



Fetch the instruction MOVE X0,X:(R0); X0 contains the new value of GPIO and R0 contains the address of the GPIO data register.

Figure 2-43. GPIO Timing

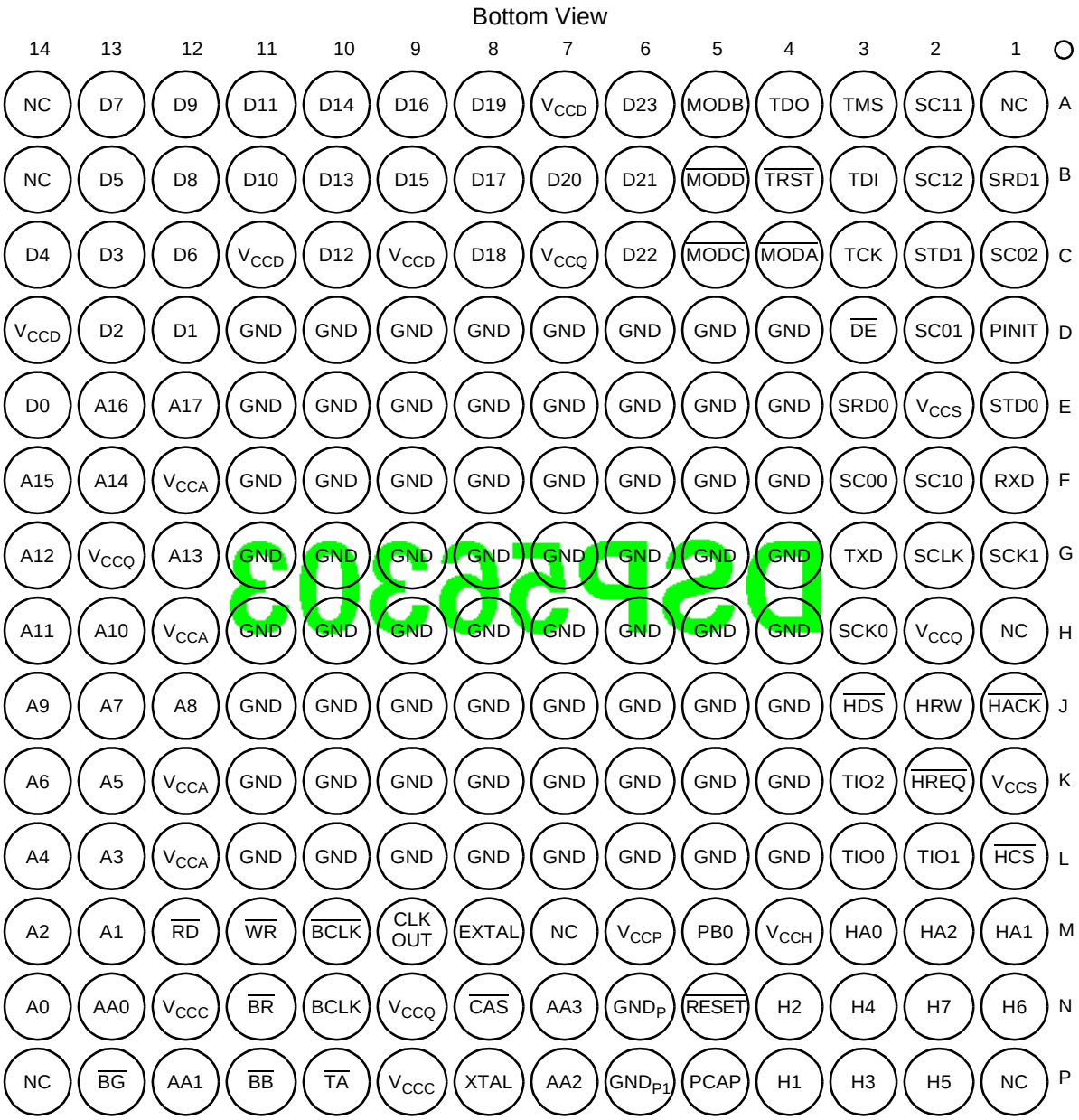


Figure 3-5. DSP56303 Molded Array Process-Ball Grid Array (MAP-BGA), Bottom View

Table 3-3. DSP56303 MAP-BGA Signal Identification by Pin Number

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
A1	Not Connected (NC), reserved	B12	D8	D9	GND
A2	SC11 or PD1	B13	D5	D10	GND
A3	TMS	B14	NC	D11	GND
A4	TDO	C1	SC02 or PC2	D12	D1
A5	MODB/$\overline{\text{IRQB}}$	C2	STD1 or PD5	D13	D2
A6	D23	C3	TCK	D14	V_{CCD}
A7	V_{CCD}	C4	MODA/$\overline{\text{IRQA}}$	E1	STD0 or PC5
A8	D19	C5	MODC/$\overline{\text{IRQC}}$	E2	V_{CCS}
A9	D16	C6	D22	E3	SRD0 or PC4
A10	D14	C7	V_{CCQ}	E4	GND
A11	D11	C8	D18	E5	GND
A12	D9	C9	V_{CCD}	E6	GND
A13	D7	C10	D12	E7	GND
A14	NC	C11	V_{CCD}	E8	GND
B1	SRD1 or PD4	C12	D6	E9	GND
B2	SC12 or PD2	C13	D3	E10	GND
B3	TDI	C14	D4	E11	GND
B4	$\overline{\text{TRST}}$	D1	PINIT/$\overline{\text{NMI}}$	E12	A17
B5	MODD/$\overline{\text{IRQD}}$	D2	SC01 or PC1	E13	A16
B6	D21	D3	$\overline{\text{DE}}$	E14	D0
B7	D20	D4	GND	F1	RXD or PE0
B8	D17	D5	GND	F2	SC10 or PD0
B9	D15	D6	GND	F3	SC00 or PC0
B10	D13	D7	GND	F4	GND
B11	D10	D8	GND	F5	GND

Table 3-4. DSP56303 MAP-BGA Signal Identification by Name

Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.
A0	N14	$\overline{BG}$	P13	D7	A13
A1	M13	$\overline{BR}$	N11	D8	B12
A10	H13	$\overline{CAS}$	N8	D9	A12
A11	H14	CLKOUT	M9	$\overline{DE}$	D3
A12	G14	D0	E14	EXTAL	M8
A13	G12	D1	D12	GND	D4
A14	F13	D10	B11	GND	D5
A15	F14	D11	A11	GND	D6
A16	E13	D12	C10	GND	D7
A17	E12	D13	B10	GND	D8
A2	M14	D14	A10	GND	D9
A3	L13	D15	B9	GND	D10
A4	L14	D16	A9	GND	D11
A5	K13	D17	B8	GND	E4
A6	K14	D18	C8	GND	E5
A7	J13	D19	A8	GND	E6
A8	J12	D2	D13	GND	E7
A9	J14	D20	B7	GND	E8
AA0	N13	D21	B6	GND	E9
AA1	P12	D22	C6	GND	E10
AA2	P7	D23	A6	GND	E11
AA3	N7	D3	C13	GND	F4
$\overline{BB}$	P11	D4	C14	GND	F5
$\overline{BCLK}$	M10	D5	B13	GND	F6
BCLK	N10	D6	C12	GND	F7

3.5 MAP-BGA Package Mechanical Drawing

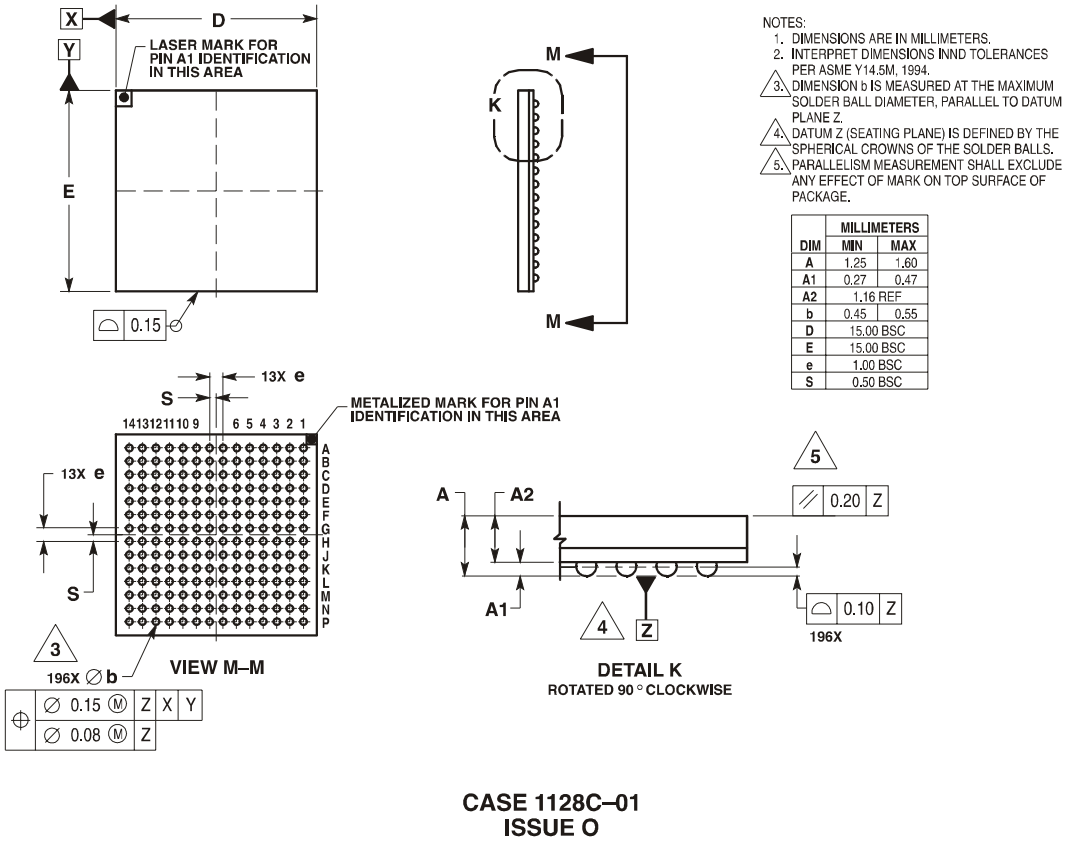


Figure 3-6. DSP56303 Mechanical Information, 196-pin MAP-BGA Package

A complicating factor is the existence of three common ways to determine the junction-to-case thermal resistance in plastic packages.

- To minimize temperature variation across the surface, the thermal resistance is measured from the junction to the outside surface of the package (case) closest to the chip mounting area when that surface has a proper heat sink.
- To define a value approximately equal to a junction-to-board thermal resistance, the thermal resistance is measured from the junction to the point at which the leads attach to the case.
- If the temperature of the package case (T_T) is determined by a thermocouple, thermal resistance is computed from the value obtained by the equation $(T_J - T_T)/P_D$.

As noted earlier, the junction-to-case thermal resistances quoted in this data sheet are determined using the first definition. From a practical standpoint, that value is also suitable to determine the junction temperature from a case thermocouple reading in forced convection environments. In natural convection, the use of the junction-to-case thermal resistance to estimate junction temperature from a thermocouple reading on the case of the package will yield an estimate of a junction temperature slightly higher than actual temperature. Hence, the new thermal metric, thermal characterization parameter or Ψ_{JT}, has been defined to be $(T_J - T_T)/P_D$. This value gives a better estimate of the junction temperature in natural convection when the surface temperature of the package is used. Remember that surface temperature readings of packages are subject to significant errors caused by inadequate attachment of the sensor to the surface and to errors caused by heat loss to the sensor. The recommended technique is to attach a 40-gauge thermocouple wire and bead to the top center of the package with thermally conductive epoxy.

4.2 Electrical Design Considerations

CAUTION

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, normal precautions are advised to avoid application of any voltages higher than maximum rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for example, either GND or V_{CC}).

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;------------------------------------------------------------------------
;
;       EQUATES for Serial Communications Interface (SCI)
;
;------------------------------------------------------------------------

;       Register Addresses

M_STXH EQU $FFFF97         ; SCI Transmit Data Register (high)
M_STXM EQU $FFFF96         ; SCI Transmit Data Register (middle)
M_STXL EQU $FFFF95         ; SCI Transmit Data Register (low)
M_SRXH EQU $FFFF9A         ; SCI Receive Data Register (high)
M_SRXM EQU $FFFF99         ; SCI Receive Data Register (middle)
M_SRXL EQU $FFFF98         ; SCI Receive Data Register (low)
M_STXA EQU $FFFF94        ; SCI Transmit Address Register
M_SCR EQU $FFFF9C         ; SCI Control Register
M_SSR EQU $FFFF93         ; SCI Status Register
M_SCCR EQU $FFFF9B         ; SCI Clock Control Register

;       SCI Control Register Bit Flags

M_WDS EQU $7              ; Word Select Mask (WDS0-WDS3)
M_WDS0 EQU 0               ; Word Select 0
M_WDS1 EQU 1               ; Word Select 1
M_WDS2 EQU 2           ; Word Select 2
M_SSFTD EQU 3         ; SCI Shift Direction
M_SBK EQU 4               ; Send Break
M_WAKE EQU 5               ; Wakeup Mode Select
M_RWU EQU 6               ; Receiver Wakeup Enable
M_WOMS EQU 7               ; Wired-OR Mode Select
M_SCRE EQU 8               ; SCI Receiver Enable
M_SCTE EQU 9               ; SCI Transmitter Enable
M_ILIE EQU 10              ; Idle Line Interrupt Enable
M_SCRIE EQU 11              ; SCI Receive Interrupt Enable
M_SCTIE EQU 12              ; SCI Transmit Interrupt Enable
M_TMIE EQU 13              ; Timer Interrupt Enable
M_TIR EQU 14              ; Timer Interrupt Rate
M_SCKP EQU 15              ; SCI Clock Polarity
M_REIE EQU 16              ; SCI Error Interrupt Enable (REIE)

;       SCI Status Register Bit Flags

M_TRNE EQU 0               ; Transmitter Empty
M_TDRE EQU 1               ; Transmit Data Register Empty
M_RDRF EQU 2               ; Receive Data Register Full
M_IDLE EQU 3               ; Idle Line Flag
M_OR EQU 4               ; Overrun Error Flag
M_PE EQU 5               ; Parity Error
M_FE EQU 6               ; Framing Error Flag
M_R8 EQU 7               ; Received Bit 8 (R8) Address

;       SCI Clock Control Register

M_CD EQU $FFF            ; Clock Divider Mask (CD0-CD11)
M_COD EQU 12              ; Clock Out Divider
M_SCP EQU 13              ; Clock Prescaler
M_RCM EQU 14              ; Receive Clock Mode Source Bit
M_TCM EQU 15              ; Transmit Clock Source Bit

;------------------------------------------------------------------------
;
;       EQUATES for Synchronous Serial Interface (SSI)
;
;------------------------------------------------------------------------

;
;       Register Addresses Of SSI0
M_TX00 EQU $FFFFBC         ; SSI0 Transmit Data Register 0
M_TX01 EQU $FFFFBB         ; SSIO Transmit Data Register 1
M_TX02 EQU $FFFFBA         ; SSIO Transmit Data Register 2
M_TSR0 EQU $FFFFB9         ; SSI0 Time Slot Register
M_RX0 EQU $FFFFB8         ; SSI0 Receive Data Register
M_SSISR0 EQU $FFFFB7   ; SSI0 Status Register
M_CRB0 EQU $FFFFB6          ; SSI0 Control Register B
M_CRA0 EQU $FFFFB5         ; SSI0 Control Register A
M_TSMA0 EQU $FFFFB4         ; SSI0 Transmit Slot Mask Register A
M_TSMB0 EQU $FFFFB3         ; SSI0 Transmit Slot Mask Register B
M_RSMA0 EQU $FFFFB2         ; SSI0 Receive Slot Mask Register A
M_RSMB0 EQU $FFFFB1         ; SSI0 Receive Slot Mask Register B
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M_DDR2 EQU $FFFFE6 ; DMA2 Destination Address Register
M_DCO2 EQU $FFFFE5 ; DMA2 Counter
M_DCR2 EQU $FFFFE4 ; DMA2 Control Register

;       Register Addresses Of DMA4

M_DSR3 EQU $FFFFE3 ; DMA3 Source Address Register
M_DDR3 EQU $FFFFE2 ; DMA3 Destination Address Register
M_DCO3 EQU $FFFFE1 ; DMA3 Counter
M_DCR3 EQU $FFFFE0 ; DMA3 Control Register

;       Register Addresses Of DMA4


M_DSR4 EQU $FFFFDF ; DMA4 Source Address Register
M_DDR4 EQU $FFFFDE ; DMA4 Destination Address Register
M_DCO4 EQU $FFFFDD ; DMA4 Counter
M_DCR4 EQU $FFFFDC ; DMA4 Control Register

;       Register Addresses Of DMA5

M_DSR5 EQU $FFFFDB ; DMA5 Source Address Register
M_DDR5 EQU $FFFFDA ; DMA5 Destination Address Register
M_DCO5 EQU $FFFFD9 ; DMA5 Counter
M_DCR5 EQU $FFFFD8 ; DMA5 Control Register

;       DMA Control Register

M_DSS EQU $3   ; DMA Source Space Mask (DSS0-Dss1)
M_DSS0 EQU 0   ; DMA Source Memory space 0
M_DSS1 EQU 1   ; DMA Source Memory space 1
M_DDS EQU $C   ; DMA Destination Space Mask (DDS-DDS1)
M_DDS0 EQU 2   ; DMA Destination Memory Space 0
M_DDS1 EQU 3   ; DMA Destination Memory Space 1
M_DAM EQU $3f0 ; DMA Address Mode Mask (DAM5-DAM0)
M_DAM0  EQU 4  ; DMA Address Mode 0
M_DAM1  EQU 5  ; DMA Address Mode 1
M_DAM2  EQU 6  ; DMA Address Mode 2
M_DAM3  EQU 7  ; DMA Address Mode 3
M_DAM4  EQU 8  ; DMA Address Mode 4
M_DAM5  EQU 9  ; DMA Address Mode 5
M_D3D EQU 10   ; DMA Three Dimensional Mode
M_DRS EQU $F800; DMA Request Source Mask (DRS0-DRS4)
M_DCON EQU 16  ; DMA Continuous Mode
M_DPR EQU $60000; DMA Channel Priority
M_DPR0 EQU 17  ; DMA Channel Priority Level (low)
M_DPR1 EQU 18  ; DMA Channel Priority Level (high)
M_DTM EQU $380000; DMA Transfer Mode Mask (DTM2-DTM0)
M_DTM0 EQU 19  ; DMA Transfer Mode 0
M_DTM1 EQU 20  ; DMA Transfer Mode 1
M_DTM2 EQU 21  ; DMA Transfer Mode 2
M_DIE EQU 22   ; DMA Interrupt Enable bit
M_DE EQU 23    ; DMA Channel Enable bit

;       DMA Status Register

M_DTD EQU $3F  ; Channel Transfer Done Status MASK (DTD0-DTD5)
M_DTD0 EQU 0   ; DMA Channel Transfer Done Status 0
M_DTD1 EQU 1   ; DMA Channel Transfer Done Status 1
M_DTD2 EQU 2   ; DMA Channel Transfer Done Status 2
M_DTD3 EQU 3   ; DMA Channel Transfer Done Status 3
M_DTD4 EQU 4   ; DMA Channel Transfer Done Status 4
M_DTD5 EQU 5   ; DMA Channel Transfer Done Status 5
M_DACT EQU  8  ; DMA Active State
M_DCH EQU  $E00; DMA Active Channel Mask (DCH0-DCH2)
M_DCH0 EQU  9  ; DMA Active Channel 0
M_DCH1 EQU  10 ; DMA Active Channel 1
M_DCH2 EQU  11 ; DMA Active Channel 2

;------------------------------------------------------------------------
;
;       EQUATES for Enhanced Filter Co-Processor (EFCOP)
;
;------------------------------------------------------------------------

M_FDIR   EQU     $FFFFB0         ; EFCOP Data Input Register
M_FDOR   EQU     $FFFFB1         ; EFCOP Data Output Register
M_FKIR   EQU     $FFFFB2         ; EFCOP K-Constant Register
M_FCNT   EQU     $FFFFB3         ; EFCOP Filter Counter
M_FCSR   EQU     $FFFFB4         ; EFCOP Control Status Register
M_FACR   EQU     $FFFFB5         ; EFCOP ALU Control Register
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M_FDBA   EQU     $FFFFB6         ; EFCOP Data Base Address
M_FCBA   EQU     $FFFFB7         ; EFCOP Coefficient Base Address
M_FDCH   EQU     $FFFFB8         ; EFCOP Decimation/Channel Register


;------------------------------------------------------------------------
;
;       EQUATES for Phase Locked Loop (PLL)
;
;------------------------------------------------------------------------

;       Register Addresses Of PLL

M_PCTL EQU $FFFFFD         ; PLL Control Register

;       PLL Control Register

M_MF EQU $FFF  : Multiplication Factor Bits Mask (MF0-MF11)
M_DF EQU $7000 ; Division Factor Bits Mask (DF0-DF2)
M_XTLR EQU 15  ; XTAL Range select bit
M_XTLD EQU 16  ; XTAL Disable Bit
M_PSTP EQU 17  ; STOP Processing State Bit
M_PEN EQU 18   ; PLL Enable Bit
M_PCOD EQU 19  ; PLL Clock Output Disable Bit
M_PD EQU $F00000; PreDivider Factor Bits Mask (PD0-PD3)



;------------------------------------------------------------------------
;
;       EQUATES for BIU
;
;------------------------------------------------------------------------

;       Register Addresses Of BIU


M_BCR EQU $FFFFFB; Bus Control Register
M_DCR EQU $FFFFFA; DRAM Control Register
M_AAR0 EQU $FFFFF9; Address Attribute Register 0
M_AAR1 EQU $FFFFF8; Address Attribute Register 1
M_AAR2 EQU $FFFFF7; Address Attribute Register 2
M_AAR3 EQU $FFFFF6; Address Attribute Register 3
M_IDR EQU  $FFFFF5 ; ID Register

;       Bus Control Register

M_BA0W EQU $1F ; Area 0 Wait Control Mask (BA0W0-BA0W4)
M_BA1W EQU $3E0; Area 1 Wait Control Mask (BA1W0-BA14)
M_BA2W EQU $1C00; Area 2 Wait Control Mask (BA2W0-BA2W2)
M_BA3W EQU $E000; Area 3 Wait Control Mask (BA3W0-BA3W3)
M_BDFW EQU $1F0000 ; Default Area Wait Control Mask (BDFW0-BDFW4)
M_BBS EQU 21   ; Bus State
M_BLH EQU 22   ; Bus Lock Hold
M_BRH EQU 23   ; Bus Request Hold

;       DRAM Control Register

M_BCW EQU $3   ; In Page Wait States Bits Mask (BCW0-BCW1)
M_BRW EQU $C   ; Out Of Page Wait States Bits Mask (BRW0-BRW1)
M_BPS EQU $300 ; DRAM Page Size Bits Mask (BPS0-BPS1)
M_BPLE EQU 11  ; Page Logic Enable
M_BME EQU 12   ; Mastership Enable
M_BRE EQU 13   ; Refresh Enable
M_BSTR EQU 14  ; Software Triggered Refresh
M_BRF EQU $7F8000; Refresh Rate Bits Mask (BRF0-BRF7)
M_BRP EQU 23   ; Refresh prescaler

;       Address Attribute Registers

M_BAT EQU $3   ; Ext. Access Type and Pin Def. Bits Mask (BAT0-BAT1)
M_BAAP EQU 2   ; Address Attribute Pin Polarity
M_BPEN EQU 3   ; Program Space Enable
M_BXEN EQU 4   ; X Data Space Enable
M_BYEN EQU 5   ; Y Data Space Enable
M_BAM EQU 6    ; Address Muxing
M_BPAC EQU 7   ; Packing Enable
M_BNC EQU $F00 ; Number of Address Bits to Compare Mask (BNC0-BNC3)
M_BAC EQU $FFF000; Address to Compare Bits Mask (BAC0-BAC11)
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Ordering Information

Consult a Motorola Semiconductor sales office or authorized distributor to determine product availability and place an order.

Part	Supply Voltage	Package Type	Pin Count	Core Frequency (MHz)	Order Number
DSP56303	3.3 V I/O	Thin Quad Flat Pack (TQFP)	144	100	DSP56303PV100
		Molded Array Process-Ball Grid Array (MAP-BGA)	196	100	DSP56303VF100

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