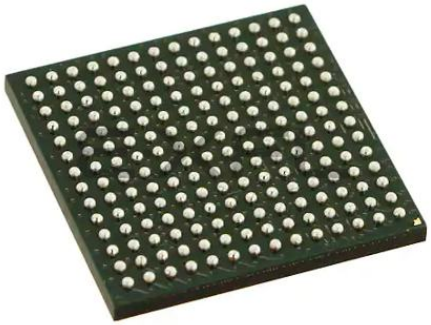

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Fixed Point
Interface	Host Interface, SSI, SCI
Clock Rate	100MHz
Non-Volatile Memory	ROM (576B)
On-Chip RAM	24kB
Voltage - I/O	3.30V
Voltage - Core	3.30V
Operating Temperature	-40°C ~ 105°C (TJ)
Mounting Type	Surface Mount
Package / Case	196-LBGA
Supplier Device Package	196-LBGA (15x15)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spakxc309vf100a

DSP56303 Features

High-Performance DSP56300 Core

- 100 million instructions per second (MIPS) with a 100 MHz clock at 3.3 V nominal
- Object code compatible with the DSP56000 core with highly parallel instruction set
- Data Arithmetic Logic Unit (Data ALU) with fully pipelined 24 × 24-bit parallel Multiplier-Accumulator (MAC), 56-bit parallel barrel shifter (fast shift and normalization; bit stream generation and parsing), conditional ALU instructions, and 24-bit or 16-bit arithmetic support under software control
- Program Control Unit (PCU) with Position Independent Code (PIC) support, addressing modes optimized for DSP applications (including immediate offsets), on-chip instruction cache controller, on-chip memory-expandable hardware stack, nested hardware DO loops, and fast auto-return interrupts
- Direct Memory Access (DMA) with six DMA channels supporting internal and external accesses; one-, two-, and three-dimensional transfers (including circular buffering); end-of-block-transfer interrupts; and triggering from interrupt lines and all peripherals
- Phase Lock Loop (PLL) allows change of low-power Divide Factor (DF) without loss of lock and output clock with skew elimination
- Hardware debugging support including On-Chip Emulation (OnCE™) module, Joint Test Action Group (JTAG) Test Access Port (TAP)

On-Chip Peripherals

- Enhanced DSP56000-like 8-bit parallel host interface (HI08) supports a variety of buses (for example, ISA) and provides glueless connection to a number of industry-standard microcomputers, microprocessors, and DSPs
- Two enhanced synchronous serial interfaces (ESSI), each with one receiver and three transmitters (allows six-channel home theater)
- Serial communications interface (SCI) with baud rate generator
- Triple timer module
- Up to thirty-four programmable general-purpose input/output (GPIO) pins, depending on which peripherals are enabled

On-Chip Memories

- 192 × 24-bit bootstrap ROM
- 128 K RAM total
- Program RAM, Instruction Cache, X data RAM, and Y data RAM sizes are programmable:

Program RAM Size	Instruction Cache Size	X Data RAM Size	Y Data RAM Size	Instruction Cache	Switch Mode
4096 × 24-bit	0	2048 × 24-bit	2048 × 24-bit	disabled	disabled
3072 × 24-bit	1024 × 24-bit	2048 × 24-bit	2048 × 24-bit	enabled	disabled
2048 × 24-bit	0	3072 × 24-bit	3072 × 24-bit	disabled	enabled
1024 × 24-bit	1024 × 24-bit	3072 × 24-bit	3072 × 24-bit	enabled	enabled

1.1 Signal Groupings

The DSP56303 input and output signals are organized into functional groups as shown in **Table 1-1**. **Figure 1-1** diagrams the DSP56303 signals by functional group. The remainder of this chapter describes the signal pins in each functional group.

Table 1-1. DSP56303 Functional Signal Groupings

Functional Group		Number of Signals	
		TQFP	MAP-BGA
Power (V_{CC})		18	18
Ground (GND)		19	66
Clock		2	2
PLL		3	3
Address bus	Port A[1]	18	18
Data bus		24	24
Bus control		13	13
Interrupt and mode control		5	5
Host interface (HI08)	Port B[2]	16	16
Enhanced synchronous serial interface (ESSI)	Ports C and D[3]	12	12
Serial communication interface (SCI)	Port E[4]	3	3
Timer		3	3
OnCE/JTAG Port		6	6

Notes:
1. Port A signals define the external memory interface port, including the external address bus, data bus, and control signals.
2. Port B signals are the HI08 port signals multiplexed with the GPIO signals.
3. Port C and D signals are the two ESSI port signals multiplexed with the GPIO signals.
4. Port E signals are the SCI port signals multiplexed with the GPIO signals.
5. There are 2 signal connections in the TQFP package and 7 signal connections in the MAP-BGA package that are not used. These are designated as no connect (NC) in the package description (see **Chapter 3**).

Note: This chapter refers to a number of configuration registers used to select individual multiplexed signal functionality. Refer to the *DSP56303 User's Manual* for details on these configuration registers.

1.9 Enhanced Synchronous Serial Interface 0 (ESSI0)

Two synchronous serial interfaces (ESSI0 and ESSI1) provide a full-duplex serial port for serial communication with a variety of serial devices, including one or more industry-standard codecs, other DSPs, microprocessors, and peripherals that implement the Motorola serial peripheral interface (SPI).

Table 1-12. Enhanced Synchronous Serial Interface 0

Signal Name	Type	State During Reset[1,2]	Signal Description
SC00	Input or Output	Ignored Input	**Serial Control 0**—For asynchronous mode, this signal is used for the receive clock I/O (Schmitt-trigger input). For synchronous mode, this signal is used either for transmitter 1 output or for serial I/O flag 0.
PC0	Input or Output		**Port C 0**—The default configuration following reset is GPIO input PC0. When configured as PC0, signal direction is controlled through the Port C Direction Register. The signal can be configured as ESSI signal SC00 through the Port C Control Register.
SC01	Input/Output	Ignored Input	**Serial Control 1**—For asynchronous mode, this signal is the receiver frame sync I/O. For synchronous mode, this signal is used either for transmitter 2 output or for serial I/O flag 1.
PC1	Input or Output		**Port C 1**—The default configuration following reset is GPIO input PC1. When configured as PC1, signal direction is controlled through the Port C Direction Register. The signal can be configured as an ESSI signal SC01 through the Port C Control Register.
SC02	Input/Output	Ignored Input	**Serial Control Signal 2**—The frame sync for both the transmitter and receiver in synchronous mode, and for the transmitter only in asynchronous mode. When configured as an output, this signal is the internally generated frame sync signal. When configured as an input, this signal receives an external frame sync signal for the transmitter (and the receiver in synchronous operation).
PC2	Input or Output		**Port C 2**—The default configuration following reset is GPIO input PC2. When configured as PC2, signal direction is controlled through the Port C Direction Register. The signal can be configured as an ESSI signal SC02 through the Port C Control Register.
SCK0	Input/Output	Ignored Input	**Serial Clock**—Provides the serial bit rate clock for the ESSI. The SCK0 is a clock input or output, used by both the transmitter and receiver in synchronous modes or by the transmitter in asynchronous modes. Although an external serial clock can be independent of and asynchronous to the DSP system clock, it must exceed the minimum clock cycle time of 6T (that is, the system clock frequency must be at least three times the external ESSI clock frequency). The ESSI needs at least three DSP phases inside each half of the serial clock.
PC3	Input or Output		**Port C 3**—The default configuration following reset is GPIO input PC3. When configured as PC3, signal direction is controlled through the Port C Direction Register. The signal can be configured as an ESSI signal SCK0 through the Port C Control Register.

Table 1-12. Enhanced Synchronous Serial Interface 0 (Continued)

Signal Name	Type	State During Reset[1,2]	Signal Description
SRD0	Input	Ignored Input	**Serial Receive Data**—Receives serial data and transfers the data to the ESSI Receive Shift Register. SRD0 is an input when data is received.
PC4	Input or Output		**Port C 4**—The default configuration following reset is GPIO input PC4. When configured as PC4, signal direction is controlled through the Port C Direction Register. The signal can be configured as an ESSI signal SRD0 through the Port C Control Register.
STD0	Output	Ignored Input	**Serial Transmit Data**—Transmits data from the Serial Transmit Shift Register. STD0 is an output when data is transmitted.
PC5	Input or Output		**Port C 5**—The default configuration following reset is GPIO input PC5. When configured as PC5, signal direction is controlled through the Port C Direction Register. The signal can be configured as an ESSI signal STD0 through the Port C Control Register.

Notes:
1. In the Stop state, the signal maintains the last state as follows:
- If the last state is input, the signal is an ignored input.
- If the last state is output, the signal is tri-stated.

2. The Wait processing state does not affect the signal state.
3. All inputs are 5 V tolerant.

1.10 Enhanced Synchronous Serial Interface 1 (ESSI1)

Table 1-13. Enhanced Serial Synchronous Interface 1

Signal Name	Type	State During Reset[1,2]	Signal Description
SC10	Input or Output	Ignored Input	**Serial Control 0**—For asynchronous mode, this signal is used for the receive clock I/O (Schmitt-trigger input). For synchronous mode, this signal is used either for transmitter 1 output or for serial I/O flag 0.
PD0	Input or Output		**Port D 0**—The default configuration following reset is GPIO input PD0. When configured as PD0, signal direction is controlled through the Port D Direction Register. The signal can be configured as an ESSI signal SC10 through the Port D Control Register.
SC11	Input/Output	Ignored Input	**Serial Control 1**—For asynchronous mode, this signal is the receiver frame sync I/O. For synchronous mode, this signal is used either for Transmitter 2 output or for Serial I/O Flag 1.
PD1	Input or Output		**Port D 1**—The default configuration following reset is GPIO input PD1. When configured as PD1, signal direction is controlled through the Port D Direction Register. The signal can be configured as an ESSI signal SC11 through the Port D Control Register.

Table 1-13. Enhanced Serial Synchronous Interface 1 (Continued)

Signal Name	Type	State During Reset[1,2]	Signal Description
SC12	Input/Output	Ignored Input	**Serial Control Signal 2**—The frame sync for both the transmitter and receiver in synchronous mode and for the transmitter only in asynchronous mode. When configured as an output, this signal is the internally generated frame sync signal. When configured as an input, this signal receives an external frame sync signal for the transmitter (and the receiver in synchronous operation).
PD2	Input or Output		**Port D 2**—The default configuration following reset is GPIO input PD2. When configured as PD2, signal direction is controlled through the Port D Direction Register. The signal can be configured as an ESSI signal SC12 through the Port D Control Register.
SCK1	Input/Output	Ignored Input	**Serial Clock**—Provides the serial bit rate clock for the ESSI. The SCK1 is a clock input or output used by both the transmitter and receiver in synchronous modes or by the transmitter in asynchronous modes. Although an external serial clock can be independent of and asynchronous to the DSP system clock, it must exceed the minimum clock cycle time of 6T (that is, the system clock frequency must be at least three times the external ESSI clock frequency). The ESSI needs at least three DSP phases inside each half of the serial clock.
PD3	Input or Output		**Port D 3**—The default configuration following reset is GPIO input PD3. When configured as PD3, signal direction is controlled through the Port D Direction Register. The signal can be configured as an ESSI signal SCK1 through the Port D Control Register.
SRD1	Input	Ignored Input	**Serial Receive Data**—Receives serial data and transfers the data to the ESSI Receive Shift Register. SRD1 is an input when data is being received.
PD4	Input or Output		**Port D 4**—The default configuration following reset is GPIO input PD4. When configured as PD4, signal direction is controlled through the Port D Direction Register. The signal can be configured as an ESSI signal SRD1 through the Port D Control Register.
STD1	Output	Ignored Input	**Serial Transmit Data**—Transmits data from the Serial Transmit Shift Register. STD1 is an output when data is being transmitted.
PD5	Input or Output		**Port D 5**—The default configuration following reset is GPIO input PD5. When configured as PD5, signal direction is controlled through the Port D Direction Register. The signal can be configured as an ESSI signal STD1 through the Port D Control Register.

Notes:
1. In the Stop state, the signal maintains the last state as follows:
- If the last state is input, the signal is an ignored input.
- If the last state is output, the signal is tri-stated.

2. The Wait processing state does not affect the signal state.
3. All inputs are 5 V tolerant.

2.6 AC Electrical Characteristics

The timing waveforms shown in the AC electrical characteristics section are tested with a V_{IL} maximum of 0.3 V and a V_{IH} minimum of 2.4 V for all pins except EXTAL, which is tested using the input levels shown in Note 6 of the previous table. AC timing specifications, which are referenced to a device input signal, are measured in production with respect to the 50 percent point of the respective input signal transition. DSP56303 output levels are measured with the production test machine V_{OL} and V_{OH} reference levels set at 0.4 V and 2.4 V, respectively.

Note: Although the minimum value for the frequency of EXTAL is 0 MHz, the device AC test conditions are 15 MHz and rated speed.

2.6.1 Internal Clocks

Table 2-4. Internal Clocks, CLKOUT

Characteristics	Symbol	Expression[1, 2]		
		Min	Typ	Max
Internal operation frequency and CLKOUT with PLL enabled	f	—	(Ef × MF)/ (PDF × DF)	—
Internal operation frequency and CLKOUT with PLL disabled	f	—	Ef/2	—
Internal clock and CLKOUT high period • With PLL disabled • With PLL enabled and MF ≤ 4 • With PLL enabled and MF > 4	T_H	 — 0.49 × ET_C × PDF × DF/MF 0.47 × ET_C × PDF × DF/MF	 ET_C — —	 — 0.51 × ET_C × PDF × DF/MF 0.53 × ET_C × PDF × DF/MF
Internal clock and CLKOUT low period • With PLL disabled • With PLL enabled and MF ≤ 4 • With PLL enabled and MF > 4	T_L	 — 0.49 × ET_C × PDF × DF/MF 0.47 × ET_C × PDF × DF/MF	 ET_C — —	 — 0.51 × ET_C × PDF × DF/MF 0.53 × ET_C × PDF × DF/MF
Internal clock and CLKOUT cycle time with PLL enabled	T_C	—	ET_C × PDF × DF/MF	—
Internal clock and CLKOUT cycle time with PLL disabled	T_C	—	2 × ET_C	—
Instruction cycle time	I_{CYC}	—	T_C	—

Notes: **1.** DF = Division Factor; Ef = External frequency; ET_C = External clock cycle; MF = Multiplication Factor; PDF = Predivision Factor; T_C = internal clock cycle

2. See the PLL and Clock Generation section in the *DSP56300 Family Manual* for a detailed discussion of the PLL.

Table 2-7. Reset, Stop, Mode Select, and Interrupt Timing[6] (Continued)

No.	Characteristics	Expression	100 MHz		Unit
			Min	Max	

Notes:

1. When fast interrupts are used and $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$, $\overline{\text{IRQC}}$, and $\overline{\text{IRQD}}$ are defined as level-sensitive, timings 19 through 21 apply to prevent multiple interrupt service. To avoid these timing restrictions, the deasserted Edge-triggered mode is recommended when fast interrupts are used. Long interrupts are recommended for Level-sensitive mode.

2. This timing depends on several settings:
- For PLL disable, using internal oscillator (PLL Control Register (PCTL) Bit 16 = 0) and oscillator disabled during Stop (PCTL Bit 17 = 0), a stabilization delay is required to assure that the oscillator is stable before programs are executed. Resetting the Stop delay (Operating Mode Register Bit 6 = 0) provides the proper delay. While Operating Mode Register Bit 6 = 1 can be set, it is not recommended, and these specifications do not guarantee timings for that case.
- For PLL disable, using internal oscillator (PCTL Bit 16 = 0) and oscillator enabled during Stop (PCTL Bit 17=1), no stabilization delay is required and recovery is minimal (Operating Mode Register Bit 6 setting is ignored).
- For PLL disable, using external clock (PCTL Bit 16 = 1), no stabilization delay is required and recovery time is defined by the PCTL Bit 17 and Operating Mode Register Bit 6 settings.
- For PLL enable, if PCTL Bit 17 is 0, the PLL is shutdown during Stop. Recovering from Stop requires the PLL to get locked. The PLL lock procedure duration, PLL Lock Cycles (PLC), may be in the range of 0 to 1000 cycles. This procedure occurs in parallel with the stop delay counter, and stop recovery ends when the last of these two events occurs. The stop delay counter completes count or PLL lock procedure completion.
- PLC value for PLL disable is 0.
- The maximum value for ET_C is 4096 (maximum MF) divided by the desired internal frequency (that is, for 66 MHz it is 4096/66 MHz = 62 µs). During the stabilization period, T_C, T_H, and T_L is not constant, and their width may vary, so timing may vary as well.

3. Periodically sampled and not 100 percent tested.

4. Value depends on clock source:
- For an external clock generator, $\overline{\text{RESET}}$ duration is measured while $\overline{\text{RESET}}$ is asserted, V_{CC} is valid, and the EXTAL input is active and valid.
- For an internal oscillator, $\overline{\text{RESET}}$ duration is measured while $\overline{\text{RESET}}$ is asserted and V_{CC} is valid. The specified timing reflects the crystal oscillator stabilization time after power-up. This number is affected both by the specifications of the crystal and other components connected to the oscillator and reflects worst case conditions.
- When the V_{CC} is valid, but the other "required $\overline{\text{RESET}}$ duration" conditions (as specified above) have not been yet met, the device circuitry is in an uninitialized state that can result in significant power consumption and heat-up. Designs should minimize this state to the shortest possible duration.

5. If PLL does not lose lock.

6. V_{CC} = 3.3 V ± 0.3 V; T_J = –40°C to +100°C, C_L = 50 pF.

7. WS = number of wait states (measured in clock cycles, number of T_C).

8. Use the expression to compute a maximum value.

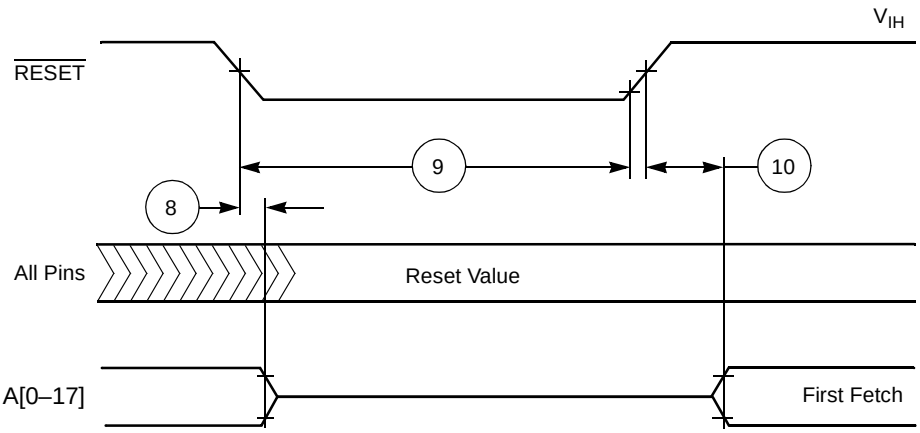


Figure 2-3. Reset Timing

2.6.6 Host Interface Timing

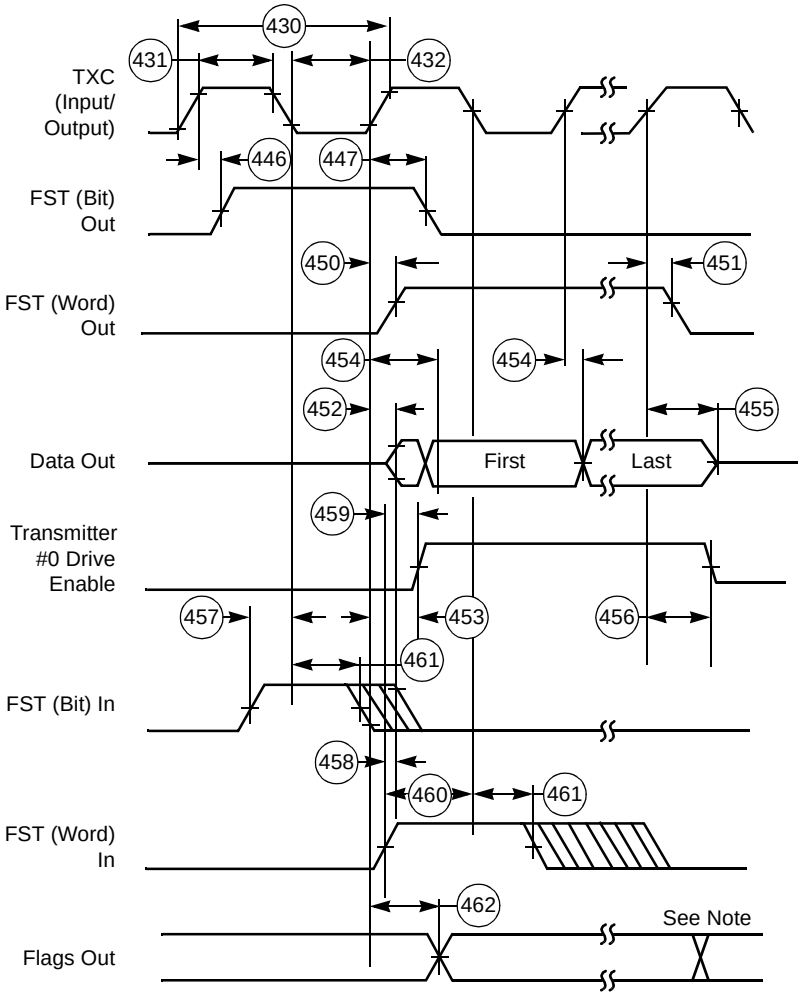
Table 2-16. Host Interface Timings[1,2,12]

No.	Characteristic[10]	Expression	100 MHz		Unit
			Min	Max	
317	Read data strobe assertion width[5] HACK assertion width	$T_C + 9.9$	19.9	—	ns
318	Read data strobe deassertion width[5] HACK deassertion width		9.9	—	ns
319	Read data strobe deassertion width[5] after “Last Data Register” reads[8,11], or between two consecutive CVR, ICR, or ISR reads[3] HACK deassertion width after “Last Data Register” reads[8,11]	$2.5 \times T_C + 6.6$	31.6	—	ns
320	Write data strobe assertion width[6]		13.2	—	ns
321	Write data strobe deassertion width[8] HACK write deassertion width • after ICR, CVR and “Last Data Register” writes • after IVR writes, or after TXH:TXM:TXL writes (with HLEND= 0), or after TXL:TXM:TXH writes (with HLEND = 1)	$2.5 \times T_C + 6.6$	31.8 16.5	— —	ns ns
322	HAS assertion width		9.9	—	ns
323	HAS deassertion to data strobe assertion[4]		0.0	—	ns
324	Host data input setup time before write data strobe deassertion[6]		9.9	—	ns
325	Host data input hold time after write data strobe deassertion[6]		3.3	—	ns
326	Read data strobe assertion to output data active from high impedance[5] HACK assertion to output data active from high impedance		3.3	—	ns
327	Read data strobe assertion to output data valid[5] HACK assertion to output data valid		—	24.5	ns
328	Read data strobe deassertion to output data high impedance[5] HACK deassertion to output data high impedance		—	9.9	ns
329	Output data hold time after read data strobe deassertion[5] Output data hold time after HACK deassertion		3.3	—	ns
330	HCS assertion to read data strobe deassertion[5]	$T_C + 9.9$	19.9	—	ns
331	HCS assertion to write data strobe deassertion[6]		9.9	—	ns
332	HCS assertion to output data valid		—	19.3	ns
333	HCS hold time after data strobe deassertion[4]		0.0	—	ns
334	Address (HAD[0–7]) setup time before HAS deassertion (HMUX=1)		4.6	—	ns
335	Address (HAD[0–7]) hold time after HAS deassertion (HMUX=1)		3.3	—	ns
336	HA[8–10] (HMUX=1), HA[0–2] (HMUX=0), HR/W setup time before data strobe assertion[4] • Read • Write		 0 4.6	 — —	 ns ns
337	HA[8–10] (HMUX=1), HA[0–2] (HMUX=0), HR/W hold time after data strobe deassertion[4]		3.3	—	ns

2.6.8 ESSI0/ESSI1 Timing

Table 2-18. ESSI Timings

No.	Characteristics[4, 5, 7]	Symbol	Expression[9]	100 MHz		Cond-ition[5]	Unit
				Min	Max		
430	Clock cycle[1]	t_{SSICC}	$3 \times T_C$ $4 \times T_C$	30.0 40.0	— —	x ck i ck	ns
431	Clock high period • For internal clock • For external clock		 $2 \times T_C$ - 10.0 $1.5 \times T_C$	 10.0 15.0	 — —		 ns ns
432	Clock low period • For internal clock • For external clock		 $2 \times T_C$ – 10.0 $1.5 \times T_C$	 10.0 15.0	 — —		 ns ns
433	RXC rising edge to FSR out (bit-length) high			— —	37.0 22.0	x ck i ck a	ns
434	RXC rising edge to FSR out (bit-length) low			— —	37.0 22.0	x ck i ck a	ns
435	RXC rising edge to FSR out (word-length-relative) high[2]			— —	39.0 37.0	x ck i ck a	ns
436	RXC rising edge to FSR out (word-length-relative) low[2]			— —	39.0 37.0	x ck i ck a	ns
437	RXC rising edge to FSR out (word-length) high			— —	36.0 21.0	x ck i ck a	ns
438	RXC rising edge to FSR out (word-length) low			— —	37.0 22.0	x ck i ck a	ns
439	Data in setup time before RXC (SCK in Synchronous mode) falling edge			10.0 19.0	— —	x ck i ck	ns
440	Data in hold time after RXC falling edge			5.0 3.0	— —	x ck i ck	ns
441	FSR input (bl, wr) high before RXC falling edge[2]			1.0 23.0	— —	x ck i ck a	ns
442	FSR input (wl) high before RXC falling edge			3.5 23.0	— —	x ck i ck a	ns
443	FSR input hold time after RXC falling edge			3.0 0.0	— —	x ck i ck a	ns
444	Flags input setup before RXC falling edge			5.5 19.0	— —	x ck i ck s	ns
445	Flags input hold time after RXC falling edge			6.0 0.0	— —	x ck i ck s	ns
446	TXC rising edge to FST out (bit-length) high			— —	29.0 15.0	x ck i ck	ns
447	TXC rising edge to FST out (bit-length) low			— —	31.0 17.0	x ck i ck	ns
448	TXC rising edge to FST out (word-length-relative) high[2]			— —	31.0 17.0	x ck i ck	ns
449	TXC rising edge to FST out (word-length-relative) low[2]			— —	33.0 19.0	x ck i ck	ns



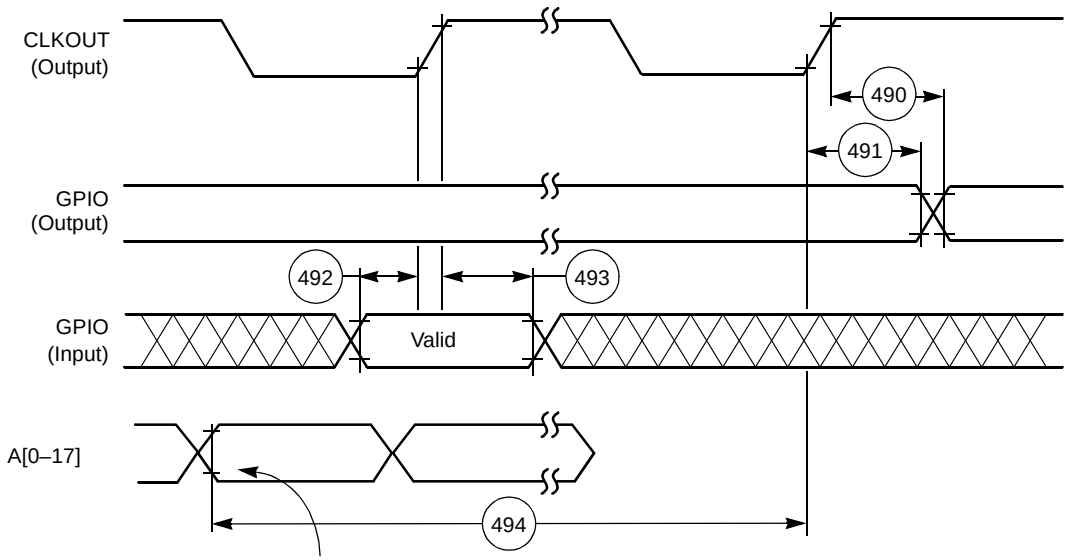
Note: In Network mode, output flag transitions can occur at the start of each time slot within the frame. In Normal mode, the output flag state is asserted for the entire frame period.

Figure 2-38. ESSI Transmitter Timing

2.6.10 GPIO Timing

Table 2-20. GPIO Timing

No.	Characteristics	Expression	100 MHz		Unit
			Min	Max	
490	CLKOUT edge to GPIO out valid (GPIO out delay time)		—	8.5	ns
491	CLKOUT edge to GPIO out not valid (GPIO out hold time)		0.0	—	ns
492	GPIO In valid to CLKOUT edge (GPIO in set-up time)		8.5	—	ns
493	CLKOUT edge to GPIO in not valid (GPIO in hold time)		0.0	—	ns
494	Fetch to CLKOUT edge before GPIO change	Minimum: $6.75 \times T_C$	67.5	—	ns
Note:	$V_{CC} = 3.3\ V \pm 0.3\ V$; $T_J = -40°C$ to $+100\ °C$, $C_L = 50\ pF$				



Fetch the instruction MOVE X0,X:(R0); X0 contains the new value of GPIO and R0 contains the address of the GPIO data register.

Figure 2-43. GPIO Timing

2.6.11 JTAG Timing

Table 2-21. JTAG Timing

No.	Characteristics	All frequencies		Unit
		Min	Max	
500	TCK frequency of operation	0.0	22.0	MHz
501	TCK cycle time in Crystal mode	45.0	—	ns
502	TCK clock pulse width measured at 1.5 V	20.0	—	ns
503	TCK rise and fall times	0.0	3.0	ns
504	Boundary scan input data setup time	5.0	—	ns
505	Boundary scan input data hold time	24.0	—	ns
506	TCK low to output data valid	0.0	40.0	ns
507	TCK low to output high impedance	0.0	40.0	ns
508	TMS, TDI data setup time	5.0	—	ns
509	TMS, TDI data hold time	25.0	—	ns
510	TCK low to TDO data valid	0.0	44.0	ns
511	TCK low to TDO high impedance	0.0	44.0	ns
512	$\overline{\text{TRST}}$ assert time	100.0	—	ns
513	$\overline{\text{TRST}}$ setup time to TCK low	40.0	—	ns

Notes: **1.** V_{CC} = 3.3 V ± 0.3 V; T_J = –40°C to +100 °C, C_L = 50 pF
2. All timings apply to OnCE module data transfers because it uses the JTAG port as an interface.

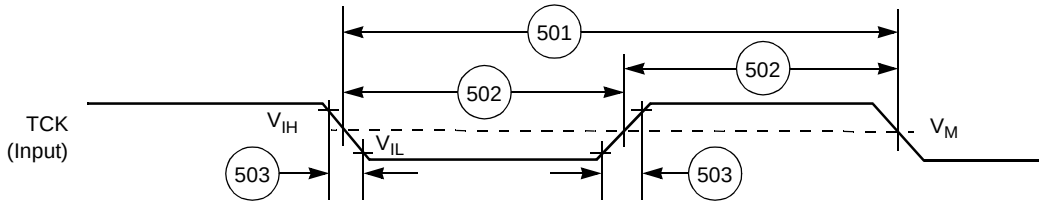


Figure 2-44. Test Clock Input Timing Diagram

Chapter 3

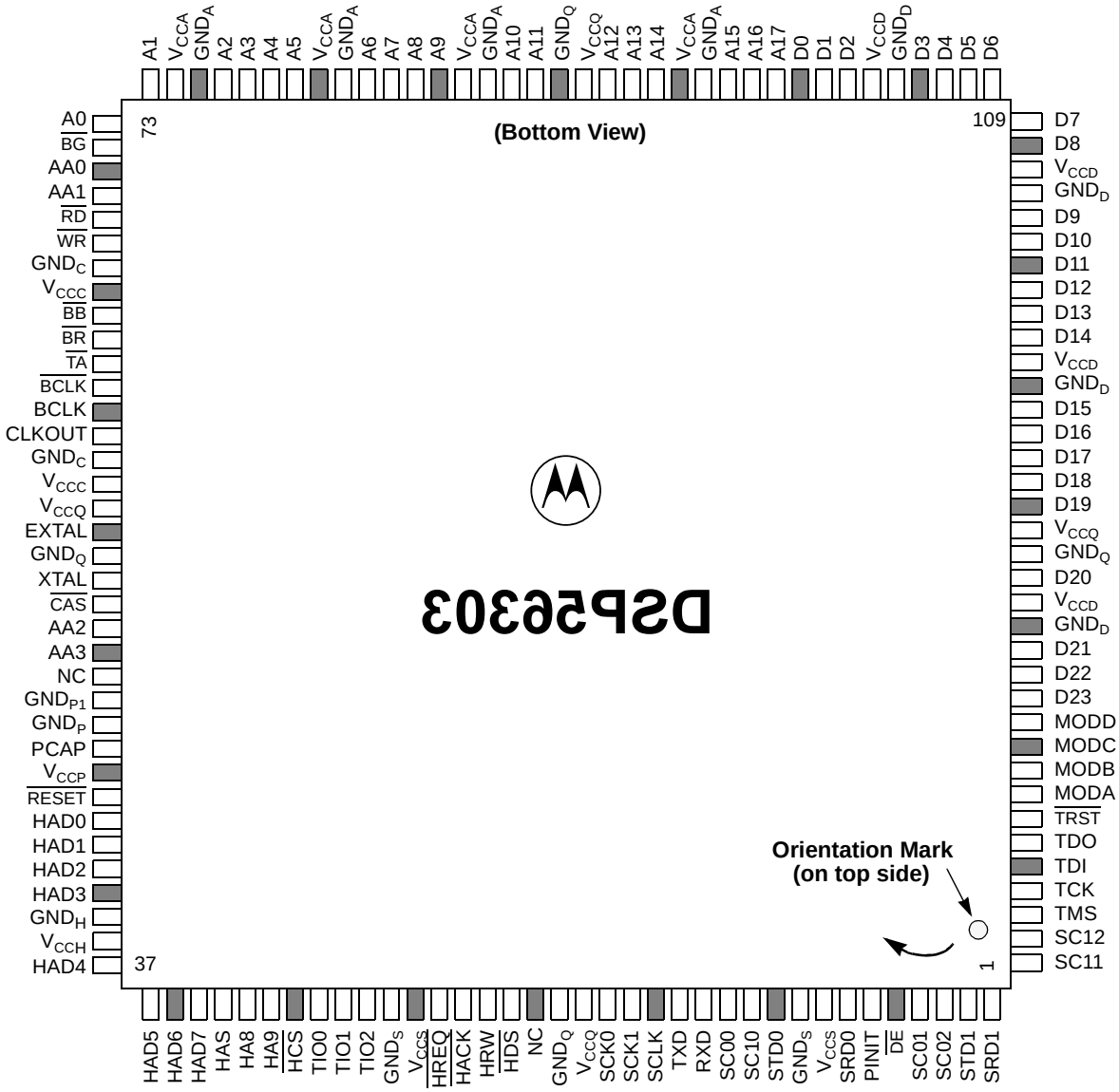
Packaging

3.1 Pin-Out and Package Information

This section includes diagrams of the DSP56303 package pin-outs and tables showing how the signals described in **Chapter 1** are allocated for each package.

The DSP56303 is available in two package types:

- 144-pin Thin Quad Flat Pack (TQFP)
- 196-pin Molded Array Process-Ball Grid Array (MAP-BGA)



Notes: Because of size constraints in this figure, only one name is shown for multiplexed pins. Refer to **Table 3-1** and **Table 3-2** for detailed information about pin functions and signal names.

Figure 3-2. DSP56303 Thin Quad Flat Pack (TQFP), Bottom View

Table 3-3. DSP56303 MAP-BGA Signal Identification by Pin Number (Continued)

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
F6	GND	H3	SCK0 or PC3	J14	A9
F7	GND	H4	GND	K1	V_{CCS}
F8	GND	H5	GND	K2	$\overline{\text{HREQ}}$/HREQ, $\overline{\text{HTRQ}}$/HTRQ, or PB14
F9	GND	H6	GND	K3	TIO2
F10	GND	H7	GND	K4	GND
F11	GND	H8	GND	K5	GND
F12	V_{CCA}	H9	GND	K6	GND
F13	A14	H10	GND	K7	GND
F14	A15	H11	GND	K8	GND
G1	SCK1 or PD3	H12	V_{CCA}	K9	GND
G2	SCLK or PE2	H13	A10	K10	GND
G3	TXD or PE1	H14	A11	K11	GND
G4	GND	J1	$\overline{\text{HACK}}$/HACK, $\overline{\text{HRRQ}}$/HRRQ, or PB15	K12	V_{CCA}
G5	GND	J2	HRW, $\overline{\text{HRD}}$/HRD, or PB11	K13	A5
G6	GND	J3	$\overline{\text{HDS}}$/HDS, $\overline{\text{HWR}}$/HWR, or PB12	K14	A6
G7	GND	J4	GND	L1	$\overline{\text{HCS}}$/HCS, HA10, or PB13
G8	GND	J5	GND	L2	TIO1
G9	GND	J6	GND	L3	TIO0
G10	GND	J7	GND	L4	GND
G11	GND	J8	GND	L5	GND
G12	A13	J9	GND	L6	GND
G13	V_{CCQ}	J10	GND	L7	GND
G14	A12	J11	GND	L8	GND
H1	NC	J12	A8	L9	GND
H2	V_{CCQ}	J13	A7	L10	GND
L11	GND	M13	A1	P1	NC
L12	V_{CCA}	M14	A2	P2	H5, HAD5, or PB5
L13	A3	N1	H6, HAD6, or PB6	P3	H3, HAD3, or PB3

MAP-BGA Package Mechanical Drawing

Appendix A

Power Consumption Benchmark

The following benchmark program evaluates DSP56303 power use in a test situation. It enables the PLL, disables the external clock, and uses repeated multiply-accumulate (MAC) instructions with a set of synthetic DSP application data to emulate intensive sustained DSP operation.

```
;*************************************************************************
;*************************************************************************
;*                                                                       *
;* CHECKS   Typical Power Consumption                                    *
;*                                                                       *
;*************************************************************************

        page    200,55,0,0,0
        nolist

I_VEC EQU $000000; Interrupt vectors for program debug only
START EQU $8000; MAIN (external) program starting address
INT_PROG  EQU $100 ; INTERNAL program memory starting address
INT_XDAT  EQU $0; INTERNAL X-data memory starting address
INT_YDAT  EQU $0; INTERNAL Y-data memory starting address

        INCLUDE "ioequ.asm"
        INCLUDE "intequ.asm"

        list

        org     P:START
;
        movep #$0243FF,x:M_BCR ;; BCR: Area 3 = 2 w.s (SRAM)
; Default: 2w.s (SRAM)
;
        movep   #$0d0000,x:M_PCTL       ; XTAL disable
                                        ; PLL enable
                                        ; CLKOUT disable
;
; Load the program
;
        move    #INT_PROG,r0
        move    #PROG_START,r1
        do      #(PROG_END-PROG_START),PLOAD_LOOP
        move    p:(r1)+,x0
        move    x0,p:(r0)+
        nop
PLOAD_LOOP
;
; Load the X-data
;
        move    #INT_XDAT,r0
        move    #XDAT_START,r1
        do      #(XDAT_END-XDAT_START),XLOAD_LOOP
        move    p:(r1)+,x0
        move    x0,x:(r0)+
XLOAD_LOOP
;
; Load the Y-data
;
        move    #INT_YDAT,r0
        move    #YDAT_START,r1
        do      #(YDAT_END-YDAT_START),YLOAD_LOOP
        move    p:(r1)+,x0
        move    x0,y:(r0)+
YLOAD_LOOP
;

        jmp     INT_PROG

PROG_START
        move    #$0,r0
        move    #$0,r4
        move    #$3f,m0
        move    #$3f,m4
;
        clr     a
```

```
        dc      $EB3B4B
        dc      $2DA928
        dc      $AB6641
        dc      $28A7E6
        dc      $4E2127
        dc      $482FD4
        dc      $7257D
        dc      $E53C72
        dc      $1A8C3
        dc      $E27540
XDAT_END

YDAT_START
;       org     y:0
        dc      $5B6DA
        dc      $C3F70B
        dc      $6A39E8
        dc      $81E801
        dc      $C666A6
        dc      $46F8E7
        dc      $AAEC94
        dc      $24233D
        dc      $802732
        dc      $2E3C83
        dc      $A43E00
        dc      $C2B639
        dc      $85A47E
        dc      $ABFDDF
        dc      $F3A2C
        dc      $2D7CF5
        dc      $E16A8A
        dc      $ECB8FB
        dc      $4BED18
        dc      $43F371
        dc      $83A556
        dc      $E1E9D7
        dc      $ACA2C4
        dc      $8135AD
        dc      $2CE0E2
        dc      $8F2C73
        dc      $432730
        dc      $A87FA9
        dc      $4A292E
        dc      $A63CCF
        dc      $6BA65C
        dc      $E06D65
        dc      $1AA3A
        dc      $A1B6EB
        dc      $48AC48
        dc      $EF7AE1
        dc      $6E3006
        dc      $62F6C7
        dc      $6064F4
        dc      $87E41D
        dc      $CB2692
        dc      $2C3863
        dc      $C6BC60
        dc      $43A519
        dc      $6139DE
        dc      $ADF7BF
        dc      $4B3E8C
        dc      $6079D5
        dc      $E0F5EA
        dc      $8230DB
        dc      $A3B778
        dc      $2BFE51
        dc      $E0A6B6
        dc      $68FFB7
        dc      $28F324
        dc      $8F2E8D
        dc      $667842
        dc      $83E053
        dc      $A1FD90
        dc      $6B2689
        dc      $85B68E
        dc      $622EAF
        dc      $6162BC
        dc      $E4A245
YDAT_END

;************************************************************************
```

```
;       control and status bits in SR

M_CP EQU $c00000; mask for CORE-DMA priority bits in SR
M_CA EQU 0      ; Carry
M_V EQU 1       ; Overflow
M_Z EQU 2       ; Zero
M_N EQU 3       ; Negative
M_U EQU 4       ; Unnormalized
M_E EQU 5       ; Extension
M_L EQU 6       ; Limit
M_S EQU 7       ; Scaling Bit
M_I0 EQU 8      ; Interupt Mask Bit 0
M_I1 EQU 9      ; Interupt Mask Bit 1
M_S0 EQU 10     ; Scaling Mode Bit 0
M_S1 EQU 11     ; Scaling Mode Bit 1
M_SC EQU 13     ; Sixteen_Bit Compatibility
M_DM EQU 14     ; Double Precision Multiply
M_LF EQU 15     ; DO-Loop Flag
M_FV EQU 16     ; DO-Forever Flag
M_SA EQU 17     ; Sixteen-Bit Arithmetic
M_CE EQU 19     ; Instruction Cache Enable
M_SM EQU 20     ; Arithmetic Saturation
M_RM EQU 21     ; Rounding Mode
M_CP0 EQU 22    ; bit 0 of priority bits in SR
M_CP1 EQU 23    ; bit 1 of priority bits in SR

;       control and status bits in OMR
M_CDP EQU $300 ; mask for CORE-DMA priority bits in OMR
M_MA    equ0    ; Operating Mode A
M_MB   equ1     ; Operating Mode B
M_MC    equ2    ; Operating Mode C
M_MD    equ3    ; Operating Mode D
M_EBD EQU 4     ; External Bus Disable bit in OMR
M_SD EQU 6      ; Stop Delay
M_MS EQU 7      ; Memory Switch bit in OMR
M_CDP0 EQU 8    ; bit 0 of priority bits in OMR
M_CDP1 EQU 9    ; bit 1 of priority bits in OMR
M_BEN   EQU 10 ; Burst Enable
M_TAS  EQU 11  ; TA Synchronize Select
M_BRT  EQU 12  ; Bus Release Timing
M_ATE EQU 15    ; Address Tracing Enable bit in OMR.
M_XYS EQU 16    ; Stack Extension space select bit in OMR.
M_EUN EQU 17    ; Extensed stack UNderflow flag in OMR.
M_EOV EQU 18    ; Extended stack OVerflow flag in OMR.
M_WRP EQU 19    ; Extended WRaP flag in OMR.
M_SEN EQU 20    ; Stack Extension Enable bit in OMR.
```

```
;*****************************************************************************
;
;     EQUATES for DSP56303 interrupts
;
;     Last update: June 11 1995
;
;*****************************************************************************

        page    132,55,0,0,0
        opt     mex

intequ  ident   1,0

        if      @DEF(I_VEC)
        ;leave user definition as is.
        else
I_VEC EQU $0
        endif

;------------------------------------------------------------------------------
; Non-Maskable interrupts
;------------------------------------------------------------------------------
I_RESET EQU I_VEC+$00  ; Hardware RESET
I_STACK EQU I_VEC+$02  ; Stack Error
I_ILL EQU I_VEC+$04    ; Illegal Instruction
I_DBG EQU I_VEC+$06    ; Debug Request
```

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