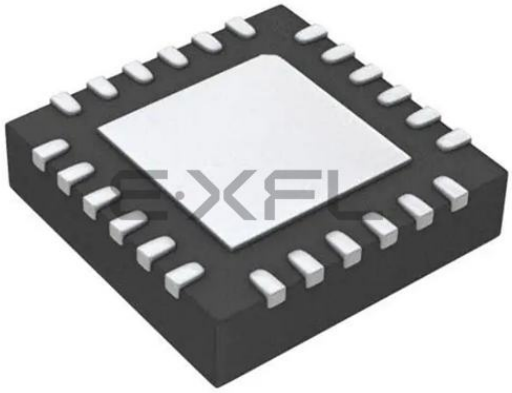


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	CIP-51 8051
Core Size	8-Bit
Speed	25MHz
Connectivity	EBI/EMI, I²C, SMBus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	16
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4.25K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 15x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	24-WFQFN Exposed Pad
Supplier Device Package	24-QFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm8sb20f32g-b-qfn24r

Ordering Part Number	Flash Memory (kB)	RAM (Bytes)	Digital Port I/Os (Total)	ADC Channels	Comparator Inputs	Pb-free (RoHS Compliant)	Temperature Range	Package
EFM8SB20F16G-B-QFN24	16	4352	16	15	8	Yes	-40 to +85 C	QFN24

10-Bit Analog-to-Digital Converter (ADC0)

The ADC is a successive-approximation-register (SAR) ADC with 10- and 8-bit modes, integrated track-and hold and a programmable window detector. The ADC is fully configurable under software control via several registers. The ADC may be configured to measure different signals using the analog multiplexer. The voltage reference for the ADC is selectable between internal and external reference sources.

- Up to 22 external inputs.
- Single-ended 10-bit mode.
- Supports an output update rate of 300 ksps samples per second.
- Operation in low power modes at lower conversion speeds.
- Asynchronous hardware conversion trigger, selectable between software, external I/O and internal timer sources.
- Output data window comparator allows automatic range checking.
- Support for burst mode, which produces one set of accumulated data per conversion-start trigger with programmable power-on settling and tracking time.
- Conversion complete and window compare interrupts supported.
- Flexible output data formatting.
- Includes an internal 1.65 V fast-settling reference and support for external reference.
- Integrated temperature sensor.

Low Current Comparators (CMP0, CMP1)

Analog comparators are used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. External input connections to device I/O pins and internal connections are available through separate multiplexers on the positive and negative inputs. Hysteresis, response time, and current consumption may be programmed to suit the specific needs of the application.

The comparator module includes the following features:

- Up to 12 external positive inputs.
- Up to 11 external negative inputs.
- Additional input options:
  - Capacitive Sense Comparator output.
  - VDD.
  - VDD divided by 2.
  - Internal connection to LDO output.
  - Direct connection to GND.
- Synchronous and asynchronous outputs can be routed to pins via crossbar.
- Programmable hysteresis between 0 and +/-20 mV.
- Programmable response time.
- Interrupts generated on rising, falling, or both edges.

3.8 Reset Sources

Reset circuitry allows the controller to be easily placed in a predefined default condition. On entry to this reset state, the following occur:

- The core halts program execution.
- Module registers are initialized to their defined reset values unless the bits reset only with a power-on reset.
- External port pins are forced to a known state.
- Interrupts and timers are disabled.

All registers are reset to the predefined values noted in the register descriptions unless the bits only reset with a power-on reset. The contents of RAM are unaffected during a reset; any previously stored data is preserved as long as power is not lost. The Port I/O latches are reset to 1 in open-drain mode. Weak pullups are enabled during and after the reset. For Supply Monitor and power-on resets, the RSTb pin is driven low until the device exits the reset state. On exit from the reset state, the program counter (PC) is reset, and the system clock defaults to an internal oscillator. The Watchdog Timer is enabled, and program execution begins at location 0x0000.

Reset sources on the device include the following:

- Power-on reset
- External reset pin
- Comparator reset
- Software-triggered reset
- Supply monitor reset (monitors VDD supply)
- Watchdog timer reset
- Missing clock detector reset
- Flash error reset
- RTC0 alarm or oscillator failure

3.9 Debugging

The EFM8SB2 devices include an on-chip Silicon Labs 2-Wire (C2) debug interface to allow flash programming and in-system debugging with the production part installed in the end application. The C2 interface uses a clock signal (C2CK) and a bi-directional C2 data signal (C2D) to transfer information between the device and a host system. See the C2 Interface Specification for details on the C2 protocol.

3.10 Bootloader

All devices come pre-programmed with a UART0 bootloader. This bootloader resides in the code security page, which is the last page of code flash; it can be erased if it is not needed.

The byte before the Lock Byte is the Bootloader Signature Byte. Setting this byte to a value of 0xA5 indicates the presence of the bootloader in the system. Any other value in this location indicates that the bootloader is not present in flash.

When a bootloader is present, the device will jump to the bootloader vector after any reset, allowing the bootloader to run. The bootloader then determines if the device should stay in bootload mode or jump to the reset vector located at 0x0000. When the bootloader is not present, the device will jump to the reset vector of 0x0000 after any reset.

More information about the bootloader protocol and usage can be found in *AN945: EFM8 Factory Bootloader User Guide*. Application notes can be found on the Silicon Labs website (www.silabs.com/8bit-appnotes) or within Simplicity Studio by using the [**Application Notes**] tile.

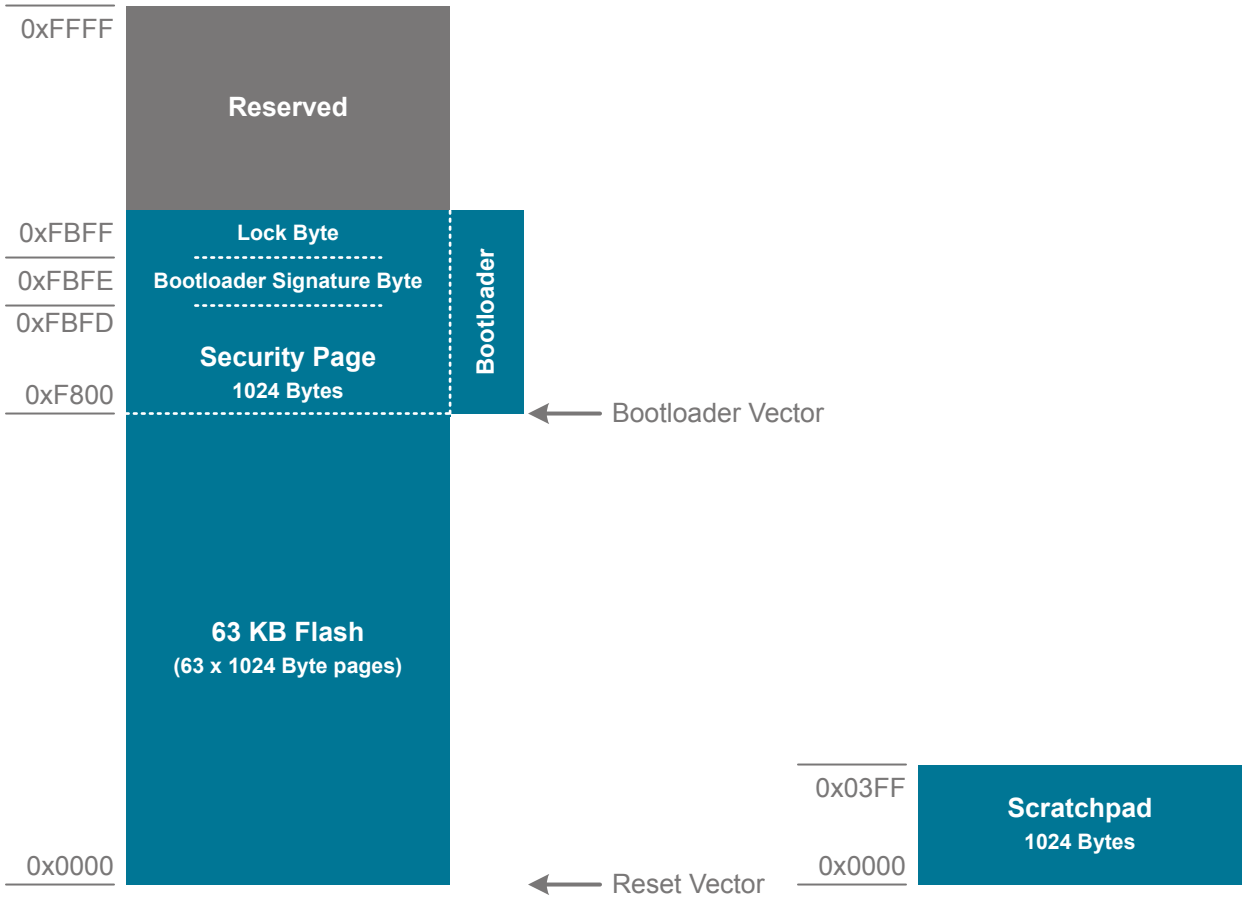


Figure 3.2. Flash Memory Map with Bootloader — 64 KB Devices

4. Electrical Specifications

4.1 Electrical Characteristics

All electrical parameters in all tables are specified under the conditions listed in Table 4.1 Recommended Operating Conditions on page 12, unless stated otherwise.

4.1.1 Recommended Operating Conditions

Table 4.1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating Supply Voltage on VDD	V_{DD}		1.8	2.4	3.6	V
Minimum RAM Data Retention Voltage on VDD[1]	V_{RAM}	Not in Sleep Mode	—	1.4	—	V
		Sleep Mode	—	0.3	0.5	V
System Clock Frequency	f_{SYSCLK}		0	—	25	MHz
Operating Ambient Temperature	T_A		–40	—	85	°C

Note:
1. All voltages with respect to GND.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Comparator 0 (CMP0) Supply Current	I_{CMP}	CPMD = 11	—	0.4	—	µA
		CPMD = 10	—	2.6	—	µA
		CPMD = 01	—	8.8	—	µA
		CPMD = 00	—	23	—	µA
Internal Fast-settling 1.65V ADC0 Reference, Always-on[8]	I_{VREFFS}		—	200	—	µA
On-chip Precision Reference	I_{VREFP}		—	15	—	µA
Temp sensor Supply Current	I_{TSENSE}		—	35	—	µA
Programmable Current Reference (IREF0) Supply Current[9]	I_{IREF}	Current Source, Either Power Mode, Any Output Code	—	10	—	µA
		Low Power Mode, Current Sink IREF0DAT = 000001	—	1	—	µA
		Low Power Mode, Current Sink IREF0DAT = 111111	—	11	—	µA
		High Current Mode, Current Sink IREF0DAT = 000001	—	12	—	µA
		High Current Mode, Current Sink IREF0DAT = 111111	—	81	—	µA

Note:

1. Based on device characterization data; Not production tested.
2. SYSCLK must be at least 32 kHz to enable debugging.
3. Digital Supply Current depends upon the particular code being executed. The values in this table are obtained with the CPU executing an “sjmp $” loop, which is the compiled form of a while(1) loop in C. One iteration requires 3 CPU clock cycles, and the flash memory is read on each cycle. The supply current will vary slightly based on the physical location of the sjmp instruction and the number of flash address lines that toggle as a result. In the worst case, current can increase by up to 30% if the sjmp loop straddles a 128-byte flash address boundary (e.g., 0x007F to 0x0080). Real-world code with larger loops and longer linear sequences will have few transitions across the 128-byte address boundaries.
4. Includes supply current from regulator and oscillator source (24.5 MHz high-frequency oscillator, 20 MHz low-power oscillator, or 32.768 kHz RTC oscillator).
5. IDD can be estimated for frequencies < 10 MHz by simply multiplying the frequency of interest by the frequency sensitivity number for that range, then adding an offset of 90 µA. When using these numbers to estimate I_{DD} for > 10 MHz, the estimate should be the current at 25 MHz minus the difference in current indicated by the frequency sensitivity number. For example: V_{DD} = 3.0 V; F = 20 MHz, I_{DD} = 4.1 mA – (25 MHz – 20 MHz) x 0.120 mA/MHz = 3.5 mA assuming the same oscillator setting.
6. Idle IDD can be estimated by taking the current at 25 MHz minus the difference in current indicated by the frequency sensitivity number. For example: V_{DD} = 3.0 V; F = 5 MHz, Idle I_{DD} = 2.5 mA – (25 MHz – 5 MHz) x 0.095 mA/MHz = 0.6 mA.
7. ADC0 always-on power excludes internal reference supply current.
8. The internal reference is enabled as-needed when operating the ADC in burst mode to save power.
9. IREF0 supply current only. Does not include current sourced or sunk from IREF0 output pin.

4.1.14 Port I/O

Table 4.14. Port I/O

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output High Voltage (High Drive)[1]	V_{OH}	I_{OH} = –3 mA	V_{DD} – 0.7	—	—	V
Output Low Voltage (High Drive)[1]	V_{OL}	I_{OL} = 8.5 mA	—	—	0.6	V
Output High Voltage (Low Drive)[1]	V_{OH}	I_{OH} = –1 mA	V_{DD} – 0.7	—	—	V
Output Low Voltage (Low Drive)[1]	V_{OL}	I_{OL} = 1.4 mA	—	—	0.6	V
Input High Voltage	V_{IH}	V_{DD} = 2.0 to 3.6 V	V_{DD} – 0.6	—	—	V
		V_{DD} = 1.8 to 2.0 V	0.7 x V_{DD}	—	—	V
Input Low Voltage	V_{IL}	V_{DD} = 2.0 to 3.6 V	—	—	0.6	V
		V_{DD} = 1.8 to 2.0 V	—	—	0.3 x V_{DD}	V
Weak Pull-Up Current	I_{PU}	V_{DD} = 1.8 V V_{IN} = 0 V	—	–4	—	µA
		V_{DD} = 3.6 V V_{IN} = 0 V	–35	–20	—	µA
Input Leakage	I_{LK}	Weak pullup disabled or pin in analog mode	–1	—	1	µA

Note:
1. See Figure 4.2 Typical V_{OH} Curves on page 24 and Figure 4.3 Typical V_{OL} Curves on page 25 for more information.

4.2 Thermal Conditions

Table 4.15. Thermal Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Thermal Resistance[1]	θ_{JA}	QFN-24 Packages	—	35	—	°C/W
		QFN-32 Packages	—	28	—	°C/W
		QFP-32 Packages	—	80	—	°C/W

Note:
1. Thermal resistance assumes a multi-layer PCB with any exposed pad soldered to a PCB pad.

4.3 Absolute Maximum Ratings

Stresses above those listed in Table 4.16 Absolute Maximum Ratings on page 23 may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. For more information on the available quality and reliability data, see the Quality and Reliability Monitor Report at http://www.silabs.com/support/quality/pages/default.aspx.

Table 4.16. Absolute Maximum Ratings

Parameter	Symbol	Test Condition	Min	Max	Unit
Ambient Temperature Under Bias	T_{BIAS}		–55	125	°C
Storage Temperature	T_{STG}		–65	150	°C
Voltage on V_{DD}	V_{DD}		GND–0.3	4.0	V
Voltage on I/O pins or RSTb	V_{IN}	V_{DD} > 2.2 V	GND–0.3	5.8	V
		V_{DD} <= 2.2 V	GND–0.3	V_{DD} + 3.6	V
Total Current Sunk into Supply Pin	I_{VDD}		—	400	mA
Total Current Sourced out of Ground Pin	I_{GND}		400	—	mA
Current Sourced or Sunk by Any I/O Pin or RSTb	I_{IO}		-100	100	mA
Maximum Total Current through all Port Pins	I_{IOTOT}		—	200	mA
Operating Junction Temperature	T_J		–40	105	°C
Exposure to maximum rating conditions for extended periods may affect device reliability.					

5. Typical Connection Diagrams

5.1 Power

Figure 5.1 Power Connection Diagram on page 26 shows a typical connection diagram for the power pins of the EFM8SB2 devices.

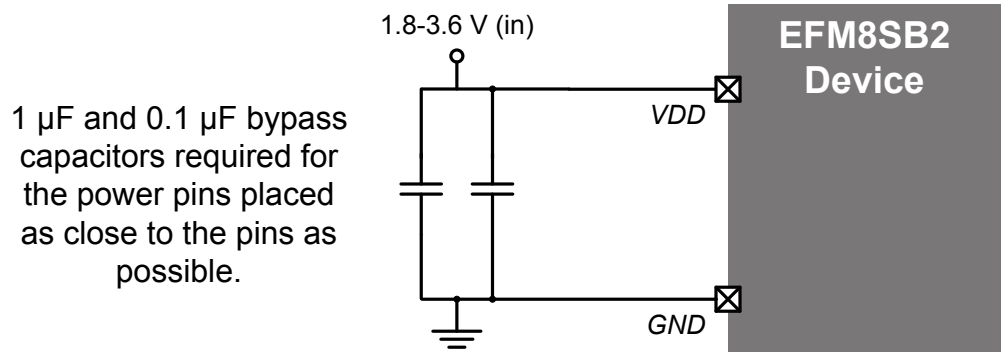


Figure 5.1. Power Connection Diagram

5.2 Debug

The diagram below shows a typical connection diagram for the debug connections pins. The pin sharing resistors are only required if the functionality on the C2D (a GPIO pin) and the C2CK (RSTb) is routed to external circuitry. For example, if the RSTb pin is connected to an external switch with debouncing filter or if the GPIO sharing with the C2D pin is connected to an external circuit, the pin sharing resistors and connections to the debug adapter must be placed on the hardware. Otherwise, these components and connections can be omitted.

For more information on debug connections, see the example schematics and information available in AN127: "Pin Sharing Techniques for the C2 Interface." Application notes can be found on the Silicon Labs website (http://www.silabs.com/8bit-appnotes) or in Simplicity Studio.

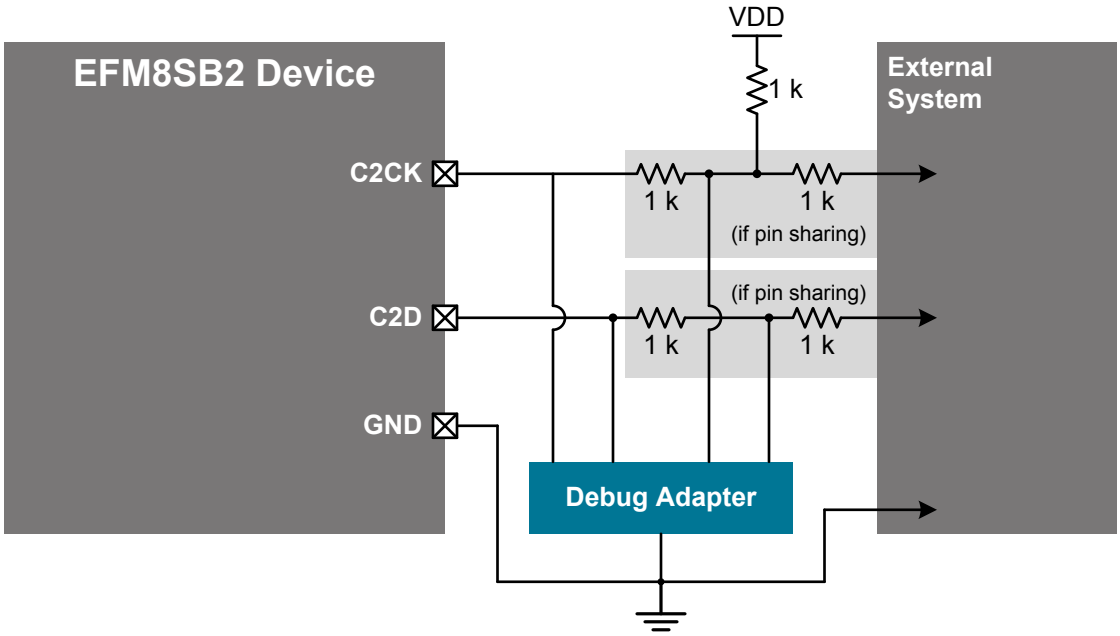


Figure 5.2. Debug Connection Diagram

6. Pin Definitions

6.1 EFM8SB2x-QFN32 Pin Definitions

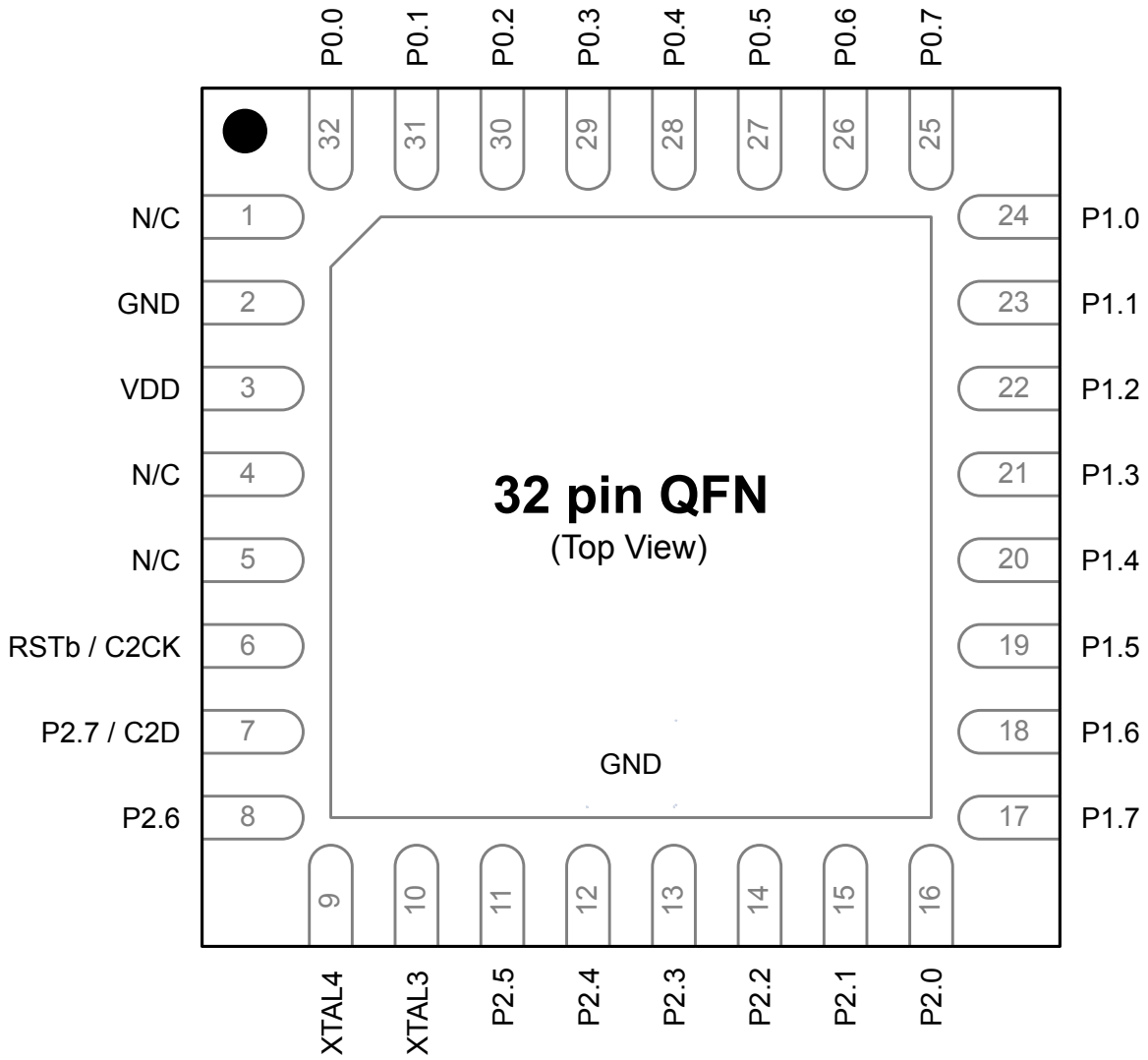


Figure 6.1. EFM8SB2x-QFN32 Pinout

Table 6.1. Pin Definitions for EFM8SB2x-QFN32

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
1	N/C	No Connection			
2	GND	Ground			
3	VDD	Supply Power Input			
4	N/C	No Connection			

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
19	P1.5	Multifunction I/O	Yes	P1MAT.5 EMIF_AD5	ADC0.13 CMP0N.6 CMP1N.6
20	P1.4	Multifunction I/O	Yes	P1MAT.4 EMIF_AD4	ADC0.12 CMP0P.6 CMP1P.6
21	P1.3	Multifunction I/O	Yes	P1MAT.3 SPI1_NSS EMIF_AD3	ADC0.11 CMP0N.5 CMP1N.5
22	P1.2	Multifunction I/O	Yes	P1MAT.2 SPI1_MOSI EMIF_AD2	ADC0.10 CMP0P.5 CMP1P.5
23	P1.1	Multifunction I/O	Yes	P1MAT.1 SPI1_MISO EMIF_AD1	ADC0.9 CMP0N.4 CMP1N.4
24	P1.0	Multifunction I/O	Yes	P1MAT.0 SPI1_SCK EMIF_AD0	ADC0.8 CMP0P.4 CMP1P.4
25	P0.7	Multifunction I/O	Yes	P0MAT.7 INT0.7 INT1.7	ADC0.7 IREF0 CMP0N.3 CMP1N.3
26	P0.6	Multifunction I/O	Yes	P0MAT.6 CNVSTR INT0.6 INT1.6	ADC0.6 CMP0P.3 CMP1P.3
27	P0.5	Multifunction I/O	Yes	P0MAT.5 INT0.5 INT1.5	ADC0.5 CMP0N.2 CMP1N.2
28	P0.4	Multifunction I/O	Yes	P0MAT.4 INT0.4 INT1.4	ADC0.4 CMP0P.2 CMP1P.2
29	P0.3	Multifunction I/O	Yes	P0MAT.3 EXTCLK INT0.3 INT1.3	ADC0.3 XTAL2 CMP0N.1 CMP1N.1

6.2 EFM8SB2x-QFN24 Pin Definitions

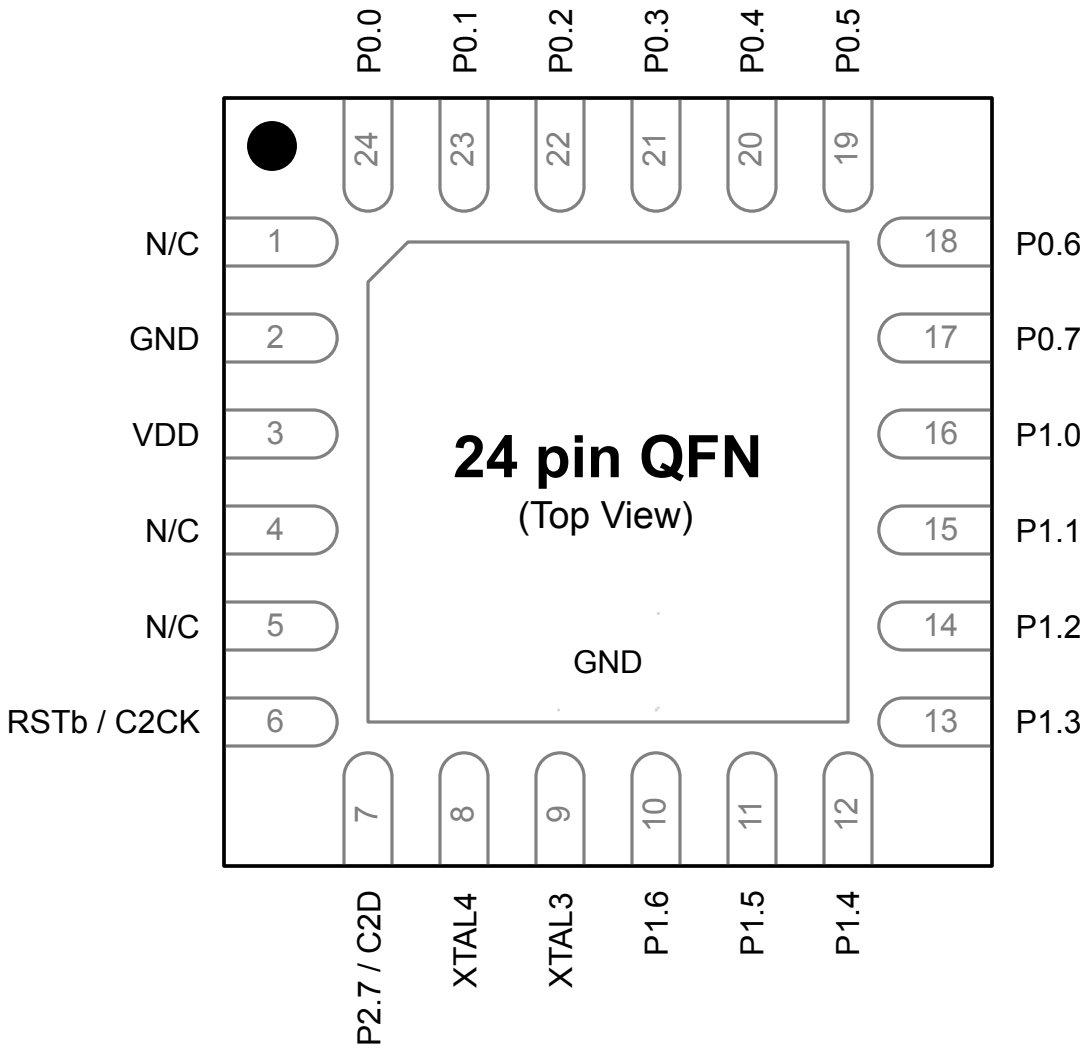


Figure 6.2. EFM8SB2x-QFN24 Pinout

Table 6.2. Pin Definitions for EFM8SB2x-QFN24

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
1	N/C	No Connection			
2	GND	Ground			
3	VDD	Supply Power Input			
4	N/C	No Connection			
5	N/C	No Connection			

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
6	RSTb / C2CK	Active-low Reset / C2 Debug Clock			
7	P2.7 / C2D	Multifunction I/O / C2 Debug Data			
8	XTAL4	RTC Crystal			XTAL4
9	XTAL3	RTC Crystal			XTAL3
10	P1.6	Multifunction I/O	Yes		ADC0.14 CMP0P.7 CMP1P.7
11	P1.5	Multifunction I/O	Yes	P1MAT.5	ADC0.13 CMP0N.6 CMP1N.6
12	P1.4	Multifunction I/O	Yes	P1MAT.4	ADC0.12 CMP0P.6 CMP1P.6
13	P1.3	Multifunction I/O	Yes	P1MAT.3 SPI1_NSS	ADC0.11 CMP0N.5 CMP1N.5
14	P1.2	Multifunction I/O	Yes	P1MAT.2 SPI1_MOSI	ADC0.10 CMP0P.5 CMP1P.5
15	P1.1	Multifunction I/O	Yes	P1MAT.1 SPI1_MISO	ADC0.9 CMP0N.4 CMP1N.4
16	P1.0	Multifunction I/O	Yes	P1MAT.0 SPI1_SCK	ADC0.8 CMP0P.4 CMP1P.4
17	P0.7	Multifunction I/O	Yes	P0MAT.7 INT0.7 INT1.7	ADC0.7 IREF0 CMP0N.3 CMP1N.3
18	P0.6	Multifunction I/O	Yes	P0MAT.6 CNVSTR INT0.6 INT1.6	ADC0.6 CMP0P.3 CMP1P.3

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
19	P0.5	Multifunction I/O	Yes	P0MAT.5 INT0.5 INT1.5	ADC0.5 CMP0N.2 CMP1N.2
20	P0.4	Multifunction I/O	Yes	P0MAT.4 INT0.4 INT1.4	ADC0.4 CMP0P.2 CMP1P.2
21	P0.3	Multifunction I/O	Yes	P0MAT.3 EXTCLK INT0.3 INT1.3	ADC0.3 XTAL2 CMP0N.1 CMP1N.1
22	P0.2	Multifunction I/O	Yes	P0MAT.2 INT0.2 INT1.2	ADC0.2 CMP0P.1 CMP1P.1 XTAL1
23	P0.1	Multifunction I/O	Yes	P0MAT.1 INT0.1 INT1.1	ADC0.1 AGND CMP0N.0 CMP1N.0
24	P0.0	Multifunction I/O	Yes	P0MAT.0 INT0.0 INT1.0	ADC0.0 CMP0P.0 CMP1P.0 VREF
Center	GND	Ground			

Dimension	Min	Typ	Max
bbb	—	—	0.10
ddd	—	—	0.05
eee	—	—	0.08

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC Solid State Outline MO-220, variation VHHD except for custom features D2, E2, and L which are toleranced per supplier designation.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

Dimension	Min	Typ	Max
bbb	—	—	0.10
ddd	—	—	0.05
eee	—	—	0.08
Z	—	0.24	—
Y	—	0.18	—

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC Solid State Outline MO-220, variation WGGD except for custom features D2, E2, Z, Y, and L which are toleranced per supplier designation.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

8.2 QFN24 PCB Land Pattern

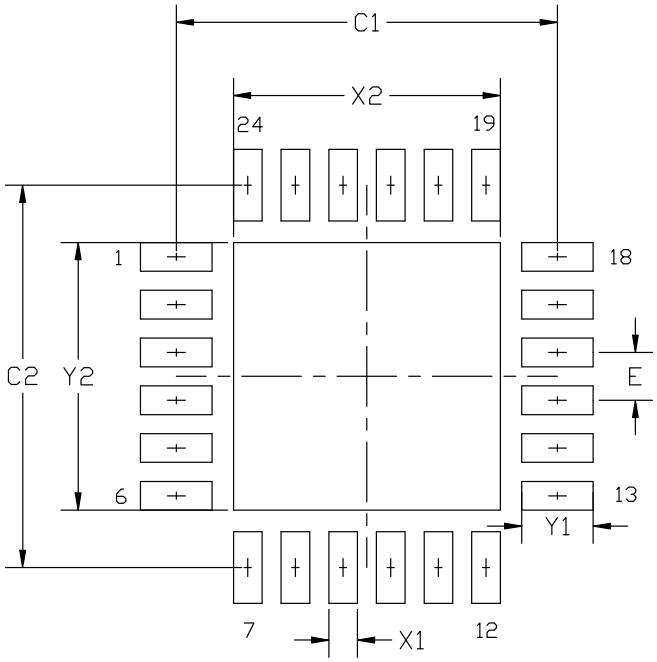


Figure 8.2. QFN24 PCB Land Pattern Drawing

Table 8.2. QFN24 PCB Land Pattern Dimensions

Dimension	Min	Max
C1	3.90	4.00
C2	3.90	4.00
E	0.50 BSC	
X1	0.20	0.30
X2	2.70	2.80
Y1	0.65	0.75
Y2	2.70	2.80

10. Revision History

10.1 Revision 1.2

Updated ordering part numbers to revision B.

Added Reset Delay from POR specification.

Added I/O 5 V tolerance to 1. Feature List.

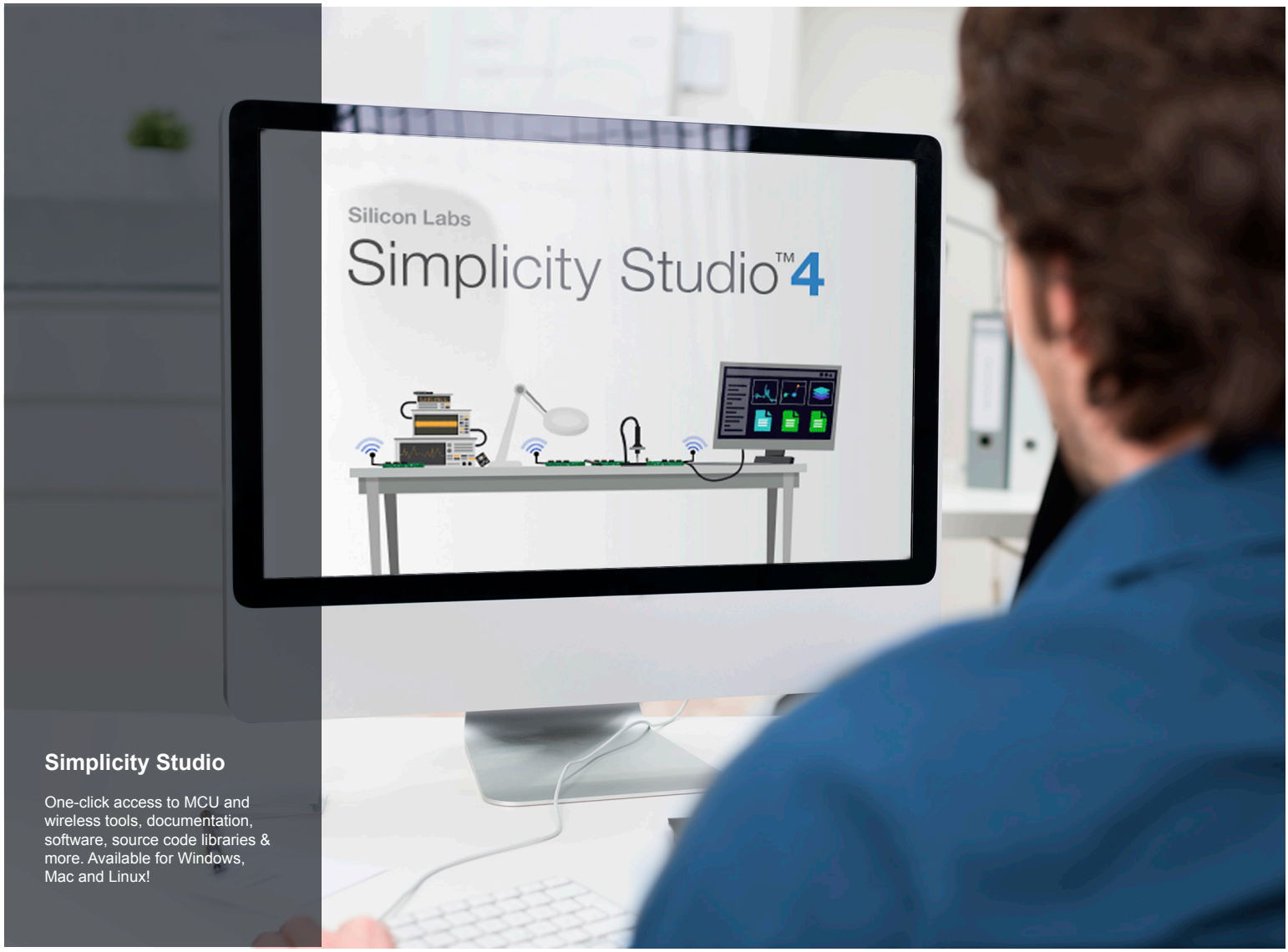
Added information on the bootloader to 3.10 Bootloader.

Added a Debug Typical Connection Diagram to 5. Typical Connection Diagrams.

Added reference to the Reference Manual in 3.1 Introduction.

10.2 Revision 1.1

Initial release.



Simplicity Studio

One-click access to MCU and wireless tools, documentation, software, source code libraries & more. Available for Windows, Mac and Linux!

IoT Portfolio
www.silabs.com/IoT

SW/HW
www.silabs.com/simplicity

Quality
www.silabs.com/quality

Support and Community
community.silabs.com

SILICON LABS®

Silicon Laboratories Inc.
400 West Cesar Chavez
Austin, TX 78701
USA

http://www.silabs.com