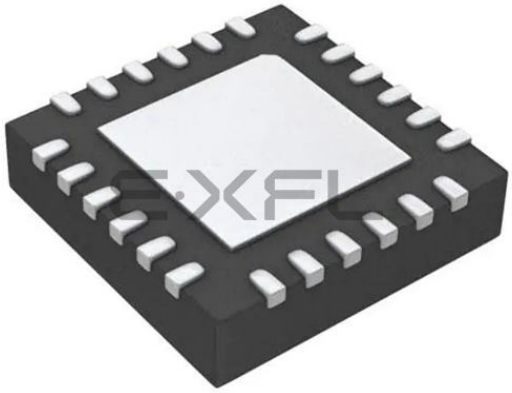

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	CIP-51 8051
Core Size	8-Bit
Speed	25MHz
Connectivity	EBI/EMI, I²C, SMBus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	16
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4.25K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 15x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	24-WFQFN Exposed Pad
Supplier Device Package	24-QFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm8sb20f64g-b-qfn24r

2. Ordering Information

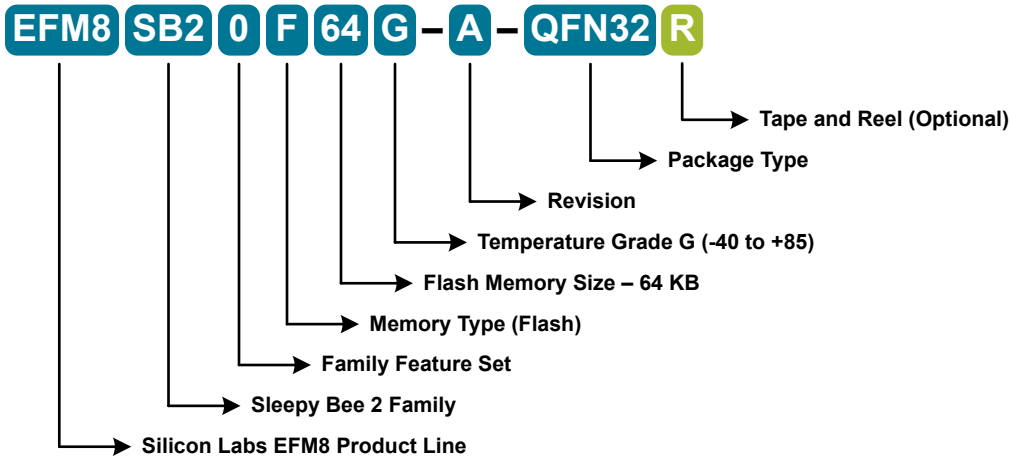

Figure 2.1. EFM8SB2 Part Numbering

All EFM8SB2 family members have the following features:

- CIP-51 Core running up to 25 MHz
- Three Internal Oscillators (24.5 MHz, 20 MHz, and 16 kHz)
- SMBus / I2C
- 2 x SPI
- UART
- 6-Channel Programmable Counter Array (PWM, Clock Generation, Capture/Compare)
- 4 16-bit Timers
- 2 Analog Comparators
- 6-bit programmable current reference
- 10-bit Analog-to-Digital Converter with integrated multiplexer, voltage reference, and temperature sensor
- Low-current 32 kHz oscillator and Real Time Clock
- 16-bit CRC Unit
- Pre-loaded UART bootloader

In addition to these features, each part number in the EFM8SB2 family has a set of features that vary across the product line. The product selection guide shows the features available on each family member.

Table 2.1. Product Selection Guide

Ordering Part Number	Flash Memory (kB)	RAM (Bytes)	Digital Port I/Os (Total)	ADC Channels	Comparator Inputs	Pb-free (RoHS Compliant)	Temperature Range	Package
EFM8SB20F64G-B-QFN32	64	4352	24	23	12	Yes	-40 to +85 C	QFN32
EFM8SB20F64G-B-QFP32	64	4352	24	23	12	Yes	-40 to +85 C	QFP32
EFM8SB20F64G-B-QFN24	64	4352	16	15	8	Yes	-40 to +85 C	QFN24
EFM8SB20F32G-B-QFN32	32	4352	24	23	12	Yes	-40 to +85 C	QFN32
EFM8SB20F32G-B-QFP32	32	4352	24	23	12	Yes	-40 to +85 C	QFP32
EFM8SB20F32G-B-QFN24	32	4352	16	15	8	Yes	-40 to +85 C	QFN24

3.2 Power

All internal circuitry draws power from the VDD supply pin. External I/O pins are powered from the VIO supply voltage (or VDD on devices without a separate VIO connection), while most of the internal circuitry is supplied by an on-chip LDO regulator. Control over the device power can be achieved by enabling/disabling individual peripherals as needed. Each analog peripheral can be disabled when not in use and placed in low power mode. Digital peripherals, such as timers and serial buses, have their clocks gated off and draw little power when they are not in use.

Table 3.1. Power Modes

Power Mode	Details	Mode Entry	Wake-Up Sources
Normal	Core and all peripherals clocked and fully operational	—	—
Idle	• Core halted • All peripherals clocked and fully operational • Code resumes execution on wake event	Set IDLE bit in PCON0	Any interrupt
Suspend	• Core and digital peripherals halted • Internal oscillators disabled • Code resumes execution on wake event	1. Switch SYSCLK to HFOSC0 or LPOSC0 2. Set SUSPEND bit in PMU0CF	• RTC0 Alarm Event • RTC0 Fail Event • Port Match Event • Comparator 0 Rising Edge
Stop	• All internal power nets shut down • Pins retain state • Exit on any reset source	Set STOP bit in PCON0	Any reset source
Sleep	• Most internal power nets shut down • Select circuits remain powered • Pins retain state • All RAM and SFRs retain state • Code resumes execution on wake event	1. Disable unused analog peripherals 2. Set SLEEP bit in PMU0CF	• RTC0 Alarm Event • RTC0 Fail Event • Port Match Event • Comparator 0 Rising Edge

3.3 I/O

Digital and analog resources are externally available on the device's multi-purpose I/O pins. Port pins P0.0-P2.6 can be defined as general-purpose I/O (GPIO), assigned to one of the internal digital resources through the crossbar or dedicated channels, or assigned to an analog function. Port pin P2.7 can be used as GPIO. Additionally, the C2 Interface Data signal (C2D) is shared with P2.7.

- Up to 24 multi-functions I/O pins, supporting digital and analog functions.
- Flexible priority crossbar decoder for digital peripheral assignment.
- Two drive strength settings for each pin.
- Two direct-pin interrupt sources with dedicated interrupt vectors (INT0 and INT1).
- Up to 16 direct-pin interrupt sources with shared interrupt vector (Port Match).

3.4 Clocking

The CPU core and peripheral subsystem may be clocked by both internal and external oscillator resources. By default, the system clock comes up running from the 20 MHz low power oscillator divided by 8.

- Provides clock to core and peripherals.
- 20 MHz low power oscillator (LPOSC0), accurate to +/- 10% over supply and temperature corners.
- 24.5 MHz internal oscillator (HFOSC0), accurate to +/- 2% over supply and temperature corners.
- External RTC 32 kHz crystal.
- External RC, C, CMOS, and high-frequency crystal clock options (EXTCLK).
- Clock divider with eight settings for flexible clock scaling: Divide the selected clock source by 1, 2, 4, 8, 16, 32, 64, or 128.

3.10 Bootloader

All devices come pre-programmed with a UART0 bootloader. This bootloader resides in the code security page, which is the last page of code flash; it can be erased if it is not needed.

The byte before the Lock Byte is the Bootloader Signature Byte. Setting this byte to a value of 0xA5 indicates the presence of the bootloader in the system. Any other value in this location indicates that the bootloader is not present in flash.

When a bootloader is present, the device will jump to the bootloader vector after any reset, allowing the bootloader to run. The bootloader then determines if the device should stay in bootload mode or jump to the reset vector located at 0x0000. When the bootloader is not present, the device will jump to the reset vector of 0x0000 after any reset.

More information about the bootloader protocol and usage can be found in *AN945: EFM8 Factory Bootloader User Guide*. Application notes can be found on the Silicon Labs website (www.silabs.com/8bit-appnotes) or within Simplicity Studio by using the [**Application Notes**] tile.

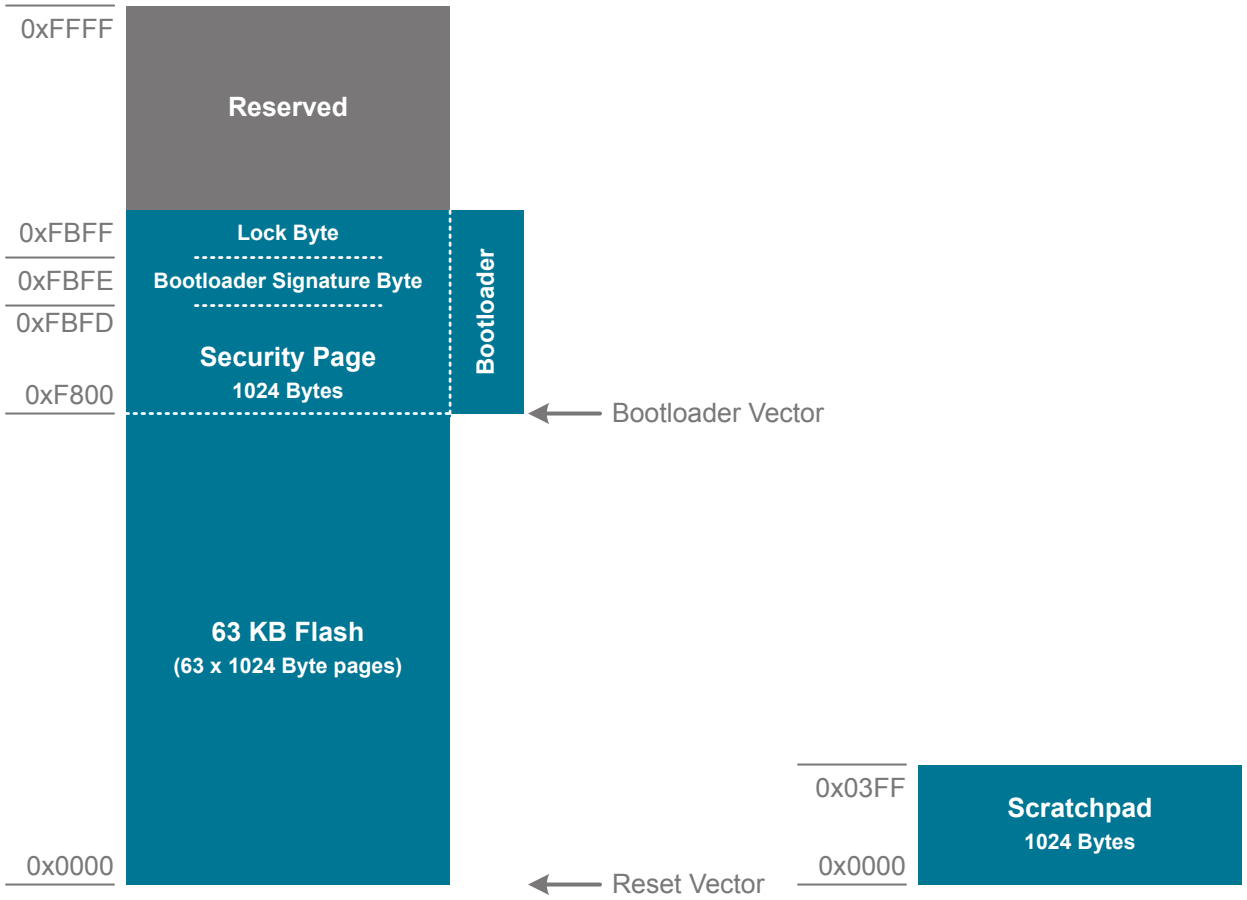

Figure 3.2. Flash Memory Map with Bootloader — 64 KB Devices

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Comparator 0 (CMP0) Supply Current	I_{CMP}	CPMD = 11	—	0.4	—	µA
		CPMD = 10	—	2.6	—	µA
		CPMD = 01	—	8.8	—	µA
		CPMD = 00	—	23	—	µA
Internal Fast-settling 1.65V ADC0 Reference, Always-on[8]	I_{VREFFS}		—	200	—	µA
On-chip Precision Reference	I_{VREFP}		—	15	—	µA
Temp sensor Supply Current	I_{TSENSE}		—	35	—	µA
Programmable Current Reference (IREF0) Supply Current[9]	I_{IREF}	Current Source, Either Power Mode, Any Output Code	—	10	—	µA
		Low Power Mode, Current Sink IREF0DAT = 000001	—	1	—	µA
		Low Power Mode, Current Sink IREF0DAT = 111111	—	11	—	µA
		High Current Mode, Current Sink IREF0DAT = 000001	—	12	—	µA
		High Current Mode, Current Sink IREF0DAT = 111111	—	81	—	µA

Note:

1. Based on device characterization data; Not production tested.
2. SYSCLK must be at least 32 kHz to enable debugging.
3. Digital Supply Current depends upon the particular code being executed. The values in this table are obtained with the CPU executing an “sjmp $” loop, which is the compiled form of a while(1) loop in C. One iteration requires 3 CPU clock cycles, and the flash memory is read on each cycle. The supply current will vary slightly based on the physical location of the sjmp instruction and the number of flash address lines that toggle as a result. In the worst case, current can increase by up to 30% if the sjmp loop straddles a 128-byte flash address boundary (e.g., 0x007F to 0x0080). Real-world code with larger loops and longer linear sequences will have few transitions across the 128-byte address boundaries.
4. Includes supply current from regulator and oscillator source (24.5 MHz high-frequency oscillator, 20 MHz low-power oscillator, or 32.768 kHz RTC oscillator).
5. IDD can be estimated for frequencies < 10 MHz by simply multiplying the frequency of interest by the frequency sensitivity number for that range, then adding an offset of 90 µA. When using these numbers to estimate I_{DD} for > 10 MHz, the estimate should be the current at 25 MHz minus the difference in current indicated by the frequency sensitivity number. For example: V_{DD} = 3.0 V; F = 20 MHz, I_{DD} = 4.1 mA – (25 MHz – 20 MHz) x 0.120 mA/MHz = 3.5 mA assuming the same oscillator setting.
6. Idle IDD can be estimated by taking the current at 25 MHz minus the difference in current indicated by the frequency sensitivity number. For example: V_{DD} = 3.0 V; F = 5 MHz, Idle I_{DD} = 2.5 mA – (25 MHz – 5 MHz) x 0.095 mA/MHz = 0.6 mA.
7. ADC0 always-on power excludes internal reference supply current.
8. The internal reference is enabled as-needed when operating the ADC in burst mode to save power.
9. IREF0 supply current only. Does not include current sourced or sunk from IREF0 output pin.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Negative Hysteresis Mode 3 (CPMD = 11)	HYS_{CP-}	CPHYN = 00	—	-1.5	—	mV
		CPHYN = 01	—	–4	—	mV
		CPHYN = 10	—	–8	—	mV
		CPHYN = 11	—	–16	—	mV
Input Range (CP+ or CP–)	V_{IN}		-0.25	—	V_{DD}+0.25	V
Input Pin Capacitance	C_{CP}		—	12	—	pF
Common-Mode Rejection Ratio	$CMRR_{CP}$		—	70	—	dB
Power Supply Rejection Ratio	$PSRR_{CP}$		—	72	—	dB
Input Offset Voltage	V_{OFF}	T_A = 25 °C	-10	0	10	mV
Input Offset Tempco	TC_{OFF}		—	3.5	—	µV/°C

4.1.13 Programmable Current Reference (IREF0)

Table 4.13. Programmable Current Reference (IREF0)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Performance						
Resolution	N_{bits}			6		bits
Output Compliance Range	V_{IOUT}	Low Power Mode, Source	0	—	V_{DD} – 0.4	V
		High Current Mode, Source	0	—	V_{DD} – 0.8	V
		Low Power Mode, Sink	0.3	—	V_{DD}	V
		High Current Mode, Sink	0.8	—	V_{DD}	V
Integral Nonlinearity	INL		—	<±0.2	±1.0	LSB
Differential Nonlinearity	DNL		—	<±0.2	±1.0	LSB
Offset Error	E_{OFF}		—	<±0.1	±0.5	LSB
Full Scale Error	E_{FS}	Low Power Mode, Source	—	—	±5	%
		High Current Mode, Source	—	—	±6	%
		Low Power Mode, Sink	—	—	±8	%
		High Current Mode, Sink	—	—	±8	%
Absolute Current Error	E_{ABS}	Low Power Mode Sourcing 20 µA	—	<±1	±3	%
Dynamic Performance						
Output Settling Time to 1/2 LSB	t_{SETTLE}		—	300	—	ns
Startup Time	t_{PWR}		—	1	—	µs

Note:
1. The PCA block may be used to improve IREF0 resolution by PWMing the two LSBs.

4.1.14 Port I/O

Table 4.14. Port I/O

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output High Voltage (High Drive)[1]	V_{OH}	I_{OH} = –3 mA	V_{DD} – 0.7	—	—	V
Output Low Voltage (High Drive)[1]	V_{OL}	I_{OL} = 8.5 mA	—	—	0.6	V
Output High Voltage (Low Drive)[1]	V_{OH}	I_{OH} = –1 mA	V_{DD} – 0.7	—	—	V
Output Low Voltage (Low Drive)[1]	V_{OL}	I_{OL} = 1.4 mA	—	—	0.6	V
Input High Voltage	V_{IH}	V_{DD} = 2.0 to 3.6 V	V_{DD} – 0.6	—	—	V
		V_{DD} = 1.8 to 2.0 V	0.7 x V_{DD}	—	—	V
Input Low Voltage	V_{IL}	V_{DD} = 2.0 to 3.6 V	—	—	0.6	V
		V_{DD} = 1.8 to 2.0 V	—	—	0.3 x V_{DD}	V
Weak Pull-Up Current	I_{PU}	V_{DD} = 1.8 V V_{IN} = 0 V	—	–4	—	µA
		V_{DD} = 3.6 V V_{IN} = 0 V	–35	–20	—	µA
Input Leakage	I_{LK}	Weak pullup disabled or pin in analog mode	–1	—	1	µA

Note:
1. See Figure 4.2 Typical V_{OH} Curves on page 24 and Figure 4.3 Typical V_{OL} Curves on page 25 for more information.

4.2 Thermal Conditions

Table 4.15. Thermal Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Thermal Resistance[1]	θ_{JA}	QFN-24 Packages	—	35	—	°C/W
		QFN-32 Packages	—	28	—	°C/W
		QFP-32 Packages	—	80	—	°C/W

Note:
1. Thermal resistance assumes a multi-layer PCB with any exposed pad soldered to a PCB pad.

4.4 Typical Performance Curves

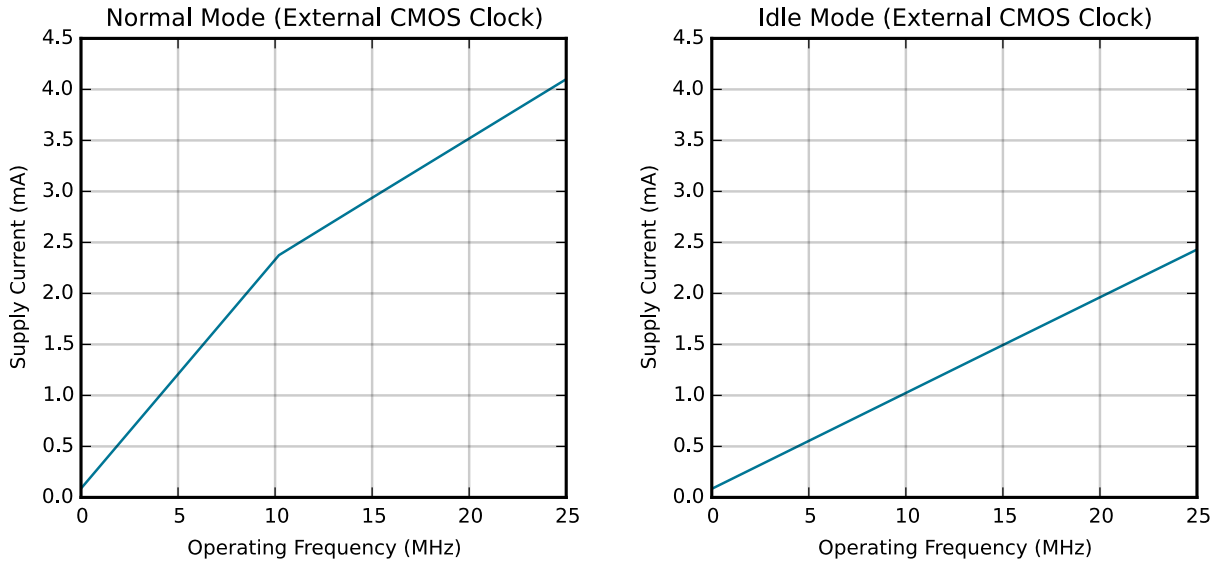

Figure 4.1. Typical Operating Supply Current (full supply voltage range)

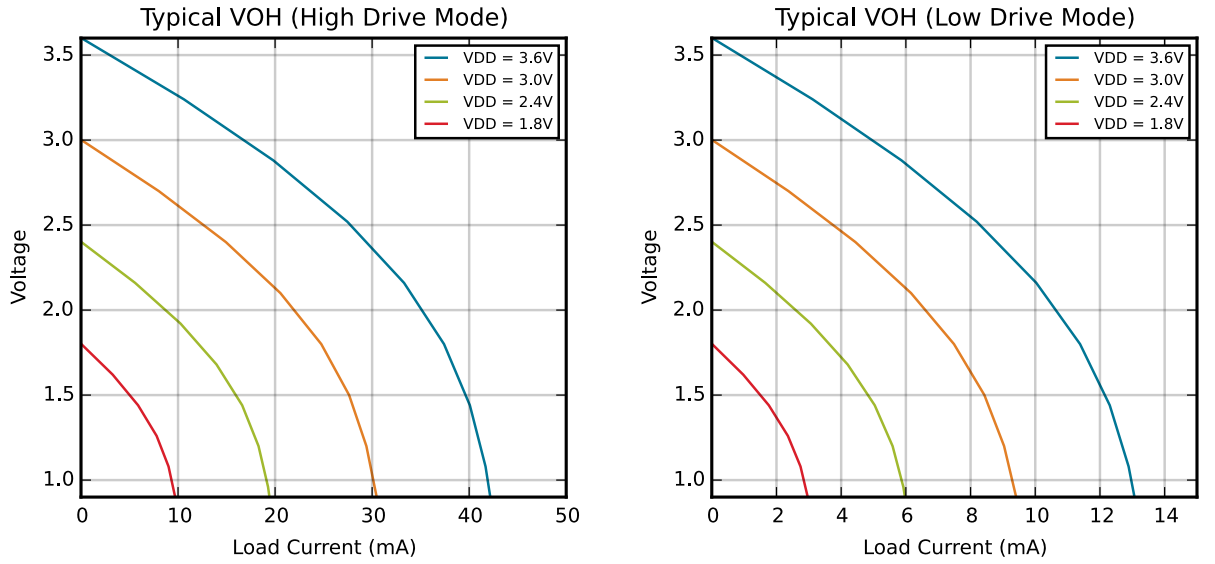

Figure 4.2. Typical V_{OH} Curves

5.3 Other Connections

Other components or connections may be required to meet the system-level requirements. Application note, "AN203: 8-bit MCU Printed Circuit Board Design Notes", contains detailed information on these connections. Application Notes can be accessed on the Silicon Labs website (www.silabs.com/8bit-appnotes).

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
6	RSTb / C2CK	Active-low Reset / C2 Debug Clock			
7	P2.7 / C2D	Multifunction I/O / C2 Debug Data			
8	XTAL4	RTC Crystal			XTAL4
9	XTAL3	RTC Crystal			XTAL3
10	P1.6	Multifunction I/O	Yes		ADC0.14 CMP0P.7 CMP1P.7
11	P1.5	Multifunction I/O	Yes	P1MAT.5	ADC0.13 CMP0N.6 CMP1N.6
12	P1.4	Multifunction I/O	Yes	P1MAT.4	ADC0.12 CMP0P.6 CMP1P.6
13	P1.3	Multifunction I/O	Yes	P1MAT.3 SPI1_NSS	ADC0.11 CMP0N.5 CMP1N.5
14	P1.2	Multifunction I/O	Yes	P1MAT.2 SPI1_MOSI	ADC0.10 CMP0P.5 CMP1P.5
15	P1.1	Multifunction I/O	Yes	P1MAT.1 SPI1_MISO	ADC0.9 CMP0N.4 CMP1N.4
16	P1.0	Multifunction I/O	Yes	P1MAT.0 SPI1_SCK	ADC0.8 CMP0P.4 CMP1P.4
17	P0.7	Multifunction I/O	Yes	P0MAT.7 INT0.7 INT1.7	ADC0.7 IREF0 CMP0N.3 CMP1N.3
18	P0.6	Multifunction I/O	Yes	P0MAT.6 CNVSTR INT0.6 INT1.6	ADC0.6 CMP0P.3 CMP1P.3

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
19	P0.5	Multifunction I/O	Yes	P0MAT.5 INT0.5 INT1.5	ADC0.5 CMP0N.2 CMP1N.2
20	P0.4	Multifunction I/O	Yes	P0MAT.4 INT0.4 INT1.4	ADC0.4 CMP0P.2 CMP1P.2
21	P0.3	Multifunction I/O	Yes	P0MAT.3 EXTCLK INT0.3 INT1.3	ADC0.3 XTAL2 CMP0N.1 CMP1N.1
22	P0.2	Multifunction I/O	Yes	P0MAT.2 INT0.2 INT1.2	ADC0.2 CMP0P.1 CMP1P.1 XTAL1
23	P0.1	Multifunction I/O	Yes	P0MAT.1 INT0.1 INT1.1	ADC0.1 AGND CMP0N.0 CMP1N.0
24	P0.0	Multifunction I/O	Yes	P0MAT.0 INT0.0 INT1.0	ADC0.0 CMP0P.0 CMP1P.0 VREF
Center	GND	Ground			

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
8	P2.6	Multifunction I/O	Yes	EMIF_WRb	ADC0.22 CMP0P.11 CMP1P.11
9	XTAL4	RTC Crystal			XTAL4
10	XTAL3	RTC Crystal			XTAL3
11	P2.5	Multifunction I/O	Yes	EMIF_RDb	ADC0.21 CMP0N.10 CMP1N.10
12	P2.4	Multifunction I/O	Yes	EMIF_ALE	ADC0.20 CMP0P.10 CMP1P.10
13	P2.3	Multifunction I/O	Yes	EMIF_A11	ADC0.19 CMP0N.9 CMP1N.9
14	P2.2	Multifunction I/O	Yes	EMIF_A10	ADC0.18 CMP0P.9 CMP1P.9
15	P2.1	Multifunction I/O	Yes	EMIF_A9	ADC0.17 CMP0N.8 CMP1N.8
16	P2.0	Multifunction I/O	Yes	EMIF_A8	ADC0.16 CMP0P.8 CMP1P.8
17	P1.7	Multifunction I/O	Yes	P1MAT.7 EMIF_AD7	ADC0.15 CMP0N.7 CMP1N.7
18	P1.6	Multifunction I/O	Yes	P1MAT.6 EMIF_AD6	ADC0.14 CMP0P.7 CMP1P.7
19	P1.5	Multifunction I/O	Yes	P1MAT.5 EMIF_AD5	ADC0.13 CMP0N.6 CMP1N.6
20	P1.4	Multifunction I/O	Yes	P1MAT.4 EMIF_AD4	ADC0.12 CMP0P.6 CMP1P.6

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
21	P1.3	Multifunction I/O	Yes	P1MAT.3 SPI1_NSS EMIF_AD3	ADC0.11 CMP0N.5 CMP1N.5
22	P1.2	Multifunction I/O	Yes	P1MAT.2 SPI1_MOSI EMIF_AD2	ADC0.10 CMP0P.5 CMP1P.5
23	P1.1	Multifunction I/O	Yes	P1MAT.1 SPI1_MISO EMIF_AD1	ADC0.9 CMP0N.4 CMP1N.4
24	P1.0	Multifunction I/O	Yes	P1MAT.0 SPI1_SCK EMIF_AD0	ADC0.8 CMP0P.4 CMP1P.4
25	P0.7	Multifunction I/O	Yes	P0MAT.7 INT0.7 INT1.7	ADC0.7 IREF0 CMP0N.3 CMP1N.3
26	P0.6	Multifunction I/O	Yes	P0MAT.6 CNVSTR INT0.6 INT1.6	ADC0.6 CMP0P.3 CMP1P.3
27	P0.5	Multifunction I/O	Yes	P0MAT.5 INT0.5 INT1.5	ADC0.5 CMP0N.2 CMP1N.2
28	P0.4	Multifunction I/O	Yes	P0MAT.4 INT0.4 INT1.4	ADC0.4 CMP0P.2 CMP1P.2
29	P0.3	Multifunction I/O	Yes	P0MAT.3 EXTCLK INT0.3 INT1.3	ADC0.3 XTAL2 CMP0N.1 CMP1N.1
30	P0.2	Multifunction I/O	Yes	P0MAT.2 INT0.2 INT1.2	ADC0.2 CMP0P.1 CMP1P.1 XTAL1

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
31	P0.1	Multifunction I/O	Yes	P0MAT.1 INT0.1 INT1.1	ADC0.1 AGND CMP0N.0 CMP1N.0
32	P0.0	Multifunction I/O	Yes	P0MAT.0 INT0.0 INT1.0	ADC0.0 CMP0P.0 CMP1P.0 VREF

Dimension	Min	Typ	Max
bbb	—	—	0.10
ddd	—	—	0.05
eee	—	—	0.08

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC Solid State Outline MO-220, variation VHHD except for custom features D2, E2, and L which are toleranced per supplier designation.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

7.3 QFN32 Package Marking

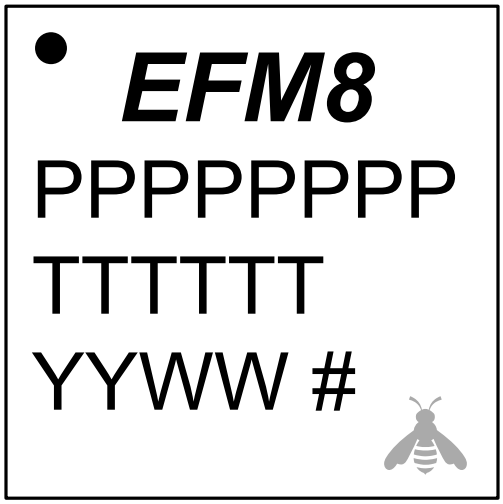

Figure 7.3. QFN32 Package Marking

The package marking consists of:

- PPPPPPPP – The part number designation.
- TTTTTT – A trace or manufacturing code.
- YY – The last 2 digits of the assembly year.
- WW – The 2-digit workweek when the device was assembled.
- # – The device revision (A, B, etc.).

Dimension	Min	Typ	Max
bbb	—	—	0.10
ddd	—	—	0.05
eee	—	—	0.08
Z	—	0.24	—
Y	—	0.18	—

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC Solid State Outline MO-220, variation WGGD except for custom features D2, E2, Z, Y, and L which are toleranced per supplier designation.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

Dimension	Min	Max

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
7. A 2 x 2 array of 1.10 mm x 1.10 mm openings on 1.30 mm pitch should be used for the center ground pad.
8. A No-Clean, Type-3 solder paste is recommended.
9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

8.3 QFN24 Package Marking

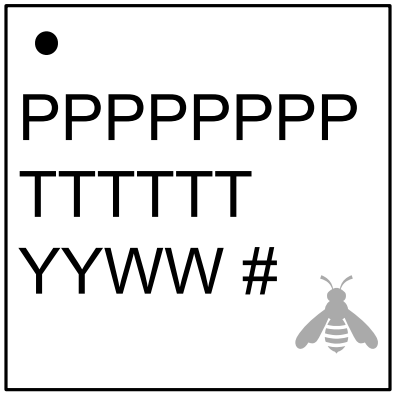

Figure 8.3. QFN24 Package Marking

The package marking consists of:

- PPPPPPPP – The part number designation.
- TTTTTT – A trace or manufacturing code.
- YY – The last 2 digits of the assembly year.
- WW – The 2-digit workweek when the device was assembled.
- # – The device revision (A, B, etc.).

9. QFP32 Package Specifications

9.1 QFP32 Package Dimensions

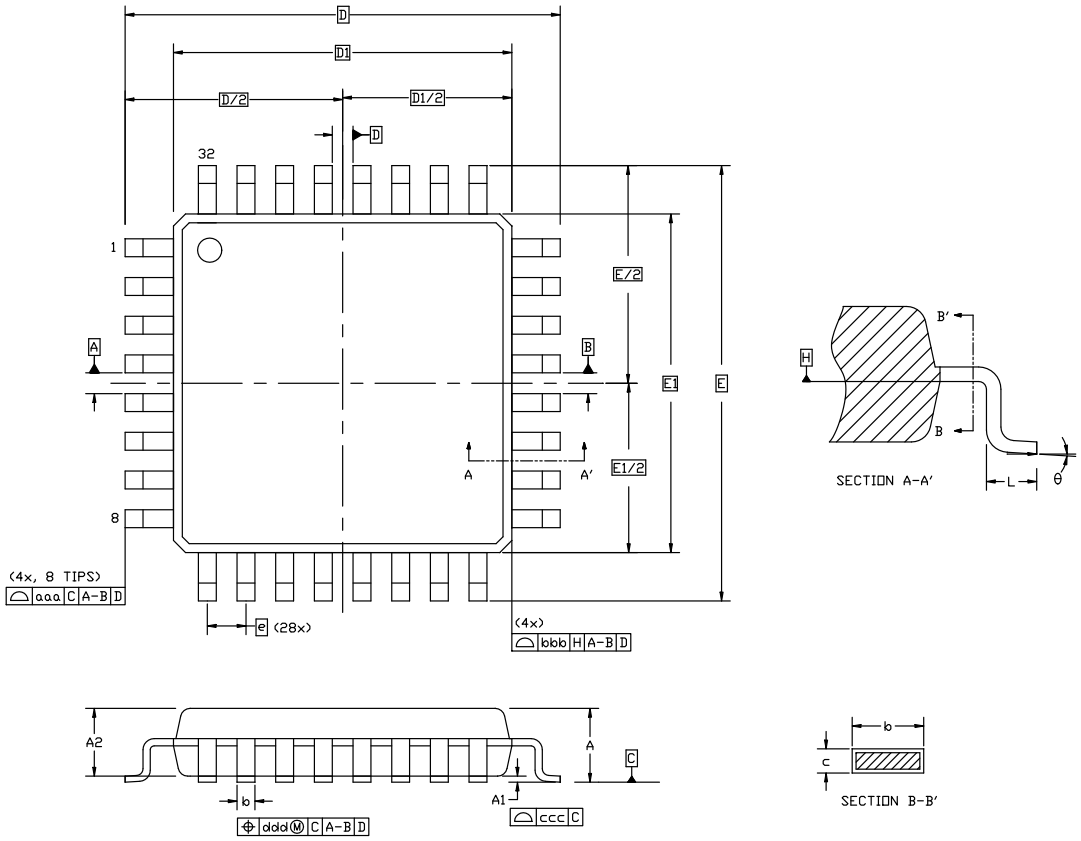

Figure 9.1. QFP32 Package Drawing

Table 9.1. QFP32 Package Dimensions

Dimension	Min	Typ	Max
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
b	0.30	0.37	0.45
D		9.00 BSC	
D1		7.00 BSC	
e		0.80 BSC	
E		9.00 BSC	
E1		7.00 BSC	
L	0.45	0.60	0.75
aaa		0.20	

10. Revision History

10.1 Revision 1.2

Updated ordering part numbers to revision B.

Added Reset Delay from POR specification.

Added I/O 5 V tolerance to 1. Feature List.

Added information on the bootloader to 3.10 Bootloader.

Added a Debug Typical Connection Diagram to 5. Typical Connection Diagrams.

Added reference to the Reference Manual in 3.1 Introduction.

10.2 Revision 1.1

Initial release.

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