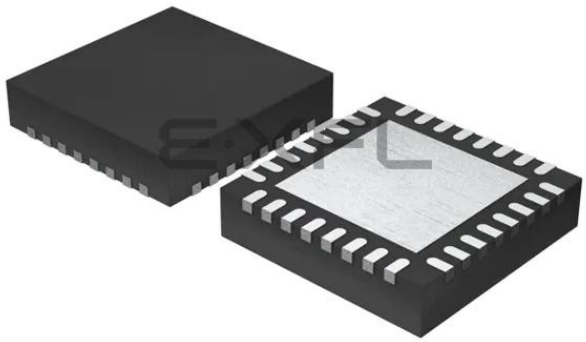

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	CIP-51 8051
Core Size	8-Bit
Speed	25MHz
Connectivity	EBI/EMI, I²C, SMBus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	24
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4.25K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 23x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-VFQFN Exposed Pad
Supplier Device Package	32-QFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm8sb20f64g-b-qfn32r

External Memory Interface (EMIF0)

The External Memory Interface (EMIF) enables access of off-chip memories and memory-mapped devices connected to the GPIO ports. The external memory space may be accessed using the external move instruction (MOVX) with the target address specified in either 8-bit or 16-bit formats.

- Supports multiplexed memory access.
- Four external memory modes:
  - Internal only.
  - Split mode without bank select.
  - Split mode with bank select.
  - External only
- Configurable ALE (address latch enable) timing.
- Configurable address setup and hold times.
- Configurable write and read pulse widths.

16/32-bit CRC (CRC0)

The cyclic redundancy check (CRC) module performs a CRC using a 16-bit or 32-bit polynomial. CRC0 accepts a stream of 8-bit data and posts the result to an internal register. In addition to using the CRC block for data manipulation, hardware can automatically CRC the flash contents of the device.

The CRC module is designed to provide hardware calculations for flash memory verification and communications protocols. The CRC module includes the following features:

- Support for CCITT-16 polynomial (0x1021).
- Support for CRC-32 polynomial (0x04C11DB7).
- Byte-level bit reversal.
- Automatic CRC of flash contents on one or more 1024-byte blocks.
- Initial seed selection of 0x0000/0x00000000 or 0xFFFF/0xFFFFFFFF.

3.7 Analog

Programmable Current Reference (IREF0)

The programmable current reference (IREF0) module enables current source or sink with two output current settings: Low Power Mode and High Current Mode. The maximum current output in Low Power Mode is 63 µA (1 µA steps) and the maximum current output in High Current Mode is 504 µA (8 µA steps).

The IREF module includes the following features:

- Capable of sourcing or sinking current in programmable steps.
- Two operational modes: Low Power Mode and High Current Mode.

10-Bit Analog-to-Digital Converter (ADC0)

The ADC is a successive-approximation-register (SAR) ADC with 10- and 8-bit modes, integrated track-and hold and a programmable window detector. The ADC is fully configurable under software control via several registers. The ADC may be configured to measure different signals using the analog multiplexer. The voltage reference for the ADC is selectable between internal and external reference sources.

- Up to 22 external inputs.
- Single-ended 10-bit mode.
- Supports an output update rate of 300 ksps samples per second.
- Operation in low power modes at lower conversion speeds.
- Asynchronous hardware conversion trigger, selectable between software, external I/O and internal timer sources.
- Output data window comparator allows automatic range checking.
- Support for burst mode, which produces one set of accumulated data per conversion-start trigger with programmable power-on settling and tracking time.
- Conversion complete and window compare interrupts supported.
- Flexible output data formatting.
- Includes an internal 1.65 V fast-settling reference and support for external reference.
- Integrated temperature sensor.

Low Current Comparators (CMP0, CMP1)

Analog comparators are used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. External input connections to device I/O pins and internal connections are available through separate multiplexers on the positive and negative inputs. Hysteresis, response time, and current consumption may be programmed to suit the specific needs of the application.

The comparator module includes the following features:

- Up to 12 external positive inputs.
- Up to 11 external negative inputs.
- Additional input options:
  - Capacitive Sense Comparator output.
  - VDD.
  - VDD divided by 2.
  - Internal connection to LDO output.
  - Direct connection to GND.
- Synchronous and asynchronous outputs can be routed to pins via crossbar.
- Programmable hysteresis between 0 and +/-20 mV.
- Programmable response time.
- Interrupts generated on rising, falling, or both edges.

3.10 Bootloader

All devices come pre-programmed with a UART0 bootloader. This bootloader resides in the code security page, which is the last page of code flash; it can be erased if it is not needed.

The byte before the Lock Byte is the Bootloader Signature Byte. Setting this byte to a value of 0xA5 indicates the presence of the bootloader in the system. Any other value in this location indicates that the bootloader is not present in flash.

When a bootloader is present, the device will jump to the bootloader vector after any reset, allowing the bootloader to run. The bootloader then determines if the device should stay in bootload mode or jump to the reset vector located at 0x0000. When the bootloader is not present, the device will jump to the reset vector of 0x0000 after any reset.

More information about the bootloader protocol and usage can be found in *AN945: EFM8 Factory Bootloader User Guide*. Application notes can be found on the Silicon Labs website (www.silabs.com/8bit-appnotes) or within Simplicity Studio by using the [**Application Notes**] tile.

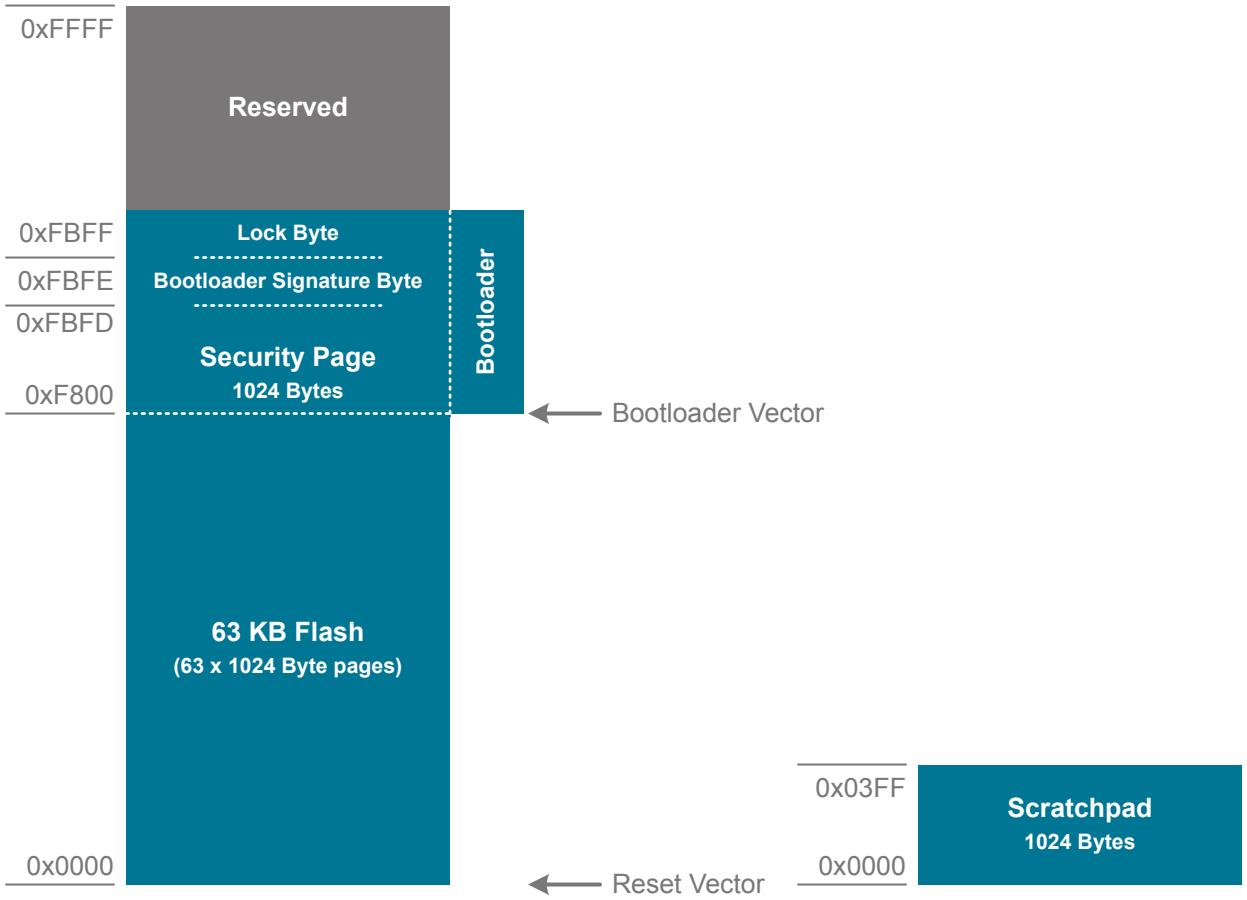

Figure 3.2. Flash Memory Map with Bootloader — 64 KB Devices

4. Electrical Specifications

4.1 Electrical Characteristics

All electrical parameters in all tables are specified under the conditions listed in Table 4.1 Recommended Operating Conditions on page 12, unless stated otherwise.

4.1.1 Recommended Operating Conditions

Table 4.1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating Supply Voltage on VDD	V_{DD}		1.8	2.4	3.6	V
Minimum RAM Data Retention Voltage on VDD[1]	V_{RAM}	Not in Sleep Mode	—	1.4	—	V
		Sleep Mode	—	0.3	0.5	V
System Clock Frequency	f_{SYSCLK}		0	—	25	MHz
Operating Ambient Temperature	T_A		–40	—	85	°C

Note:
1. All voltages with respect to GND.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Comparator 0 (CMP0) Supply Current	I_{CMP}	CPMD = 11	—	0.4	—	µA
		CPMD = 10	—	2.6	—	µA
		CPMD = 01	—	8.8	—	µA
		CPMD = 00	—	23	—	µA
Internal Fast-settling 1.65V ADC0 Reference, Always-on[8]	I_{VREFFS}		—	200	—	µA
On-chip Precision Reference	I_{VREFP}		—	15	—	µA
Temp sensor Supply Current	I_{TSENSE}		—	35	—	µA
Programmable Current Reference (IREF0) Supply Current[9]	I_{IREF}	Current Source, Either Power Mode, Any Output Code	—	10	—	µA
		Low Power Mode, Current Sink IREF0DAT = 000001	—	1	—	µA
		Low Power Mode, Current Sink IREF0DAT = 111111	—	11	—	µA
		High Current Mode, Current Sink IREF0DAT = 000001	—	12	—	µA
		High Current Mode, Current Sink IREF0DAT = 111111	—	81	—	µA

Note:

1. Based on device characterization data; Not production tested.
2. SYSCLK must be at least 32 kHz to enable debugging.
3. Digital Supply Current depends upon the particular code being executed. The values in this table are obtained with the CPU executing an “sjmp $” loop, which is the compiled form of a while(1) loop in C. One iteration requires 3 CPU clock cycles, and the flash memory is read on each cycle. The supply current will vary slightly based on the physical location of the sjmp instruction and the number of flash address lines that toggle as a result. In the worst case, current can increase by up to 30% if the sjmp loop straddles a 128-byte flash address boundary (e.g., 0x007F to 0x0080). Real-world code with larger loops and longer linear sequences will have few transitions across the 128-byte address boundaries.
4. Includes supply current from regulator and oscillator source (24.5 MHz high-frequency oscillator, 20 MHz low-power oscillator, or 32.768 kHz RTC oscillator).
5. IDD can be estimated for frequencies < 10 MHz by simply multiplying the frequency of interest by the frequency sensitivity number for that range, then adding an offset of 90 µA. When using these numbers to estimate I_{DD} for > 10 MHz, the estimate should be the current at 25 MHz minus the difference in current indicated by the frequency sensitivity number. For example: V_{DD} = 3.0 V; F = 20 MHz, I_{DD} = 4.1 mA – (25 MHz – 20 MHz) x 0.120 mA/MHz = 3.5 mA assuming the same oscillator setting.
6. Idle IDD can be estimated by taking the current at 25 MHz minus the difference in current indicated by the frequency sensitivity number. For example: V_{DD} = 3.0 V; F = 5 MHz, Idle I_{DD} = 2.5 mA – (25 MHz – 5 MHz) x 0.095 mA/MHz = 0.6 mA.
7. ADC0 always-on power excludes internal reference supply current.
8. The internal reference is enabled as-needed when operating the ADC in burst mode to save power.
9. IREF0 supply current only. Does not include current sourced or sunk from IREF0 output pin.

4.1.3 Reset and Supply Monitor

Table 4.3. Reset and Supply Monitor

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
VDD Supply Monitor Threshold	V_{VDDM}	Reset Trigger	1.7	1.75	1.8	V
	V_{WARN}	Early Warning	1.8	1.85	1.9	V
VDD Supply Monitor Turn-On Time	t_{MON}		—	300	—	ns
Power-On Reset (POR) Monitor Threshold	V_{POR}	Initial Power-On (Rising Voltage on V_{DD})	—	0.75	—	V
		Falling Voltage on V_{DD}	0.7	0.8	0.9	V
		Brownout Recovery (Rising Voltage on V_{DD})	—	0.95	—	V
V_{DD} Ramp Time	t_{RMP}	Time to V_{DD} ≥ 1.8 V	—	—	3	ms
Reset Delay from POR	t_{POR}	Relative to V_{DD} > V_{POR}	3	10	31	ms
Reset Delay	t_{RST}	Time between release of reset source and code execution	—	10	—	µs
RST Low Time to Generate Reset	t_{RSTL}		15	—	—	µs
Missing Clock Detector Response Time (final rising edge to reset)	t_{MCD}	F_{SYSCLK} > 1 MHz	100	650	1000	µs
Missing Clock Detector Trigger Frequency	F_{MCD}		—	7	10	kHz

4.1.4 Flash Memory

Table 4.4. Flash Memory

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Write Time[1]	t_{WRITE}	One Byte	57	64	71	µs
Erase Time[1]	t_{ERASE}	One Page	28	32	36	ms
Endurance (Write/Erase Cycles)	N_{WE}		1 k	30 k	—	Cycles

Note:
1. Does not include sequencing time before and after the write/erase operation, which may be multiple SYSCLK cycles.
2. Data Retention Information is published in the Quarterly Quality and Reliability Report.

4.1.5 Power Management Timing

Table 4.5. Power Management Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Idle Mode Wake-up Time	t_{IDLEWK}		2	—	3	SYSCLKs
Suspend Mode Wake-up Time	$t_{SUS-PENDWK}$	CLKDIV = 0x00 Precision Osc.	—	400	—	ns
		CLKDIV = 0x00 Low Power Osc.	—	1.3	—	µs
Sleep Mode Wake-up Time	$t_{SLEEPWK}$		—	2	—	µs

4.1.6 Internal Oscillators

Table 4.6. Internal Oscillators

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High Frequency Oscillator 0 (24.5 MHz)						
Oscillator Frequency	f_{HFOSC0}	Full Temperature and Supply Range	24	24.5	25	MHz
Low Power Oscillator (20 MHz)						
Oscillator Frequency	f_{LPOSC}	Full Temperature and Supply Range	18	20	22	MHz
RTC in Self-Oscillate Mode						
Oscillator Frequency	f_{LFOSC}	Bias Off	—	12 ± 5	—	kHz
		Bias On	—	25 ± 10	—	kHz

4.1.7 Crystal Oscillator

Table 4.7. Crystal Oscillator

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal Frequency	f_{XTAL}		0.02	-	25	MHz

4.1.10 Voltage References

Table 4.10. Voltage References

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Internal Fast Settling Reference						
Output Voltage	V_{REFFS}		1.60	1.65	1.70	V
Temperature Coefficient	TC_{REFFS}		—	50	—	ppm/°C
Turn-on Time	t_{VREFFS}		—	—	1.5	µs
Power Supply Rejection	$PSRR_{REFFS}$		—	400	—	ppm/V
On-chip Precision Reference						
Output Voltage	V_{REFP}		1.645	1.68	1.715	V
Turn-on Time, settling to 0.5 LSB	t_{VREFP}	4.7 µF tantalum + 0.1 µF ceramic bypass on VREF pin	—	15	—	ms
		0.1 µF ceramic bypass on VREF pin	—	300	—	µs
		No bypass on VREF pin	—	25	—	µs
Load Regulation	LR_{VREFP}	Load = 0 to 200 µA to GND	—	400	—	µV / µA
Short-circuit current	ISC_{VREFP}		—	3.5	—	mA
Power Supply Rejection	$PSRR_{VREFP}$		—	140	—	ppm/V
External Reference						
Input Voltage	V_{EXTREF}		1	—	V_{DD}	V
Input Current	I_{EXTREF}	Sample Rate = 300 ksps; VREF = 3.0 V	—	5.25	—	µA

4.1.11 Temperature Sensor

Table 4.11. Temperature Sensor

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Offset	V_{OFF}	T_A = 0 °C	—	940	—	mV
Offset Error[1]	E_{OFF}	T_A = 0 °C	—	18	—	mV
Slope	M		—	3.40	—	mV/°C
Slope Error[1]	E_M		—	40	—	µV/°C
Linearity			—	±1	—	°C
Turn-on Time	t_{PWR}		—	1.8	—	µs

Note:
1. Represents one standard deviation from the mean.

4.1.12 Comparators

Table 4.12. Comparators

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Response Time, CPMD = 00 (Highest Speed)	t_{RESP0}	+100 mV Differential	—	130	—	ns
		–100 mV Differential	—	200	—	ns
Response Time, CPMD = 11 (Lowest Power)	t_{RESP3}	+100 mV Differential	—	1.75	—	µs
		–100 mV Differential	—	6.2	—	µs
Positive Hysterisis Mode 0 (CPMD = 00)	HYS_{CP+}	CPHYP = 00	—	0.4	—	mV
		CPHYP = 01	—	8	—	mV
		CPHYP = 10	—	16	—	mV
		CPHYP = 11	—	32	—	mV
Negative Hysterisis Mode 0 (CPMD = 00)	HYS_{CP-}	CPHYN = 00	—	-0.4	—	mV
		CPHYN = 01	—	–8	—	mV
		CPHYN = 10	—	–16	—	mV
		CPHYN = 11	—	–32	—	mV
Positive Hysterisis Mode 1 (CPMD = 01)	HYS_{CP+}	CPHYP = 00	—	0.5	—	mV
		CPHYP = 01	—	6	—	mV
		CPHYP = 10	—	12	—	mV
		CPHYP = 11	—	24	—	mV
Negative Hysterisis Mode 1 (CPMD = 01)	HYS_{CP-}	CPHYN = 00	—	-0.5	—	mV
		CPHYN = 01	—	–6	—	mV
		CPHYN = 10	—	–12	—	mV
		CPHYN = 11	—	–24	—	mV
Positive Hysterisis Mode 2 (CPMD = 10)	HYS_{CP+}	CPHYP = 00	—	0.7	—	mV
		CPHYP = 01	—	4.5	—	mV
		CPHYP = 10	—	9	—	mV
		CPHYP = 11	—	18	—	mV
Negative Hysterisis Mode 2 (CPMD = 10)	HYS_{CP-}	CPHYN = 00	—	-0.6	—	mV
		CPHYN = 01	—	–4.5	—	mV
		CPHYN = 10	—	–9	—	mV
		CPHYN = 11	—	–18	—	mV
Positive Hysteresis Mode 3 (CPMD = 11)	HYS_{CP+}	CPHYP = 00	—	1.5	—	mV
		CPHYP = 01	—	4	—	mV
		CPHYP = 10	—	8	—	mV
		CPHYP = 11	—	16	—	mV

4.3 Absolute Maximum Ratings

Stresses above those listed in Table 4.16 Absolute Maximum Ratings on page 23 may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. For more information on the available quality and reliability data, see the Quality and Reliability Monitor Report at http://www.silabs.com/support/quality/pages/default.aspx.

Table 4.16. Absolute Maximum Ratings

Parameter	Symbol	Test Condition	Min	Max	Unit
Ambient Temperature Under Bias	T_{BIAS}		–55	125	°C
Storage Temperature	T_{STG}		–65	150	°C
Voltage on V_{DD}	V_{DD}		GND–0.3	4.0	V
Voltage on I/O pins or RSTb	V_{IN}	V_{DD} > 2.2 V	GND–0.3	5.8	V
		V_{DD} <= 2.2 V	GND–0.3	V_{DD} + 3.6	V
Total Current Sunk into Supply Pin	I_{VDD}		—	400	mA
Total Current Sourced out of Ground Pin	I_{GND}		400	—	mA
Current Sourced or Sunk by Any I/O Pin or RSTb	I_{IO}		-100	100	mA
Maximum Total Current through all Port Pins	I_{IOTOT}		—	200	mA
Operating Junction Temperature	T_J		–40	105	°C
Exposure to maximum rating conditions for extended periods may affect device reliability.					

6. Pin Definitions

6.1 EFM8SB2x-QFN32 Pin Definitions

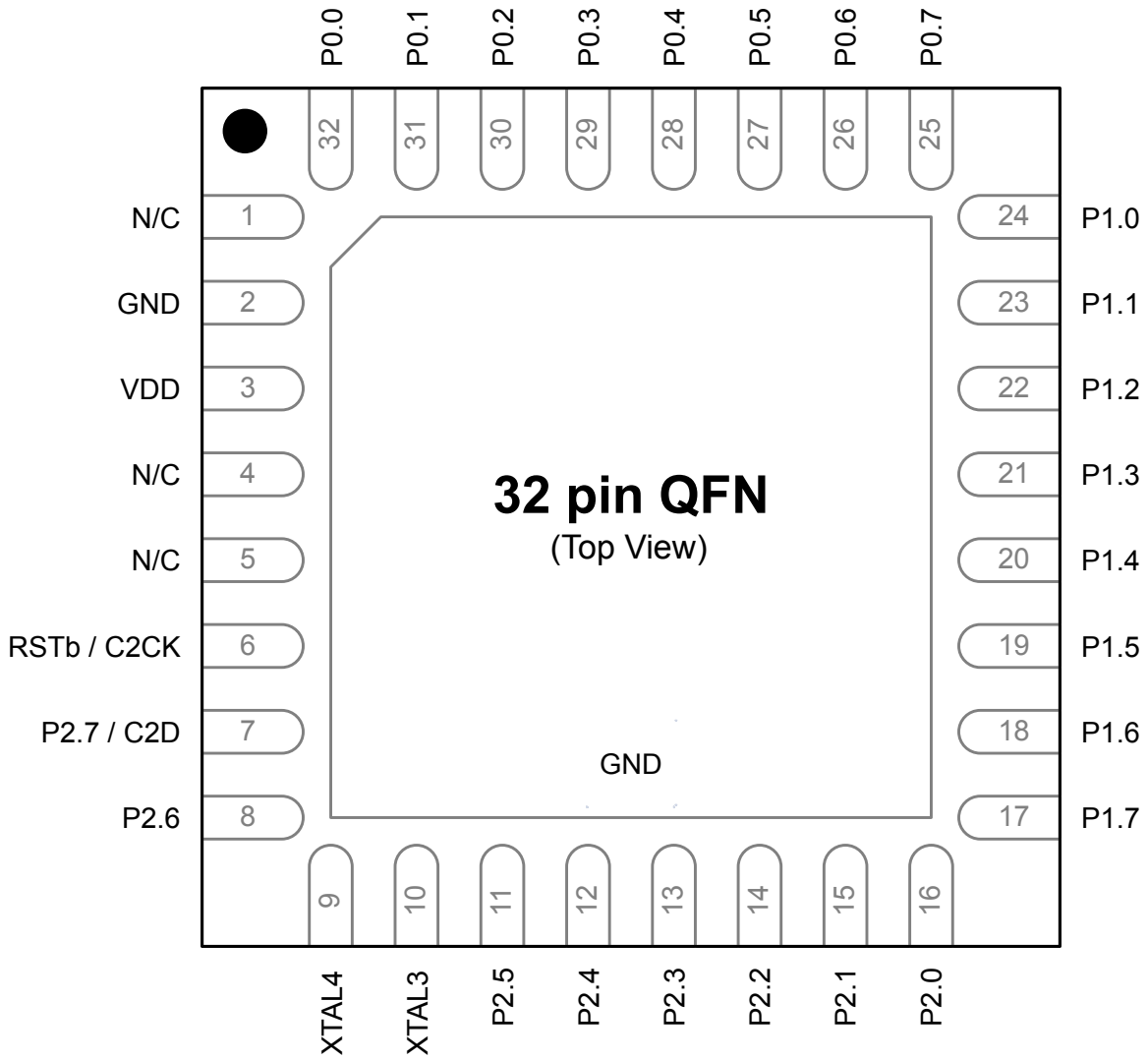

Figure 6.1. EFM8SB2x-QFN32 Pinout

Table 6.1. Pin Definitions for EFM8SB2x-QFN32

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
1	N/C	No Connection			
2	GND	Ground			
3	VDD	Supply Power Input			
4	N/C	No Connection			

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
5	N/C	No Connection			
6	RSTb / C2CK	Active-low Reset / C2 Debug Clock			
7	P2.7 / C2D	Multifunction I/O / C2 Debug Data			
8	P2.6	Multifunction I/O	Yes	EMIF_WRb	ADC0.22 CMP0P.11 CMP1P.11
9	XTAL4	RTC Crystal			XTAL4
10	XTAL3	RTC Crystal			XTAL3
11	P2.5	Multifunction I/O	Yes	EMIF_RDb	ADC0.21 CMP0N.10 CMP1N.10
12	P2.4	Multifunction I/O	Yes	EMIF_ALE	ADC0.20 CMP0P.10 CMP1P.10
13	P2.3	Multifunction I/O	Yes	EMIF_A11	ADC0.19 CMP0N.9 CMP1N.9
14	P2.2	Multifunction I/O	Yes	EMIF_A10	ADC0.18 CMP0P.9 CMP1P.9
15	P2.1	Multifunction I/O	Yes	EMIF_A9	ADC0.17 CMP0N.8 CMP1N.8
16	P2.0	Multifunction I/O	Yes	EMIF_A8	ADC0.16 CMP0P.8 CMP1P.8
17	P1.7	Multifunction I/O	Yes	P1MAT.7 EMIF_AD7	ADC0.15 CMP0N.7 CMP1N.7
18	P1.6	Multifunction I/O	Yes	P1MAT.6 EMIF_AD6	ADC0.14 CMP0P.7 CMP1P.7

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
6	RSTb / C2CK	Active-low Reset / C2 Debug Clock			
7	P2.7 / C2D	Multifunction I/O / C2 Debug Data			
8	XTAL4	RTC Crystal			XTAL4
9	XTAL3	RTC Crystal			XTAL3
10	P1.6	Multifunction I/O	Yes		ADC0.14 CMP0P.7 CMP1P.7
11	P1.5	Multifunction I/O	Yes	P1MAT.5	ADC0.13 CMP0N.6 CMP1N.6
12	P1.4	Multifunction I/O	Yes	P1MAT.4	ADC0.12 CMP0P.6 CMP1P.6
13	P1.3	Multifunction I/O	Yes	P1MAT.3 SPI1_NSS	ADC0.11 CMP0N.5 CMP1N.5
14	P1.2	Multifunction I/O	Yes	P1MAT.2 SPI1_MOSI	ADC0.10 CMP0P.5 CMP1P.5
15	P1.1	Multifunction I/O	Yes	P1MAT.1 SPI1_MISO	ADC0.9 CMP0N.4 CMP1N.4
16	P1.0	Multifunction I/O	Yes	P1MAT.0 SPI1_SCK	ADC0.8 CMP0P.4 CMP1P.4
17	P0.7	Multifunction I/O	Yes	P0MAT.7 INT0.7 INT1.7	ADC0.7 IREF0 CMP0N.3 CMP1N.3
18	P0.6	Multifunction I/O	Yes	P0MAT.6 CNVSTR INT0.6 INT1.6	ADC0.6 CMP0P.3 CMP1P.3

7. QFN32 Package Specifications

7.1 QFN32 Package Dimensions

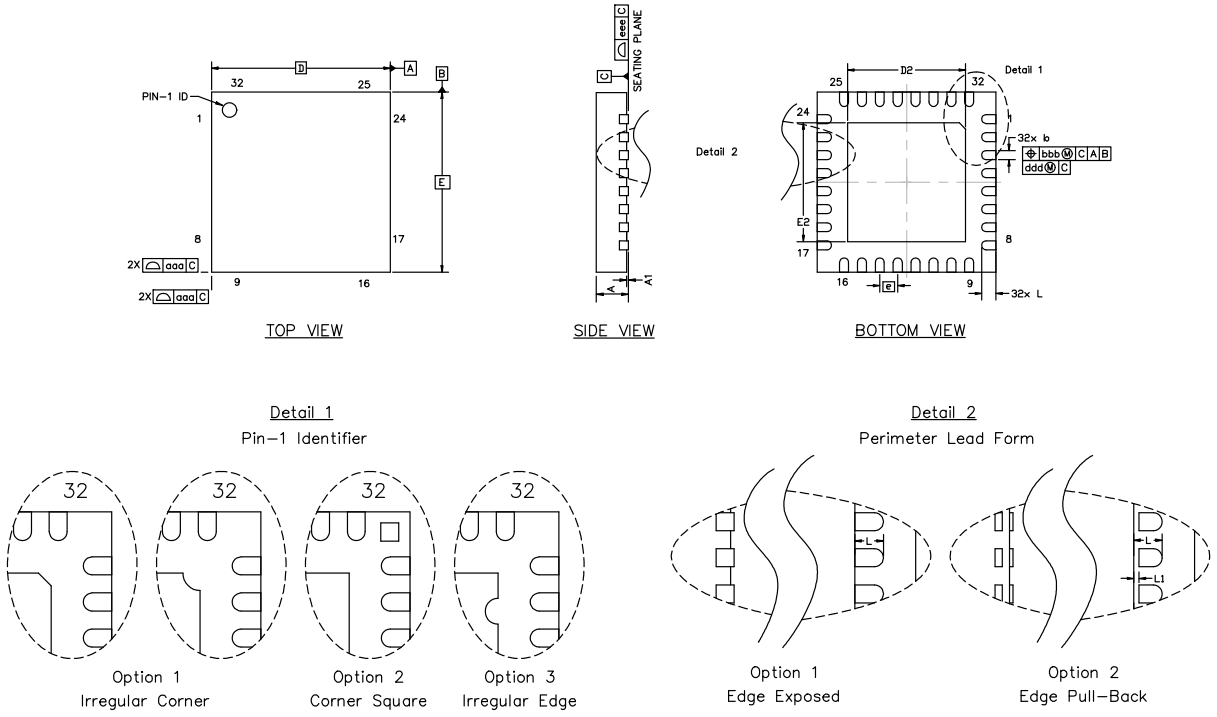

Figure 7.1. QFN32 Package Drawing

Table 7.1. QFN32 Package Dimensions

Dimension	Min	Typ	Max
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D		5.00 BSC	
D2	3.20	3.30	3.40
e		0.50 BSC	
E		5.00 BSC	
E2	3.20	3.30	3.40
L	0.30	0.40	0.50
L1	0.00	—	0.15
aaa	—	—	0.15

Dimension	Min	Typ	Max
bbb	—	—	0.10
ddd	—	—	0.05
eee	—	—	0.08

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC Solid State Outline MO-220, variation VHHD except for custom features D2, E2, and L which are toleranced per supplier designation.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

7.2 QFN32 PCB Land Pattern

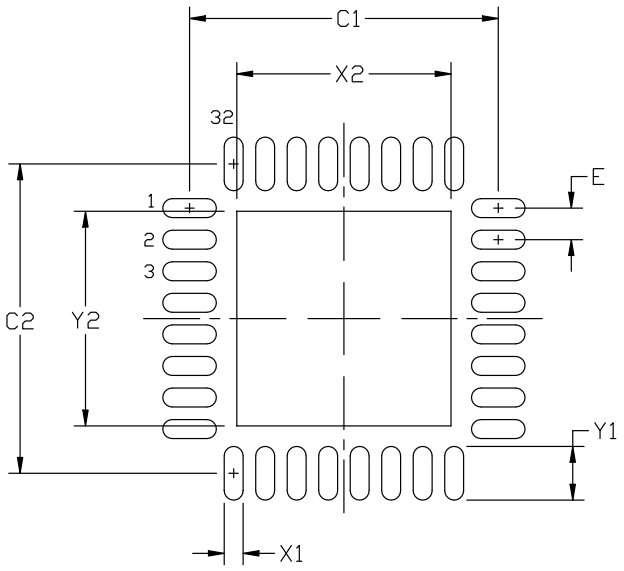

Figure 7.2. QFN32 PCB Land Pattern Drawing

Table 7.2. QFN32 PCB Land Pattern Dimensions

Dimension	Min	Max
C1	4.80	4.90
C2	4.80	4.90
E	0.50 BSC	
X1	0.20	0.30
X2	3.20	3.40
Y1	0.75	0.85
Y2	3.20	3.40

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
7. A 3 x 3 array of 1.0 mm x 1.0 mm openings on a 1.2 mm pitch should be used for the center pad.
8. A No-Clean, Type-3 solder paste is recommended.
9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

Dimension	Min	Typ	Max
bbb	—	—	0.10
ddd	—	—	0.05
eee	—	—	0.08
Z	—	0.24	—
Y	—	0.18	—

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC Solid State Outline MO-220, variation WGGD except for custom features D2, E2, Z, Y, and L which are toleranced per supplier designation.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

9.2 QFP32 PCB Land Pattern

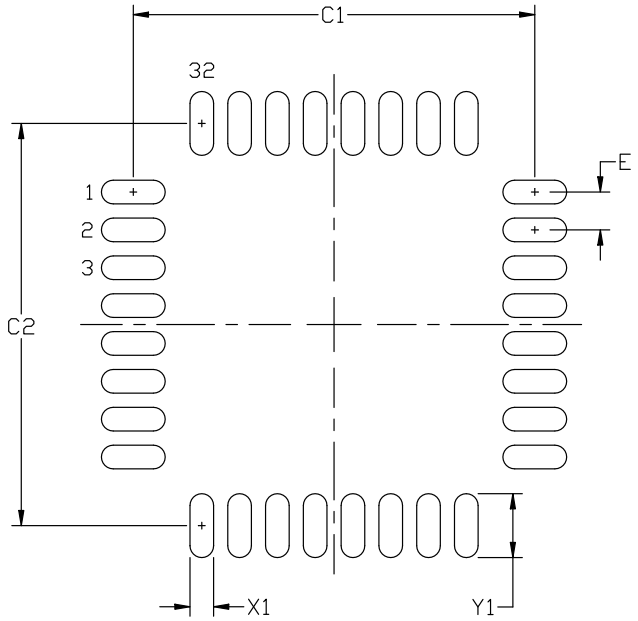

Figure 9.2. QFP32 PCB Land Pattern Drawing

Table 9.2. QFP32 PCB Land Pattern Dimensions

Dimension	Min	Max
C1	8.40	8.50
C2	8.40	8.50
E	0.80 BSC	
X1	0.40	0.50
Y1	1.25	1.35

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
7. A No-Clean, Type-3 solder paste is recommended.
8. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

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