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Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e600
Number of Cores/Bus Width	2 Core, 32-Bit
Speed	1.0GHz
Co-Processors/DSP	-
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (4)
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	1023-BBGA, FCBGA
Supplier Device Package	1023-FCCBGA (33x33)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc8641dhx1000ne

5 RESET Initialization

This section describes the AC electrical specifications for the RESET initialization timing requirements of the MPC8641. [Table 11](#) provides the RESET initialization AC timing specifications.

Table 11. RESET Initialization Timing Specifications

Parameter/Condition	Min	Max	Unit	Notes
Required assertion time of $\overline{\text{HRESET}}$	100	—	μs	—
Minimum assertion time for $\overline{\text{SRESET}}_0$ & $\overline{\text{SRESET}}_1$	3	—	SYCLKs	1
Platform PLL input setup time with stable SYCLK before $\overline{\text{HRESET}}$ negation	100	—	μs	2
Input setup time for POR configs (other than PLL config) with respect to negation of $\overline{\text{HRESET}}$	4	—	SYCLKs	1
Input hold time for all POR configs (including PLL config) with respect to negation of $\overline{\text{HRESET}}$	2	—	SYCLKs	1
Maximum valid-to-high impedance time for actively driven POR configs with respect to negation of $\overline{\text{HRESET}}$	—	5	SYCLKs	1

Notes:

1. SYCLK is the primary clock input for the MPC8641.
- 2 This is related to $\overline{\text{HRESET}}$ assertion time. Stable PLL configuration inputs are required when a stable SYCLK is applied. See the *MPC8641D Integrated Host Processor Reference Manual* for more details on the power-on reset sequence.

[Table 12](#) provides the PLL lock times.

Table 12. PLL Lock Times

Parameter/Condition	Min	Max	Unit	Notes
(Platform and E600) PLL lock times	—	100	μs	1
Local bus PLL	—	50	μs	—

Note:

- 1.The PLL lock time for e600 PLLs require an additional 255 MPX_CLK cycles.

6.2 DDR SDRAM AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR SDRAM interface.

6.2.1 DDR SDRAM Input AC Timing Specifications

Table 18 provides the input AC timing specifications for the DDR2 SDRAM when $Dn_GV_{DD}(typ)=1.8\text{ V}$.

Table 18. DDR2 SDRAM Input AC Timing Specifications for 1.8-V Interface

At recommended operating conditions

Parameter	Symbol	Min	Max	Unit	Notes
AC input low voltage 400, 533 MHz 600 MHz	V_{IL}	—	$Dn_MV_{REF} - 0.25$ $Dn_MV_{REF} - 0.20$	V	—
AC input high voltage 400, 533 MHz 600 MHz	V_{IH}	$Dn_MV_{REF} + 0.25$ $Dn_MV_{REF} + 0.20$	—	V	—

Table 19 provides the input AC timing specifications for the DDR SDRAM when $Dn_GV_{DD}(typ)=2.5\text{ V}$.

Table 19. DDR SDRAM Input AC Timing Specifications for 2.5-V Interface

At recommended operating conditions.

Parameter	Symbol	Min	Max	Unit	Notes
AC input low voltage	V_{IL}	—	$Dn_MV_{REF} - 0.31$	V	—
AC input high voltage	V_{IH}	$Dn_MV_{REF} + 0.31$	—	V	—

Table 20 provides the input AC timing specifications for the DDR SDRAM interface.

Table 20. DDR SDRAM Input AC Timing Specifications

At recommended operating conditions.

Parameter	Symbol	Min	Max	Unit	Notes
Controller Skew for MDQS—MDQ/MECC	t_{CISKEW}	—	240 300 365	ps	1, 2
600 MHz	—	–240		—	3
533 MHz	—	–300		—	3
400 MHz	—	–365		—	—

Note:

- t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that will be captured with MDQS[n]. This should be subtracted from the total timing budget.
- The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called t_{DISKEW} . This can be determined by the following equation: $t_{DISKEW} = \pm(T/4 - \text{abs}(t_{CISKEW}))$ where T is the clock period and $\text{abs}(t_{CISKEW})$ is the absolute value of t_{CISKEW} .
- Maximum DDR1 frequency is 400 MHz.

Figure 4 shows the DDR SDRAM input timing for the MDQS to MDQ skew measurement (t_{DISKEW}).

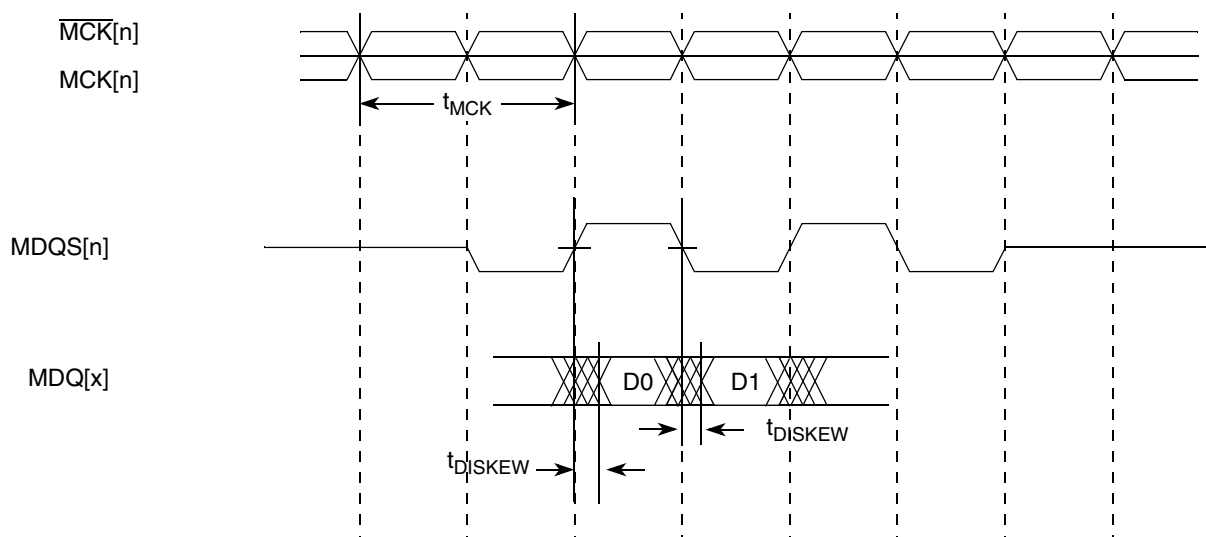


Figure 4. DDR Input Timing Diagram for t_{DISKEW}

6.2.2 DDR SDRAM Output AC Timing Specifications

Table 21. DDR SDRAM Output AC Timing Specifications

At recommended operating conditions.

Parameter	Symbol ¹	Min	Max	Unit	Notes
MCK[n] cycle time, MCK[n]/ $\overline{\text{MCK}}[n]$ crossing	t_{MCK}	3	10	ns	2
MCK duty cycle	t_{MCKH}/t_{MCK}			%	
600 MHz		47.5	52.5		8
533 MHz		47	53		9
400 MHz		47	53		9
ADDR/CMD output setup with respect to MCK	t_{DDKHAS}			ns	3
600 MHz		1.10	—		7
533 MHz		1.48	—		7
400 MHz		1.95	—		
ADDR/CMD output hold with respect to MCK	t_{DDKHAX}			ns	3
600 MHz		1.10	—		7
533 MHz		1.48	—		7
400 MHz		1.95	—		
$\overline{\text{MCS}}[n]$ output setup with respect to MCK	t_{DDKHCS}			ns	3
600 MHz		1.10	—		7
533 MHz		1.48	—		7
400 MHz		1.95	—		

8.2.7 RMII AC Timing Specifications

This section describes the RMII transmit and receive AC timing specifications.

8.2.7.1 RMII Transmit AC Timing Specifications

The RMII transmit AC timing specifications are in [Table 36](#).

Table 36. RMII Transmit AC Timing Specifications

At recommended operating conditions with L/TV_{DD} of 3.3 V ± 5%.

Parameter/Condition	Symbol ¹	Min	Typ	Max	Unit
REF_CLK clock period	t_{RMT}	—	20.0	—	ns
REF_CLK duty cycle	t_{RMTH}/t_{RMT}	35	50	65	%
REF_CLK peak-to-peak jitter	t_{RMTJ}	—	—	250	ps
Rise time REF_CLK (20%–80%)	t_{RMTR}	1.0	—	2.0	ns
Fall time REF_CLK (80%–20%)	t_{RMTF}	1.0	—	2.0	ns
REF_CLK to RMII data TXD[1:0], TX_EN delay	t_{RMTDX}	1.0	—	10.0	ns

Note:

- The symbols used for timing specifications herein follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)\ (reference)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

[Figure 20](#) shows the RMII transmit AC timing diagram.

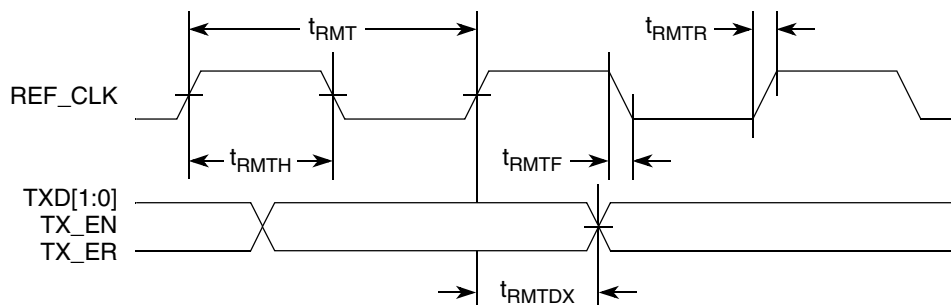


Figure 20. RMII Transmit AC Timing Diagram

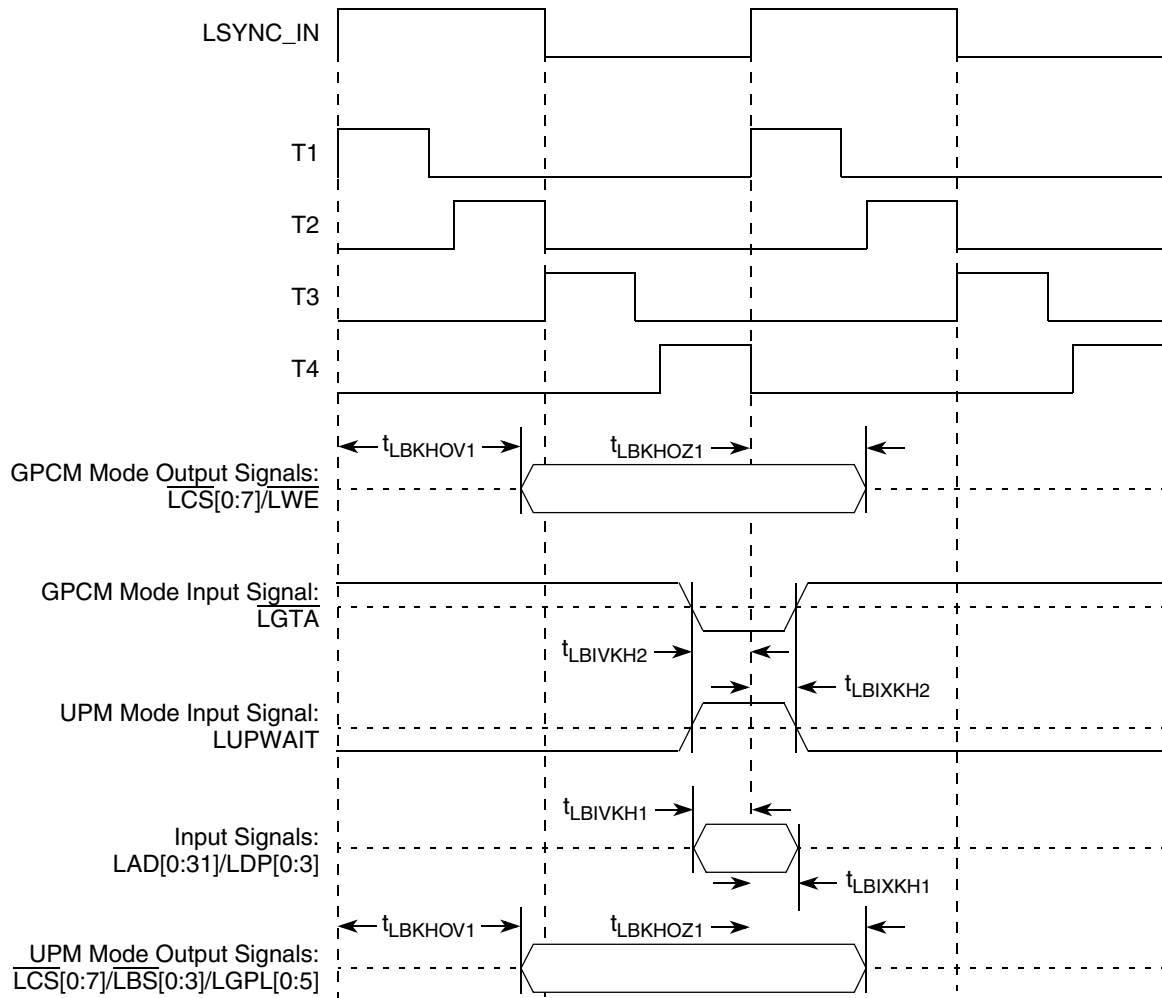


Figure 30. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 4 or 8 (clock ratio of 8 or 16) (PLL Enabled)

Table 45. I²C DC Electrical Characteristics (continued)

At recommended operating conditions with OV_{DD} of 3.3 V ± 5%.

Parameter	Symbol	Min	Max	Unit	Notes
Capacitance for each I/O pin	C _I	—	10	pF	—

Notes:

1. Output voltage (open drain or open collector) condition = 3 mA sink current.
2. Refer to the *MPC8641 Integrated Host Processor Reference Manual* for information on the digital filter used.
3. I/O pins will obstruct the SDA and SCL lines if OV_{DD} is switched off.

12.2 I²C AC Electrical Specifications

Table 46 provides the AC timing parameters for the I²C interfaces.

Table 46. I²C AC Electrical Specifications

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 45).

Parameter	Symbol ¹	Min	Max	Unit
SCL clock frequency	f _{I2C}	0	400	kHz
Low period of the SCL clock	t _{I2CL} ⁴	1.3	—	μs
High period of the SCL clock	t _{I2CH} ⁴	0.6	—	μs
Setup time for a repeated START condition	t _{I2SVKH} ⁴	0.6	—	μs
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t _{I2SXKL} ⁴	0.6	—	μs
Data setup time	t _{I2DVKH} ⁴	100	—	ns
Data input hold time: CBUS compatible masters I ² C bus devices	t _{I2DXKL}	— 0 ²	— —	μs
Rise time of both SDA and SCL signals	t _{I2CR}	20 + 0.1 C _B ⁵	300	ns
Fall time of both SDA and SCL signals	t _{I2CF}	20 + 0.1 C _b ⁵	300	ns
Data output delay time	t _{I2OVKL}	—	0.9 ³	μs
Set-up time for STOP condition	t _{I2PVKH}	0.6	—	μs
Bus free time between a STOP and START condition	t _{I2KHDX}	1.3	—	μs
Noise margin at the LOW level for each connected device (including hysteresis)	V _{NL}	0.1 × OV _{DD}	—	V

- The input amplitude requirement
 - This requirement is described in detail in the following sections.

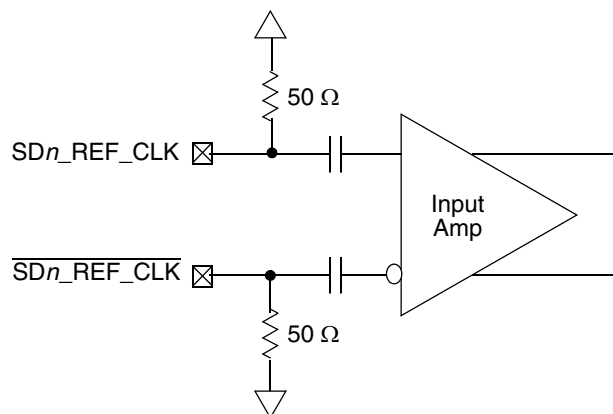


Figure 39. Receiver of SerDes Reference Clocks

13.2.2 DC Level Requirement for SerDes Reference Clocks

The DC level requirement for the MPC8641D SerDes reference clock inputs is different depending on the signaling mode used to connect the clock driver chip and SerDes reference clock inputs as described below.

- **Differential Mode**
 - The input amplitude of the differential clock must be between 400 mV and 1600 mV differential peak-peak (or between 200 mV and 800 mV differential peak). In other words, each signal wire of the differential pair must have a single-ended swing less than 800mV and greater than 200 mV. This requirement is the same for both external DC-coupled or AC-coupled connection.
 - For **external DC-coupled** connection, as described in [Section 13.2.1, “SerDes Reference Clock Receiver Characteristics,”](#) the maximum average current requirements sets the requirement for average voltage (common mode voltage) to be between 100 mV and 400 mV. [Figure 40](#) shows the SerDes reference clock input requirement for DC-coupled connection scheme.
 - For **external AC-coupled** connection, there is no common mode voltage requirement for the clock driver. Since the external AC-coupling capacitor blocks the DC level, the clock driver and the SerDes reference clock receiver operate in different command mode voltages. The SerDes reference clock receiver in this connection scheme has its common mode voltage set to SGND. Each signal wire of the differential inputs is allowed to swing below and above the command mode voltage (SGND). [Figure 41](#) shows the SerDes reference clock input requirement for AC-coupled connection scheme.
- **Single-ended Mode**
 - The reference clock can also be single-ended. The SDn_REF_CLK input amplitude (single-ended swing) must be between 400 mV and 800 mV peak-peak (from V_{min} to V_{max}) with $\overline{SDn_REF_CLK}$ either left unconnected or tied to ground.

- The SDn_REF_CLK input average voltage must be between 200 and 400 mV. Figure 42 shows the SerDes reference clock input requirement for single-ended signaling mode.
- To meet the input amplitude requirement, the reference clock inputs might need to be DC or AC-coupled externally. For the best noise performance, the reference of the clock could be DC or AC-coupled into the unused phase (SDn_REF_CLK) through the same source impedance as the clock input (SDn_REF_CLK) in use.

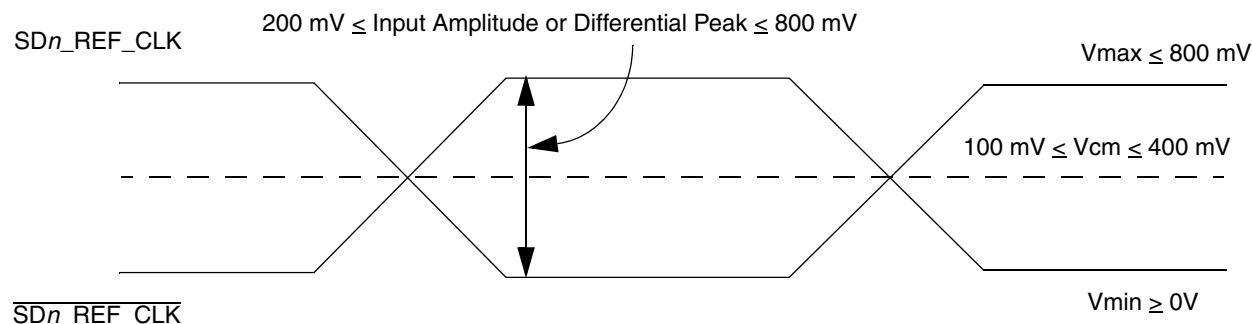


Figure 40. Differential Reference Clock Input DC Requirements (External DC-Coupled)

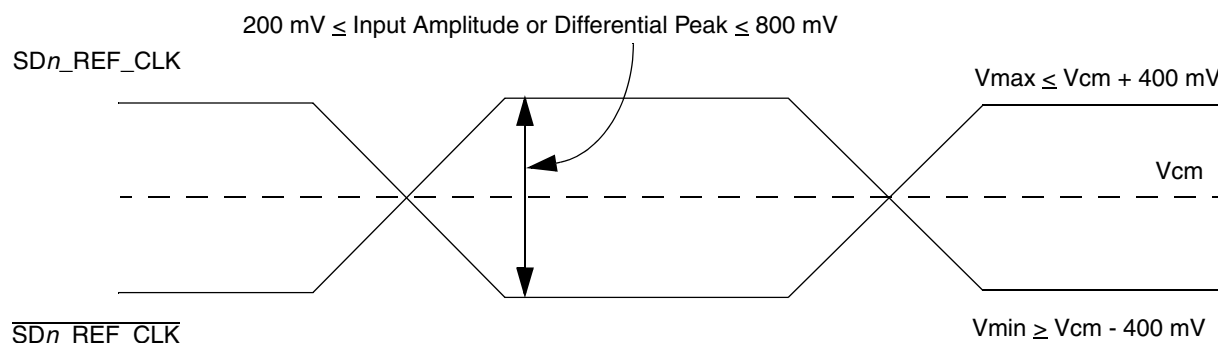


Figure 41. Differential Reference Clock Input DC Requirements (External AC-Coupled)

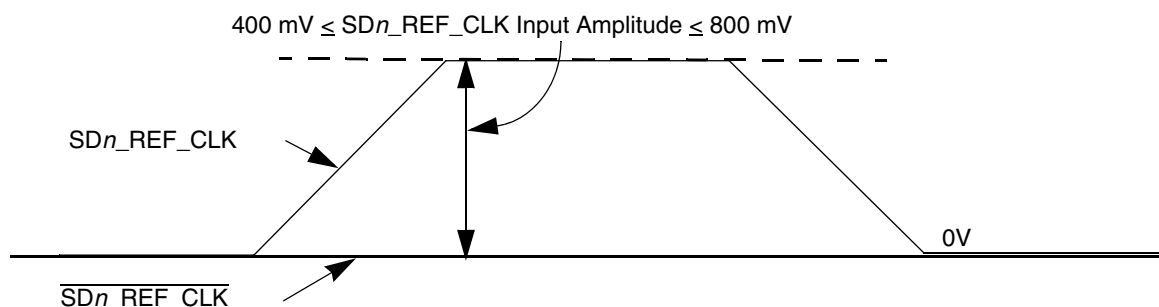


Figure 42. Single-Ended Reference Clock Input DC Requirements

MPC8641D SerDes reference clock input's DC requirement, AC-coupling has to be used. Figure 45 assumes that the LVPECL clock driver's output impedance is $50\ \Omega$. R1 is used to DC-bias the LVPECL outputs prior to AC-coupling. Its value could be ranged from $140\ \Omega$ to $240\ \Omega$ depending on clock driver vendor's requirement. R2 is used together with the SerDes reference clock receiver's $50\text{-}\Omega$ termination resistor to attenuate the LVPECL output's differential peak level such that it meets the MPC8641D SerDes reference clock's differential input amplitude requirement (between 200 mV and 800 mV differential peak). For example, if the LVPECL output's differential peak is 900 mV and the desired SerDes reference clock input amplitude is selected as 600 mV , the attenuation factor is 0.67 , which requires $R2 = 25\ \Omega$. Please consult clock driver chip manufacturer to verify whether this connection scheme is compatible with a particular clock driver chip.

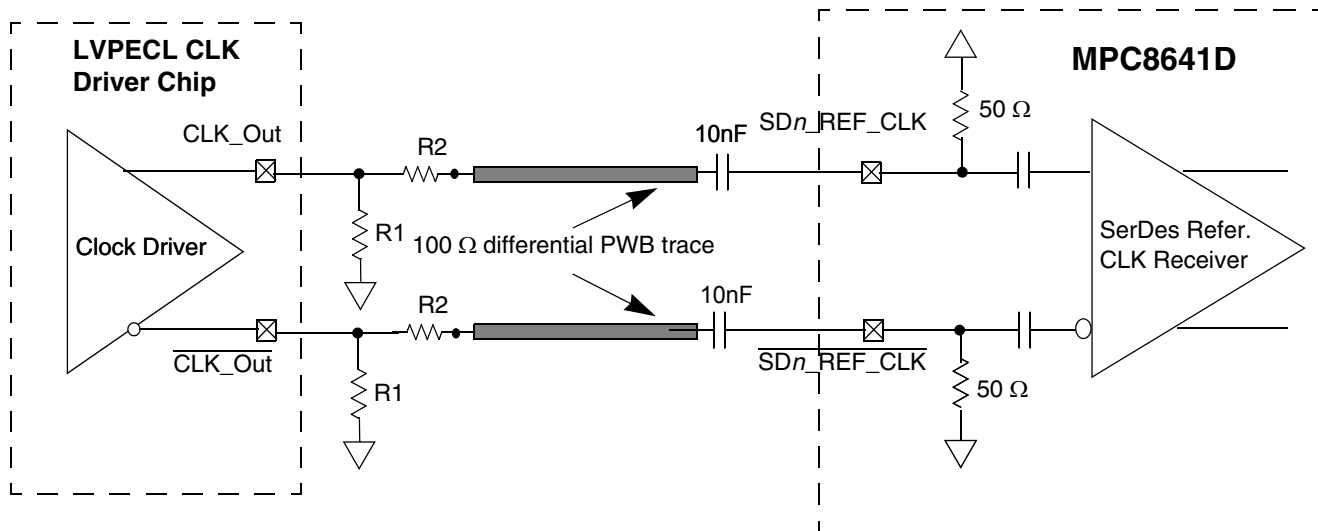


Figure 45. AC-Coupled Differential Connection with LVPECL Clock Driver (Reference Only)

Table 51. SDn_REF_CLK and $\overline{\text{SDn_REF_CLK}}$ AC Requirements

Symbol	Parameter Description	Min	Typical	Max	Units	Comments
t_{REF}	REFCLK cycle time	—	10(8)	—	ns	8 ns applies only to serial RapidIO with 125-MHz reference clock
t_{REFCJ}	REFCLK cycle-to-cycle jitter. Difference in the period of any two adjacent REFCLK cycles	—	—	80	ps	—
t_{REFPJ}	Phase jitter. Deviation in edge location with respect to mean edge location	–40	—	40	ps	—

15.3 Signal Definitions

LP-Serial links use differential signaling. This section defines terms used in the description and specification of differential signals. Figure 53 shows how the signals are defined. The figures show waveforms for either a transmitter output (TD and $\overline{\text{TD}}$) or a receiver input (RD and $\overline{\text{RD}}$). Each signal swings between A Volts and B Volts where $A > B$. Using these waveforms, the definitions are as follows:

1. The transmitter output signals and the receiver input signals TD, $\overline{\text{TD}}$, RD and $\overline{\text{RD}}$ each have a peak-to-peak swing of $A - B$ Volts
2. The differential output signal of the transmitter, V_{OD} , is defined as $V_{\text{TD}} - V_{\overline{\text{TD}}}$
3. The differential input signal of the receiver, V_{ID} , is defined as $V_{\text{RD}} - V_{\overline{\text{RD}}}$
4. The differential output signal of the transmitter and the differential input signal of the receiver each range from $A - B$ to $-(A - B)$ Volts
5. The peak value of the differential transmitter output signal and the differential receiver input signal is $A - B$ Volts
6. The peak-to-peak value of the differential transmitter output signal and the differential receiver input signal is $2 * (A - B)$ Volts

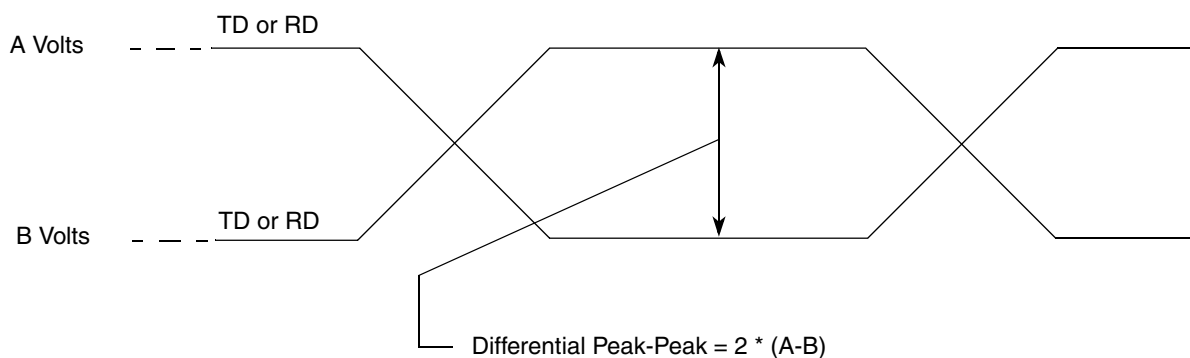


Figure 53. Differential Peak-Peak Voltage of Transmitter or Receiver

To illustrate these definitions using real values, consider the case of a CML (Current Mode Logic) transmitter that has a common mode voltage of 2.25 V and each of its outputs, TD and $\overline{\text{TD}}$, has a swing that goes between 2.5V and 2.0V. Using these values, the peak-to-peak voltage swing of the signals TD and $\overline{\text{TD}}$ is 500 mV p-p. The differential output signal ranges between 500 mV and –500 mV. The peak differential voltage is 500 mV. The peak-to-peak differential voltage is 1000 mV p-p.

Table 57. Long Run Transmitter AC Timing Specifications—3.125 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output Voltage,	V_O	-0.40	2.30	Volts	Voltage relative to COMMON of either signal comprising a differential pair
Differential Output Voltage	V_{DIFFPP}	800	1600	mV p-p	—
Deterministic Jitter	J_D	—	0.17	UI p-p	—
Total Jitter	J_T	—	0.35	UI p-p	—
Multiple output skew	S_{MO}	—	1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	320	320	ps	+/- 100 ppm

For each baud rate at which an LP-Serial transmitter is specified to operate, the output eye pattern of the transmitter shall fall entirely within the unshaded portion of the Transmitter Output Compliance Mask shown in Figure 54 with the parameters specified in Table 58 when measured at the output pins of the device and the device is driving a 100 Ω +/-5% differential resistive load. The output eye pattern of an LP-Serial transmitter that implements pre-emphasis (to equalize the link and reduce inter-symbol interference) need only comply with the Transmitter Output Compliance Mask when pre-emphasis is disabled or minimized.

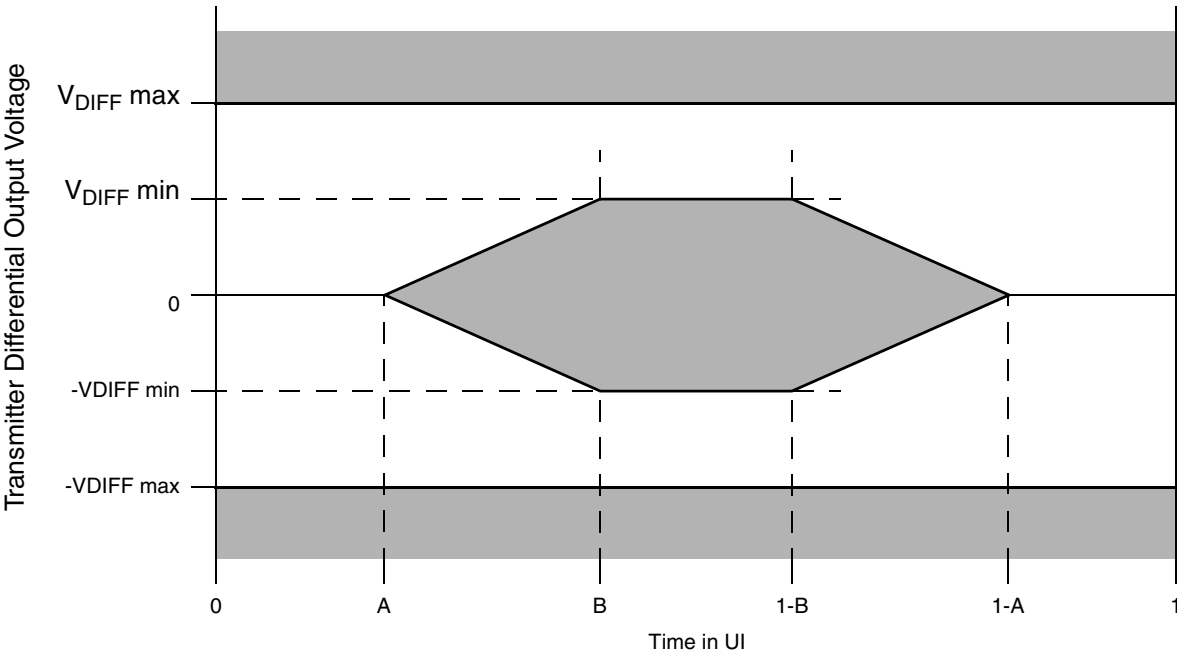


Figure 54. Transmitter Output Compliance Mask

Table 58. Transmitter Differential Output Eye Diagram Parameters

Transmitter Type	V _{DIFFmin} (mV)	V _{DIFFmax} (mV)	A (UI)	B (UI)
1.25 GBaud short range	250	500	0.175	0.39
1.25 GBaud long range	400	800	0.175	0.39
2.5 GBaud short range	250	500	0.175	0.39
2.5 GBaud long range	400	800	0.175	0.39
3.125 GBaud short range	250	500	0.175	0.39
3.125 GBaud long range	400	800	0.175	0.39

15.7 Receiver Specifications

LP-Serial receiver electrical and timing specifications are stated in the text and tables of this section.

Receiver input impedance shall result in a differential return loss better than 10 dB and a common mode return loss better than 6 dB from 100 MHz to (0.8)*(Baud Frequency). This includes contributions from on-chip circuitry, the chip package and any off-chip components related to the receiver. AC coupling components are included in this requirement. The reference impedance for return loss measurements is 100 Ohm resistive for differential return loss and 25 Ohm resistive for common mode.

Table 59. Receiver AC Timing Specifications—1.25 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Differential Input Voltage	V _{IN}	200	1600	mV p-p	Measured at receiver
Deterministic Jitter Tolerance	J _D	0.37	—	UI p-p	Measured at receiver
Combined Deterministic and Random Jitter Tolerance	J _{DR}	0.55	—	UI p-p	Measured at receiver
Total Jitter Tolerance ¹	J _T	0.65	—	UI p-p	Measured at receiver
Multiple Input Skew	S _{MI}	—	24	ns	Skew at the receiver input between lanes of a multilane link
Bit Error Rate	BER	—	10 ⁻¹²	—	—
Unit Interval	UI	800	800	ps	+/- 100 ppm

Note:

1. Total jitter is composed of three components, deterministic jitter, random jitter and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of [Figure 55](#). The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects.

Table 63. MPC8641 Signal Reference by Functional Block (continued)

Name ¹	Package Pin Number	Pin Type	Power Supply	Notes
SD1_PLL_TPA	T28	Analog	SV _{DD}	13, 18
SD1_DLL_TPD	N28	O	SV _{DD}	13, 17
SD1_DLL_TPA	P31	Analog	SV _{DD}	13, 18
High Speed I/O Interface 2 (SERDES 2)⁴				
SD2_TX[0:3]	Y24, AA27, AB25, AC27	O	SV _{DD}	—
SD2_TX[4:7]	AE27, AG27, AJ27, AL27	O	SV _{DD}	34
$\overline{\text{SD2_TX}}[0:3]$	Y25, AA28, AB26, AC28	O	SV _{DD}	—
$\overline{\text{SD2_TX}}[4:7]$	AE28, AG28, AJ28, AL28	O	SV _{DD}	34
SD2_RX[0:3]	Y30, AA32, AB30, AC32	I	SV _{DD}	32
SD2_RX[4:7]	AH30, AJ32, AK30, AL32	I	SV _{DD}	32, 35
$\overline{\text{SD2_RX}}[0:3]$	Y29, AA31, AB29, AC31	I	SV _{DD}	—
$\overline{\text{SD2_RX}}[4:7]$	AH29, AJ31, AK29, AL31	I	SV _{DD}	35
SD2_REF_CLK	AE32	I	SV _{DD}	—
$\overline{\text{SD2_REF_CLK}}$	AE31	I	SV _{DD}	—
SD2_IMP_CAL_TX	AM29	Analog	SV _{DD}	19
SD2_IMP_CAL_RX	AA26	Analog	SV _{DD}	30
SD2_PLL_TPD	AF29	O	SV _{DD}	13, 17
SD2_PLL_TPA	AF31	Analog	SV _{DD}	13, 18
SD2_DLL_TPD	AD29	O	SV _{DD}	13, 17
SD2_DLL_TPA	AD30	Analog	SV _{DD}	13, 18
Special Connection Requirement pins				
No Connects	K24, K25, P28, P29, W26, W27, AD25, AD26	—	—	13
Reserved	H30, R32, V28, AG32	—	—	14
Reserved	H29, R31, W28, AG31	—	—	15
Reserved	AD24, AG26	—	—	16
Ethernet Miscellaneous Signals⁵				
EC1_GTX_CLK125	AL23	I	LV _{DD}	39
EC2_GTX_CLK125	AM23	I	TV _{DD}	39
EC_MDC	G31	O	OV _{DD}	—
EC_MDIO	G32	I/O	OV _{DD}	—
eTSEC Port 1 Signals⁵				

Table 63. MPC8641 Signal Reference by Functional Block (continued)

Name ¹	Package Pin Number	Pin Type	Power Supply	Notes
IRQ[9]/DMA_DREQ[3]	B30	I	OV _{DD}	10
IRQ[10]/DMA_DACK[3]	C30	I	OV _{DD}	9, 10
IRQ[11]/DMA_DDONE[3]	D30	I	OV _{DD}	9, 10
IRQ_OUT	J26	O	OV _{DD}	7, 11
DUART Signals⁵				
UART_SIN[0:1]	B32, C32	I	OV _{DD}	—
UART_SOUT[0:1]	D31, A32	O	OV _{DD}	—
UART_CTS[0:1]	A31, B31	I	OV _{DD}	—
UART_RTS[0:1]	C31, E30	O	OV _{DD}	—
I²C Signals				
IIC1_SDA	A16	I/O	OV _{DD}	7, 11
IIC1_SCL	B17	I/O	OV _{DD}	7, 11
IIC2_SDA	A21	I/O	OV _{DD}	7, 11
IIC2_SCL	B21	I/O	OV _{DD}	7, 11
System Control Signals⁵				
HRESET	B18	I	OV _{DD}	—
HRESET_REQ	K18	O	OV _{DD}	—
SMI_0	L15	I	OV _{DD}	—
SMI_1	L16	I	OV _{DD}	12, S4
SRESET_0	C20	I	OV _{DD}	—
SRESET_1	C21	I	OV _{DD}	12, S4
CKSTP_IN	L18	I	OV _{DD}	—
CKSTP_OUT	L17	O	OV _{DD}	7, 11
READY/TRIG_OUT	J13	O	OV _{DD}	10, 25
Debug Signals⁵				
TRIG_IN	J14	I	OV _{DD}	—
TRIG_OUT/READY	J13	O	OV _{DD}	10, 25
D1_MSRCID[0:1]/ LB_SRCID[0:1]	F15, K15	O	OV _{DD}	6, 10
D1_MSRCID[2]/ LB_SRCID[2]	K14	O	OV _{DD}	10, 25
D1_MSRCID[3:4]/ LB_SRCID[3:4]	H15, G15	O	OV _{DD}	10
D2_MSRCID[0:4]	E16, C17, F16, H16, K16	O	OV _{DD}	—

Table 63. MPC8641 Signal Reference by Functional Block (continued)

Name ¹	Package Pin Number	Pin Type	Power Supply	Notes
AGND_SRDS1	P30	SerDes Port 1 Ground pin for AV _{DD} _SRDS1	—	—
AGND_SRDS2	AF30	SerDes Port 2 Ground pin for AV _{DD} _SRDS2	—	—
SGND	H28, H32, J30, K31, L28, L29, M32, N30, R29, T32, U30, V31, W29, Y32 AA30, AB31, AC29, AD32, AE30, AG29, AH32, AJ30, AK31, AL29, AM32	Ground pins for SV _{DD}	—	—
XGND	K27, L25, M26, N24, P27, R25, T26, U24, V27, W25, Y28, AA24, AB27, AC25, AD28, AE26, AF27, AH28, AJ26, AK27, AL26, AM28	Ground pins for XV _{DD} _SRDS _n	—	—
Reset Configuration Signals²⁰				
TSEC1_TXD[0] / cfg_alt_boot_vec	AF25	—	LV _{DD}	—
TSEC1_TXD[1] / cfg_platform_freq	AC23	—	LV _{DD}	21
TSEC1_TXD[2:4] / cfg_device_id[5:7]	AG24, AG23, AE24	—	LV _{DD}	—
TSEC1_TXD[5] / cfg_tsec1_reduce	AE23	—	LV _{DD}	—
TSEC1_TXD[6:7] / cfg_tsec1_prtcl[0:1]	AE22, AD22	—	LV _{DD}	—
TSEC2_TXD[0:3] / cfg_rom_loc[0:3]	AB20, AJ23, AJ22, AD19	—	LV _{DD}	—
TSEC2_TXD[4], TSEC2_TX_ER / cfg_dram_type[0:1]	AH23, AB19	—	LV _{DD}	38
TSEC2_TXD[5] / cfg_tsec2_reduce	AH21	—	LV _{DD}	—
TSEC2_TXD[6:7] / cfg_tsec2_prtcl[0:1]	AG22, AG21	—	LV _{DD}	—
TSEC3_TXD[0:1] / cfg_spare[0:1]	AL21, AJ21	O	TV _{DD}	33
TSEC3_TXD[2] / cfg_core1_enable	AM20	O	TV _{DD}	—
TSEC3_TXD[3] / cfg_core1_lm_offset	AJ20	—	LV _{DD}	—
TSEC3_TXD[5] / cfg_tsec3_reduce	AK21	—	LV _{DD}	—

example, assuming a T_i of 30°C, a T_r of 5°C, a package $R_{\theta JC} = 0.1$, and a typical power consumption (P_d) of 43.4 W, the following expression for T_j is obtained:

$$\text{Die-junction temperature: } T_j = 30^\circ\text{C} + 5^\circ\text{C} + (0.1^\circ\text{C/W} + 0.2^\circ\text{C/W} + \theta_{sa}) \times 43.4 \text{ W}$$

For this example, a $R_{\theta sa}$ value of 1.32 °C/W or less is required to maintain the die junction temperature below the maximum value of [Table 2](#).

Though the die junction-to-ambient and the heat sink-to-ambient thermal resistances are a common figure-of-merit used for comparing the thermal performance of various microelectronic packaging technologies, one should exercise caution when only using this metric in determining thermal management because no single parameter can adequately describe three-dimensional heat flow. The final die-junction operating temperature is not only a function of the component-level thermal resistance, but the system-level design and its operating conditions. In addition to the component's power consumption, a number of factors affect the final operating die-junction temperature—airflow, board population (local heat flux of adjacent components), heat sink efficiency, heat sink placement, next-level interconnect technology, system air temperature rise, altitude, and so on.

Due to the complexity and variety of system-level boundary conditions for today's microelectronic equipment, the combined effects of the heat transfer mechanisms (radiation, convection, and conduction) may vary widely. For these reasons, we recommend using conjugate heat transfer models for the board as well as system-level designs.

For system thermal modeling, the MPC8641 thermal model is shown in [Figure 62](#). Four cuboids are used to represent this device. The die is modeled as 12.4x15.3 mm at a thickness of 0.86 mm. See [Section 3, “Power Characteristics”](#) for power dissipation details. The substrate is modeled as a single block 33x33x1.2 mm with orthotropic conductivity: 13.5 W/(m • K) in the xy-plane and 5.3 W/(m • K) in the z-direction. The die is centered on the substrate. The bump/underfill layer is modeled as a collapsed thermal resistance between the die and substrate with a conductivity of 5.3 W/(m • K) in the thickness dimension of 0.07 mm. Because the bump/underfill is modeled with zero physical dimension (collapsed height), the die thickness was slightly enlarged to provide the correct height. The C5 solder layer is modeled as a cuboid with dimensions 33x33x0.4 mm and orthotropic thermal conductivity of 0.034 W/(m • K) in the xy-plane and 9.6 W/(m • K) in the z-direction. An LGA solder layer would be modeled as a collapsed thermal resistance with thermal conductivity of 9.6 W/(m • K) and an effective height of 0.1 mm. The thermal model uses approximate dimensions to reduce grid. Please refer to the case outline for actual dimensions.

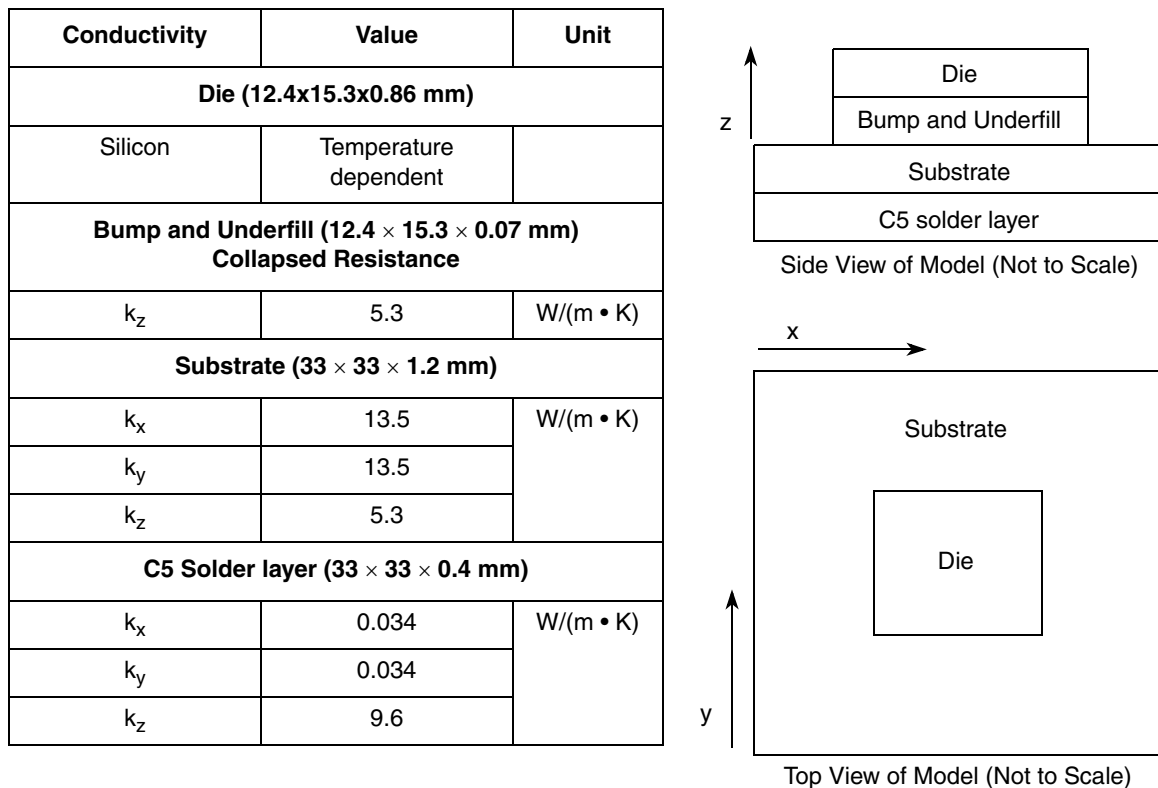


Figure 62. Recommended Thermal Model of MPC8641

19.2.4 Temperature Diode

The MPC8641 has a temperature diode on the microprocessor that can be used in conjunction with other system temperature monitoring devices (such as Analog Devices, ADT7461™). These devices use the negative temperature coefficient of a diode operated at a constant current to determine the temperature of the microprocessor and its environment. It is recommended that each device be individually calibrated.

The following are the specifications of the MPC8641 on-board temperature diode:

$$V_f > 0.40 \text{ V}$$

$$V_f < 0.90 \text{ V}$$

An approximate value of the ideality may be obtained by calibrating the device near the expected operating temperature.

Ideality factor is defined as the deviation from the ideal diode equation:

$$I_{fw} = I_s \left[e^{\frac{qV_f}{nKT}} - 1 \right]$$

For other pin pull-up or pull-down recommendations of signals, please see [Section 17, “Signal Listings.”](#)

20.7 Output Buffer DC Impedance

The MPC8641 drivers are characterized over process, voltage, and temperature. For all buses, the driver is a push-pull single-ended driver type (open drain for I²C).

To measure Z_0 for the single-ended drivers, an external resistor is connected from the chip pad to OV_{DD} or GND. Then, the value of each resistor is varied until the pad voltage is $OV_{DD}/2$ (see [Figure 66](#)). The output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held high, SW1 is closed (SW2 is open) and R_P is trimmed until the voltage at the pad equals $OV_{DD}/2$. R_P then becomes the resistance of the pull-up devices. R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N)/2$.

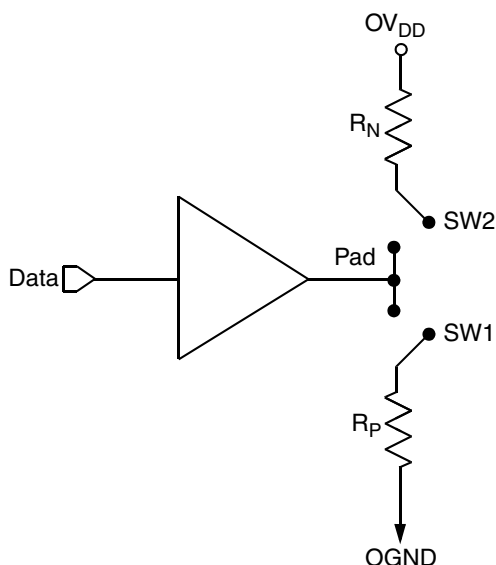


Figure 66. Driver Impedance Measurement

[Table 73](#) summarizes the signal impedance targets. The driver impedances are targeted at minimum V_{DD} , nominal OV_{DD} , 105°C.

Table 73. Impedance Characteristics

Impedance	DUART, Control, Configuration, Power Management	PCI Express	DDR DRAM	Symbol	Unit
R_N	43 Target	25 Target	20 Target	Z_0	W
R_P	43 Target	25 Target	20 Target	Z_0	W

Note: Nominal supply voltages. See [Table 1](#), $T_j = 105^\circ\text{C}$.

20.8 Configuration Pin Muxing

The MPC8641 provides the user with power-on configuration options which can be set through the use of external pull-up or pull-down resistors of 4.7 k Ω on certain output pins (see customer visible configuration pins). These pins are generally used as output only pins in normal operation.

While $\overline{\text{HRESET}}$ is asserted however, these pins are treated as inputs. The value presented on these pins while $\overline{\text{HRESET}}$ is asserted, is latched when $\overline{\text{HRESET}}$ deasserts, at which time the input receiver is disabled and the I/O circuit takes on its normal function. Most of these sampled configuration pins are equipped with an on-chip gated resistor of approximately 20 k Ω . This value should permit the 4.7-k Ω resistor to pull the configuration pin to a valid logic low level. The pull-up resistor is enabled only during $\overline{\text{HRESET}}$ (and for platform /system clocks after $\overline{\text{HRESET}}$ deassertion to ensure capture of the reset value). When the input receiver is disabled the pull-up is also, thus allowing functional operation of the pin as an output with minimal signal quality or delay disruption. The default value for all configuration bits treated this way has been encoded such that a high voltage level puts the device into the default state and external resistors are needed only when non-default settings are required by the user.

Careful board layout with stubless connections to these pull-down resistors coupled with the large value of the pull-down resistor should minimize the disruption of signal quality or speed for output pins thus configured.

The platform PLL ratio and e600 PLL ratio configuration pins are not equipped with these default pull-up devices.

20.9 JTAG Configuration Signals

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in [Figure 68](#). Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions as most have asynchronous behavior and spurious assertion will give unpredictable results.

Boundary-scan testing is enabled through the JTAG interface signals. The $\overline{\text{TRST}}$ signal is optional in the IEEE 1149.1 specification, but is provided on all processors that implement the Power Architecture technology. The device requires $\overline{\text{TRST}}$ to be asserted during reset conditions to ensure the JTAG boundary logic does not interfere with normal chip operation. While it is possible to force the TAP controller to the reset state using only the TCK and TMS signals, more reliable power-on reset performance will be obtained if the $\overline{\text{TRST}}$ signal is asserted during power-on reset. Because the JTAG interface is also used for accessing the common on-chip processor (COP) function, simply tying $\overline{\text{TRST}}$ to $\overline{\text{HRESET}}$ is not practical.

The COP function of these processors allows a remote computer system (typically a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP port connects primarily through the JTAG interface of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$ in order to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.

The arrangement shown in [Figure 67](#) allows the COP port to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$, while ensuring that the target can drive $\overline{\text{HRESET}}$ as well.

21 Ordering Information

Ordering information for the parts fully covered by this specification document is provided in [Section 21.1, “Part Numbers Fully Addressed by This Document.”](#)

21.1 Part Numbers Fully Addressed by This Document

[Table 74](#) provides the Freescale part numbering nomenclature for the MPC8641. Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Freescale sales office. In addition to the processor frequency, the part numbering scheme also includes an application modifier which may specify special application conditions. Each part number also contains a revision code which refers to the die mask revision number.

Table 74. Part Numbering Nomenclature

MC	nnnn	x	xx	nnnn	x	x
Product Code	Part Identifier	Core Count	Package ¹	Core Processor Frequency ² (MHz)	DDR speed (MHz)	Product Revision Level
MC	8641	Blank = Single Core D = Dual Core	HX = High-lead HCTE FC-CBGA VU = RoHS lead-free HCTE FC-CBGA ⁵ VJ = lead-free HCTE FC-CBGA ⁶	1000, 1250, 1333, 1500	N = 500 MHz ⁴ K = 600 MHz J = 533 MHz H = 500 MHz G = 400 MHz	Revision B = 2.0 System Version Register Value for Rev B: 0x8090_0020 - MPC8641 0x8090_0120 - MPC8641D Revision C = 2.1 System Version Register Value for Rev C: 0x8090_0021 - MPC8641 0x8090_0121 - MPC8641D Revision E = 3.0 System Version Register Value for Rev E: 0x8090_0030 - MPC8641 0x8090_0130 - MPC8641D

Notes:

1. See [Section 16, “Package,”](#) for more information on available package types.
2. Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by part number specifications may support other maximum core frequencies.
3. The P prefix in a Freescale part number designates a “Pilot Production Prototype” as defined by Freescale SOP 3-13. These parts have only preliminary reliability and characterization data. Before pilot production prototypes may be shipped, written authorization from the customer must be on file in the applicable sales office acknowledging the qualification status and the fact that product changes may still occur while shipping pilot production prototypes.
4. Part Number MC8641xxx1000NX is our low V_{DD_Coren} device. $V_{DD_Coren} = 0.95\text{ V}$ and $V_{DD_PLAT} = 1.05\text{ V}$.
5. VU part number is RoHS compliant with the permitted exception of the C4 die bumps.
6. VJ part number is entirely lead-free including the C4 die bumps.