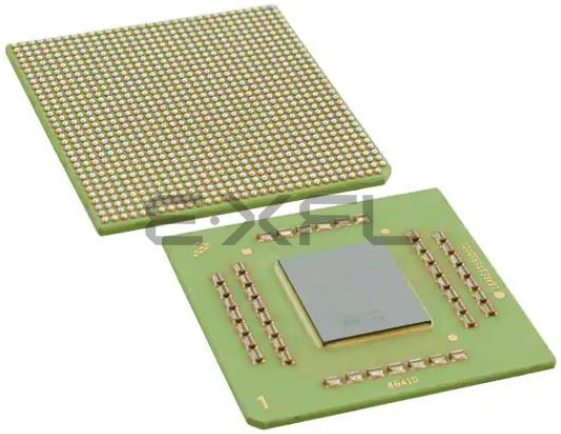

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## Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | PowerPC e600 |
| Number of Cores/Bus Width | 2 Core, 32-Bit |
| Speed | 1.25GHz |
| Co-Processors/DSP | - |
| RAM Controllers | DDR, DDR2 |
| Graphics Acceleration | No |
| Display & Interface Controllers | - |
| Ethernet | 10/100/1000Mbps (4) |
| SATA | - |
| USB | - |
| Voltage - I/O | 1.8V, 2.5V, 3.3V |
| Operating Temperature | 0°C ~ 105°C (TA) |
| Security Features | - |
| Package / Case | 1023-BBGA, FCBGA |
| Supplier Device Package | 1023-FCCBGA (33x33) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/mc8641dhx1250hb |

**Table 2. Recommended Operating Conditions (continued)**

| Characteristic | | Symbol | Recommended Value | Unit | Notes |
|---|---|---|---|---|---|
| SerDes Serial I/O Supply Port 1 | | $XV_{DD}$_SRDS1 | 1.10 ± 50 mV | V | 8 |
| | | | 1.05 ± 50 mV | | 7 |
| SerDes Serial I/O Supply Port 2 | | $XV_{DD}$_SRDS2 | 1.10 ± 50 mV | V | 8 |
| | | | 1.05 ± 50 mV | | 7 |
| SerDes DLL and PLL supply voltage for Port 1 and Port 2 | | $AV_{DD}$_SRDS1, $AV_{DD}$_SRDS2 | 1.10 ± 50 mV | V | 8 |
| | | | 1.05 ± 50 mV | | 7 |
| Platform Supply voltage | | $V_{DD}$_PLAT | 1.10 ± 50 mV | V | 8 |
| | | | 1.05 ± 50 mV | | 7 |
| Local Bus and Platform PLL supply voltage | | $AV_{DD}$_LB, $AV_{DD}$_PLAT | 1.10 ± 50 mV | V | 8 |
| | | | 1.05 ± 50 mV | | 7 |
| DDR and DDR2 SDRAM I/O supply voltages | | D1_$GV_{DD}$, D2_$GV_{DD}$ | 2.5 V ± 125 mV | V | 9 |
| | | | 1.8 V ± 90 mV | V | 9 |
| eTSEC 1 and 2 I/O supply voltage | | $LV_{DD}$ | 3.3 V ± 165 mV | V | 10 |
| | | | 2.5 V ± 125 mV | V | 10 |
| eTSEC 3 and 4 I/O supply voltage | | $TV_{DD}$ | 3.3 V ± 165 mV | V | 10 |
| | | | 2.5 V ± 125 mV | V | 10 |
| Local Bus, DUART, DMA, Multiprocessor Interrupts, System Control & Clocking, Debug, Test, Power management, $I^2C$, JTAG and Miscellaneous I/O voltage | | $OV_{DD}$ | 3.3 V ± 165 mV | V | 5 |
| Input voltage | DDR and DDR2 SDRAM signals | D*n*_$MV_{IN}$ | GND to D*n*_$GV_{DD}$ | V | 3, 6 |
| | DDR and DDR2 SDRAM reference | D*n*_$MV_{REF}$ | D*n*_$GV_{DD}$/2 ± 1% | V | |
| | Three-speed Ethernet signals | $LV_{IN}$ $TV_{IN}$ | GND to $LV_{DD}$ GND to $TV_{DD}$ | V | 4, 6 |
| | DUART, Local Bus, DMA, Multiprocessor Interrupts, System Control & Clocking, Debug, Test, Power management, $I^2C$, JTAG and Miscellaneous I/O voltage | $OV_{IN}$ | GND to $OV_{DD}$ | V | 5,6 |

# 5 RESET Initialization

This section describes the AC electrical specifications for the RESET initialization timing requirements of the MPC8641. Table 11 provides the RESET initialization AC timing specifications.

**Table 11. RESET Initialization Timing Specifications**

| Parameter/Condition | Min | Max | Unit | Notes |
|---|---|---|---|---|
| Required assertion time of $\overline{\text{HRESET}}$ | 100 | — | μs | — |
| Minimum assertion time for $\overline{\text{SRESET\_0}}$ & $\overline{\text{SRESET\_1}}$ | 3 | — | SYSCLKs | 1 |
| Platform PLL input setup time with stable SYSCLK before $\overline{\text{HRESET}}$ negation | 100 | — | μs | 2 |
| Input setup time for POR configs (other than PLL config) with respect to negation of $\overline{\text{HRESET}}$ | 4 | — | SYSCLKs | 1 |
| Input hold time for all POR configs (including PLL config) with respect to negation of $\overline{\text{HRESET}}$ | 2 | — | SYSCLKs | 1 |
| Maximum valid-to-high impedance time for actively driven POR configs with respect to negation of $\overline{\text{HRESET}}$ | — | 5 | SYSCLKs | 1 |

**Notes:**
1. SYSCLK is the primary clock input for the MPC8641.
2 This is related to $\overline{\text{HRESET}}$ assertion time. Stable PLL configuration inputs are required when a stable SYSCLK is applied. See the *MPC8641D Integrated Host Processor Reference Manual* for more details on the power-on reset sequence.

Table 12 provides the PLL lock times.

**Table 12. PLL Lock Times**

| Parameter/Condition | Min | Max | Unit | Notes |
|---|---|---|---|---|
| (Platform and E600) PLL lock times | — | 100 | μs | 1 |
| Local bus PLL | — | 50 | μs | — |

**Note:**
1.The PLL lock time for e600 PLLs require an additional 255 MPX_CLK cycles.

**Table 21. DDR SDRAM Output AC Timing Specifications (continued)**

At recommended operating conditions.

| Parameter | Symbol [1] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| MDQS epilogue end | $t_{DDKHME}$ | –0.6 | 0.6 | ns | 6 |

**Note:**

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, $t_{DDKHAS}$ symbolizes DDR timing (DD) for the time $t_{MCK}$ memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, $t_{DDKLDX}$ symbolizes DDR timing (DD) for the time $t_{MCK}$ memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/$\overline{\text{MCK}}$ referenced measurements are made from the crossing of the two signals ±0.1 V.
3. ADDR/CMD includes all DDR SDRAM output signals except MCK/$\overline{\text{MCK}}$, $\overline{\text{MCS}}$, and MDQ/MECC/MDM/MDQS.
4. Note that $t_{DDKHMH}$ follows the symbol conventions described in note 1. For example, $t_{DDKHMH}$ describes the DDR timing (DD) from the rising edge of the MCK[n] clock (KH) until the MDQS signal is valid (MH). $t_{DDKHMH}$ can be modified through control of the DQS override bits (called WR_DATA_DELAY) in the TIMING_CFG_2 register. This will typically be set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these 2 parameters have been set to the same adjustment value. See the *MPC8641 Integrated Processor Reference Manual* for a description and understanding of the timing modifications enabled by use of these bits.
5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the microprocessor.
6. All outputs are referenced to the rising edge of MCK[n] at the pins of the microprocessor. Note that $t_{DDKHMP}$ follows the symbol conventions described in note 1.
7. Maximum DDR1 frequency is 400 MHz
8. Per the JEDEC spec the DDR2 duty cycle at 600 MHz is the average low and high cycle time values that are defined as the average pulse widths calculated across any consecutive 200 pulses. Jitter can sometimes force single low and high cycle times to drift from the average values. $t_{JIT}$ = ±125 ps.
9. Per the JEDEC spec the DDR2 duty cycle at 400 and 533 MHz is the low and high cycle time values.

## NOTE

For the ADDR/CMD setup and hold specifications in Table 21, it is assumed that the Clock Control register is set to adjust the memory clocks by 1/2 applied cycle.

Figure 5 shows the DDR SDRAM output timing for the MCK to MDQS skew measurement (tDDKHMH).

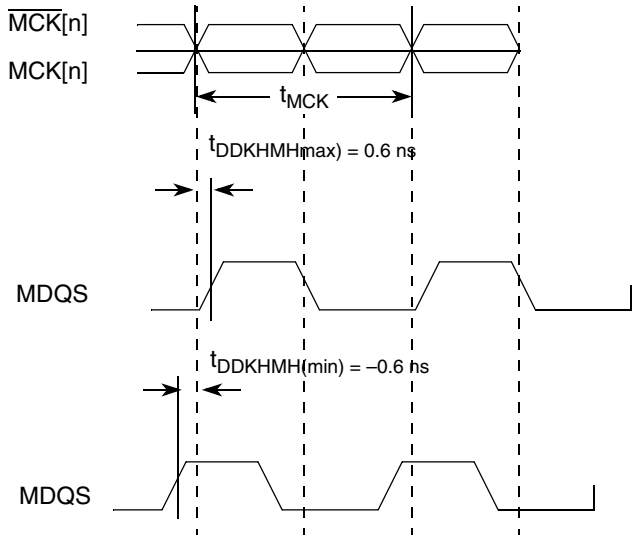



**Figure 5. Timing Diagram for tDDKHMH**

Figure 6 shows the DDR SDRAM output timing diagram.

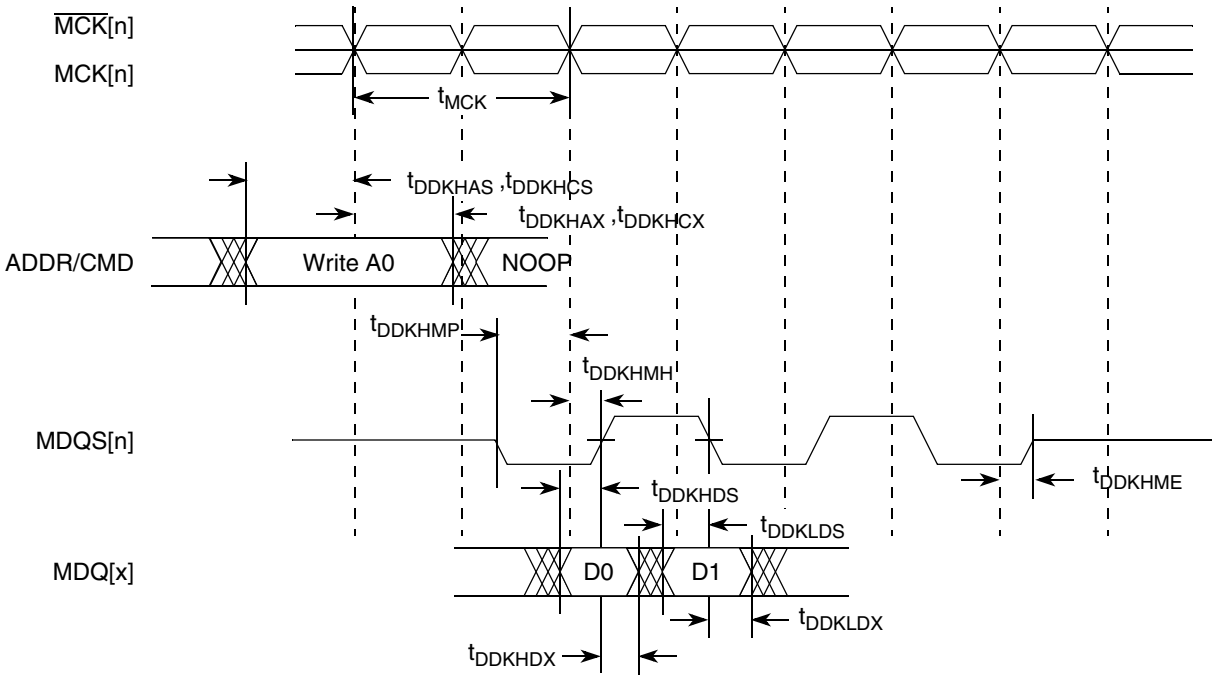



**Figure 6. DDR SDRAM Output Timing Diagram**

clock to synchronously generate transmit data and outputs an echoed copy of the transmit clock back out onto the TSEC*n*_GTX_CLK pin (while transmit data appears on TSEC*n*_TXD[7:0], for example). It is intended that external receivers capture eTSEC transmit data using the clock on TSEC*n*_GTX_CLK as a source-synchronous timing reference. Typically, the clock edge that launched the data can be used, since the clock is delayed by the eTSEC to allow acceptable set-up margin at the receiver. Note that there is relationship between the maximum FIFO speed and the platform speed. For more information see Section 18.4.2, "Platform to FIFO Restrictions."

**NOTE**

The phase between the output clocks TSEC1_GTX_CLK and TSEC2_GTX_CLK (ports 1 and 2) is no more than 100 ps. The phase between the output clocks TSEC3_GTX_CLK and TSEC4_GTX_CLK (ports 3 and 4) is no more than 100 ps.

A summary of the FIFO AC specifications appears in Table 26 and Table 27.

**Table 26. FIFO Mode Transmit AC Timing Specification**

At recommended operating conditions with $L/TV_{DD}$ of 3.3 V ± 5% and 2.5 V ± 5%.

| Parameter/Condition | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| TX_CLK, GTX_CLK clock period (GMII mode) | $t_{FIT}$ | 7.0 | 8.0 | 100 | ns |
| TX_CLK, GTX_CLK clock period (Encoded mode) | $t_{FIT}$ | 5.3 | 8.0 | 100 | ns |
| TX_CLK, GTX_CLK duty cycle | $t_{FITH}/t_{FIT}$ | 45 | 50 | 55 | % |
| TX_CLK, GTX_CLK peak-to-peak jitter | $t_{FITJ}$ | — | — | 250 | ps |
| Rise time TX_CLK (20%–80%) | $t_{FITR}$ | — | — | 0.75 | ns |
| Fall time TX_CLK (80%–20%) | $t_{FITF}$ | — | — | 0.75 | ns |
| FIFO data TXD[7:0], TX_ER, TX_EN setup time to GTX_CLK | $t_{FITDV}$ | 2.0 | — | — | ns |
| GTX_CLK to FIFO data TXD[7:0], TX_ER, TX_EN hold time | $t_{FITDX}$ | 0.5 | — | 3.0 | ns |

**Table 27. FIFO Mode Receive AC Timing Specification**

At recommended operating conditions with $L/TV_{DD}$ of 3.3 V ± 5% and 2.5 V ± 5%.

| Parameter/Condition | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| RX_CLK clock period (GMII mode) | $t_{FIR}$[1] | 7.0 | 8.0 | 100 | ns |
| RX_CLK clock period (Encoded mode) | $t_{FIR}$[1] | 5.3 | 8.0 | 100 | ns |
| RX_CLK duty cycle | $t_{FIRH}/t_{FIR}$ | 45 | 50 | 55 | % |
| RX_CLK peak-to-peak jitter | $t_{FIRJ}$ | — | — | 250 | ps |
| Rise time RX_CLK (20%–80%) | $t_{FIRR}$ | — | — | 0.75 | ns |
| Fall time RX_CLK (80%–20%) | $t_{FIRF}$ | — | — | 0.75 | ns |
| RXD[7:0], RX_DV, RX_ER setup time to RX_CLK | $t_{FIRDV}$ | 1.5 | — | — | ns |
| RXD[7:0], RX_DV, RX_ER hold time to RX_CLK | $t_{FIRDX}$ | 0.5 | — | — | ns |

[1] ±100 ppm tolerance on RX_CLK frequency

# 9 Ethernet Management Interface Electrical Characteristics

The electrical characteristics specified here apply to MII management interface signals MDIO (management data input/output) and MDC (management data clock). The electrical characteristics for GMII, RGMII, RMII, TBI and RTBI are specified in "Section 8, "Ethernet: Enhanced Three-Speed Ethernet (eTSEC), MII Management."

## 9.1 MII Management DC Electrical Characteristics

The MDC and MDIO are defined to operate at a supply voltage of 3.3 V. The DC electrical characteristics for MDIO and MDC are provided in Table 38.

**Table 38. MII Management DC Electrical Characteristics**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Supply voltage (3.3 V) | $OV_{DD}$ | 3.135 | 3.465 | V |
| Output high voltage ($OV_{DD}$ = Min, $I_{OH}$ = –1.0 mA) | $V_{OH}$ | 2.10 | — | V |
| Output low voltage ($OV_{DD}$ =Min, $I_{OL}$ = 1.0 mA) | $V_{OL}$ | — | 0.50 | V |
| Input high voltage | $V_{IH}$ | 1.70 | — | V |
| Input low voltage | $V_{IL}$ | — | 0.90 | V |
| Input high current ($OV_{DD}$ = Max, $V_{IN}$ [1] = 2.1 V) | $I_{IH}$ | — | 40 | μA |
| Input low current ($OV_{DD}$ = Max, $V_{IN}$ = 0.5 V) | $I_{IL}$ | –600 | — | μA |

**Note:**
1. Note that the symbol $V_{IN}$, in this case, represents the $OV_{IN}$ symbol referenced in Table 1 and Table 2.

## 9.2 MII Management AC Electrical Specifications

Table 39 provides the MII management AC timing specifications.

**Table 39. MII Management AC Timing Specifications**

At recommended operating conditions with $OV_{DD}$ is 3.3 V ± 5%.

| Parameter/Condition | Symbol [1] | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| MDC frequency | $f_{MDC}$ | 2.5 | — | 9.3 | MHz | 2, 4 |
| MDC period | $t_{MDC}$ | 80 | — | 400 | ns | — |
| MDC clock pulse width high | $t_{MDCH}$ | 32 | — | — | ns | — |
| MDC to MDIO valid | $t_{MDKHDV}$ | $16*t_{MPXCLK}$ | — | — | ns | 5 |
| MDC to MDIO delay | $t_{MDKHDX}$ | 10 | — | $16*t_{MPXCLK}$ | ns | 3, 5 |
| MDIO to MDC setup time | $t_{MDDVKH}$ | 5 | — | — | ns | — |

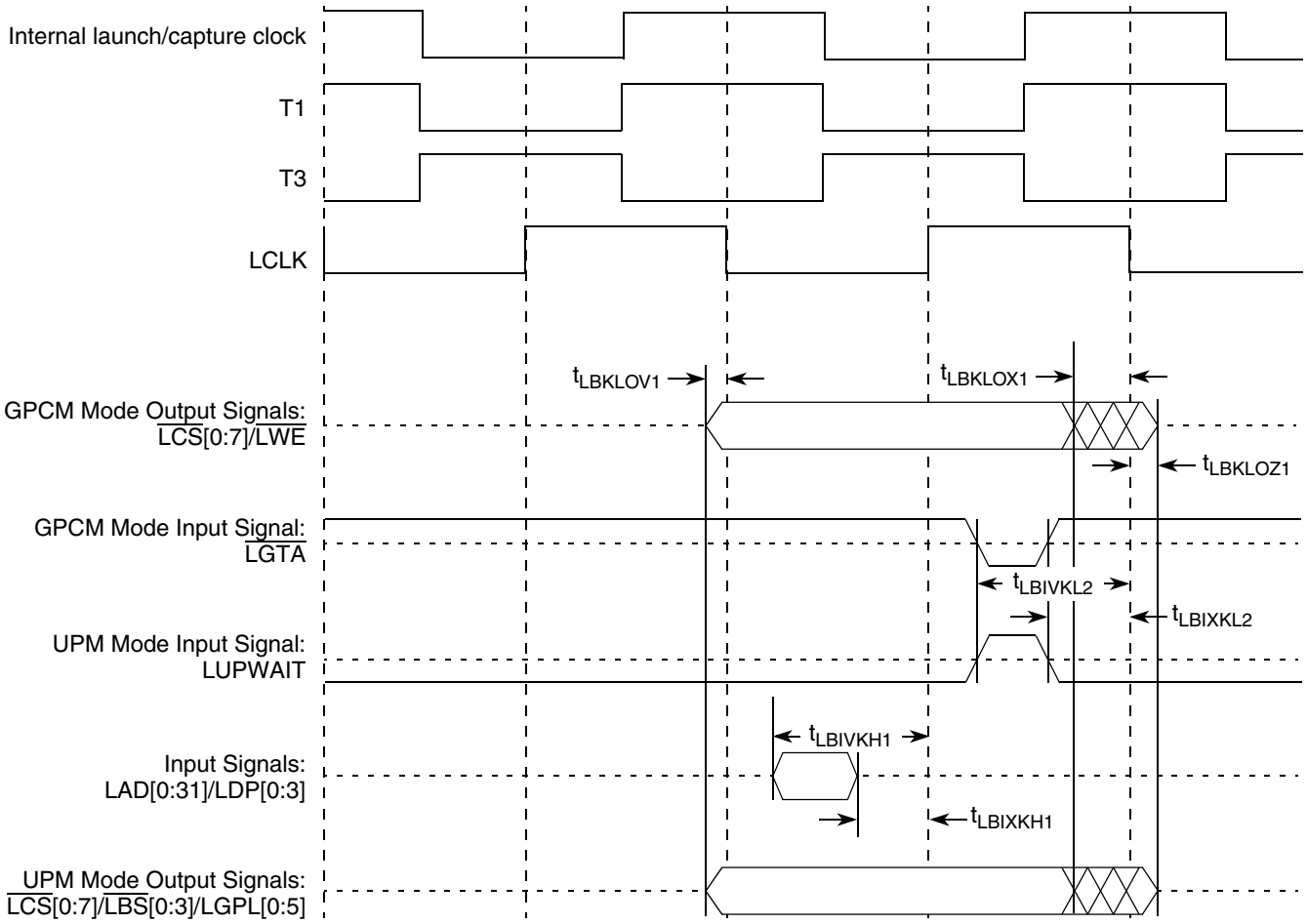



**Figure 29. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 2 (clock ratio of 4) (PLL Bypass Mode)**

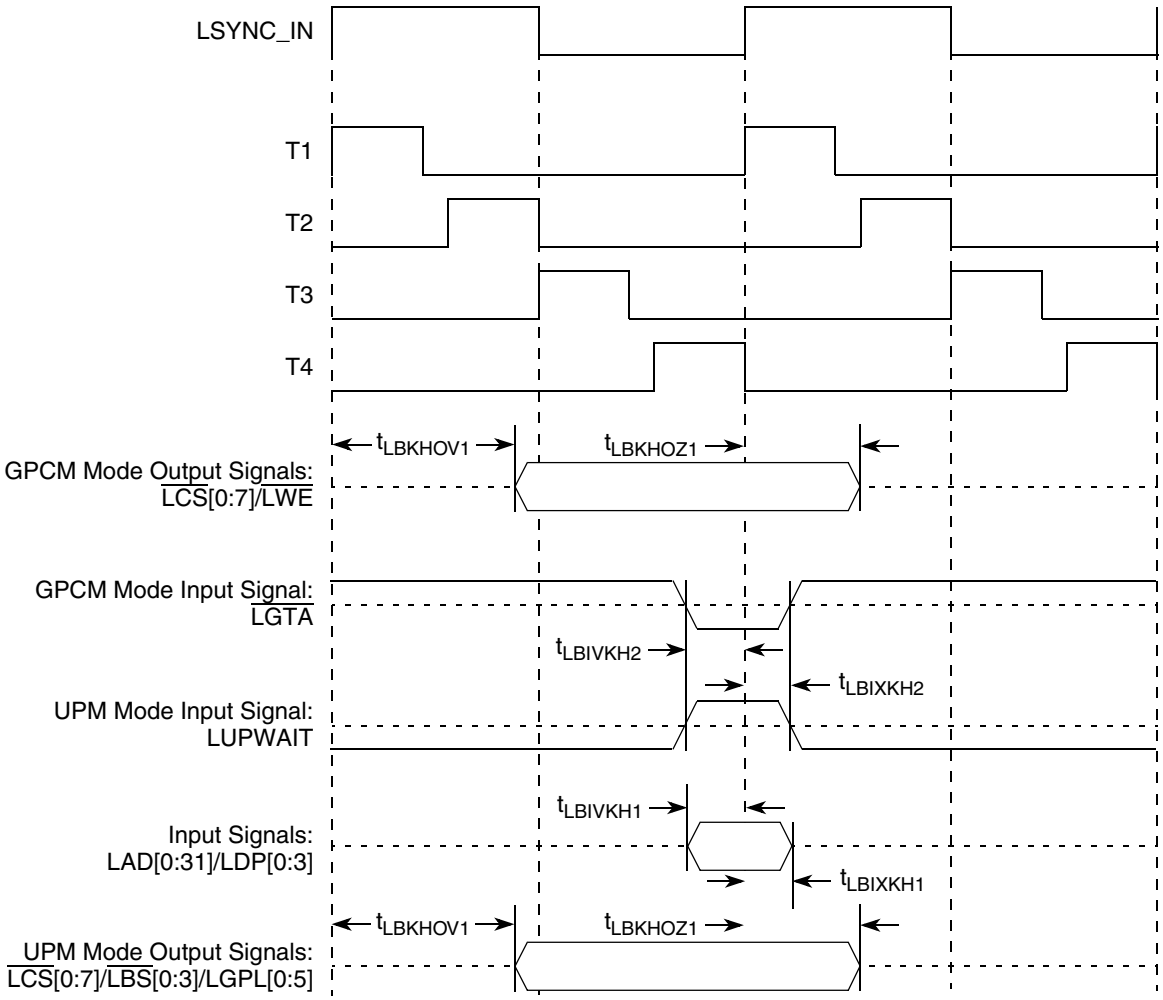



**Figure 30. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 4 or 8 (clock ratio of 8 or 16) (PLL Enabled)**

### 13.2.3 Interfacing With Other Differential Signaling Levels

With on-chip termination to SGND, the differential reference clocks inputs are HCSL (High-Speed Current Steering Logic) compatible DC-coupled.

Many other low voltage differential type outputs like LVDS (Low Voltage Differential Signaling) can be used but may need to be AC-coupled due to the limited common mode input range allowed (100 to 400 mV) for DC-coupled connection.

LVPECL outputs can produce signal with too large amplitude and may need to be DC-biased at clock driver output first, then followed with series attenuation resistor to reduce the amplitude, in addition to AC-coupling.

**NOTE**

Figure 43 to Figure 46 below are for conceptual reference only. Due to the fact that clock driver chip's internal structure, output impedance and termination requirements are different between various clock driver chip manufacturers, it is very possible that the clock circuit reference designs provided by clock driver chip vendor are different from what is shown below. They might also vary from one vendor to the other. Therefore, Freescale Semiconductor can neither provide the optimal clock driver reference circuits, nor guarantee the correctness of the following clock driver connection reference circuits. The system designer is recommended to contact the selected clock driver chip vendor for the optimal reference circuits with the MPC8641D SerDes reference clock receiver requirement provided in this document.

Figure 46 shows the SerDes reference clock connection reference circuits for a single-ended clock driver. It assumes the DC levels of the clock driver are compatible with MPC8641D SerDes reference clock input's DC requirement.

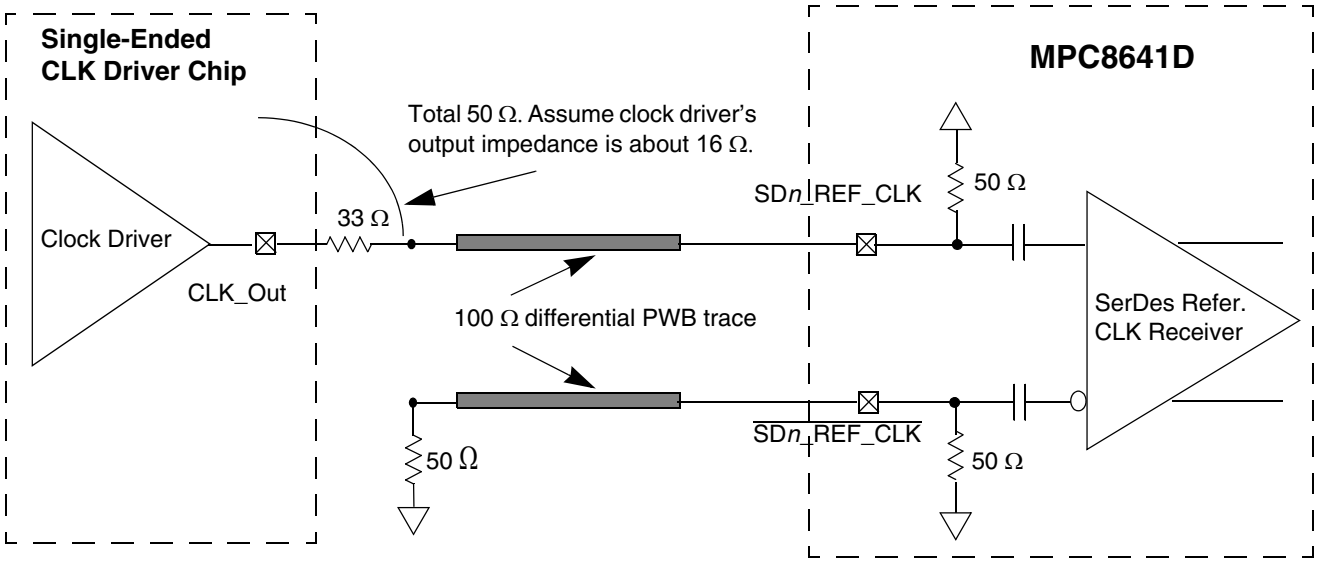



**Figure 46. Single-Ended Connection (Reference Only)**

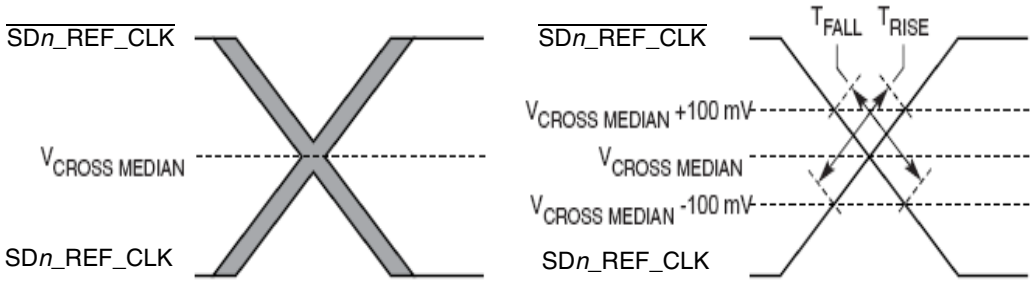



**Figure 48. Single-Ended Measurement Points for Rise and Fall Time Matching**

The other detailed AC requirements of the SerDes Reference Clocks is defined by each interface protocol based on application usage. Refer to the following sections for detailed information:

- Section 14.2, "AC Requirements for PCI Express SerDes Clocks"
- Section 15.2, "AC Requirements for Serial RapidIO SDn_REF_CLK and SDn_REF_CLK"

## 13.3 SerDes Transmitter and Receiver Reference Circuits

Figure 49 shows the reference circuits for SerDes data lane's transmitter and receiver.

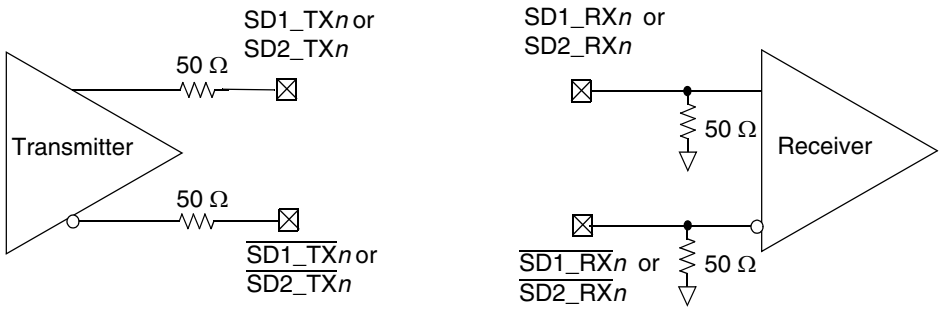



**Figure 49. SerDes Transmitter and Receiver Reference Circuits**

The DC and AC specification of SerDes data lanes are defined in each interface protocol section below (PCI Express or Serial Rapid IO) in this document based on the application usage:"

- Section 14, "PCI Express"
- Section 15, "Serial RapidIO"

Note that external AC Coupling capacitor is required for the above two serial transmission protocols with the capacitor value defined in specification of each protocol section.

# 14 PCI Express

This section describes the DC and AC electrical specifications for the PCI Express bus of the MPC8641.

### 14.4.2 Transmitter Compliance Eye Diagrams

The TX eye diagram in Figure 50 is specified using the passive compliance/test measurement load (see Figure 52) in place of any real PCI Express interconnect + RX component.

There are two eye diagrams that must be met for the transmitter. Both eye diagrams must be aligned in time using the jitter median to locate the center of the eye diagram. The different eye diagrams will differ in voltage depending whether it is a transition bit or a de-emphasized bit. The exact reduced voltage level of the de-emphasized bit will always be relative to the transition bit.

The eye diagram must be valid for any 250 consecutive UIs.

A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.

**NOTE**

It is recommended that the recovered TX UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function (that is, least squares and median deviation fits).

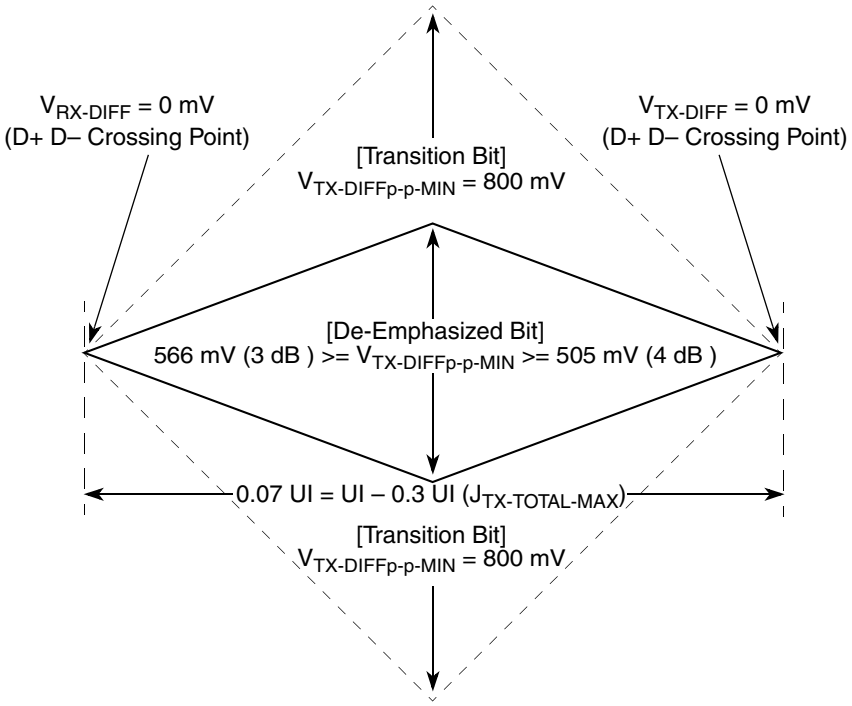



**Figure 50. Minimum Transmitter Timing and Voltage Output Compliance Specifications**

**Table 50. Differential Receiver (RX) Input Specifications (continued)**

| Symbol | Parameter | Min | Nom | Max | Units | Comments |
|---|---|---|---|---|---|---|
| $T_{RX-IDLE-DET-DIFF-ENTERTIME}$ | Unexpected Electrical Idle Enter Detect Threshold Integration Time | — | — | 10 | ms | An unexpected Electrical Idle ($V_{RX-DIFFp-p} < V_{RX-IDLE-DET-DIFFp-p}$) must be recognized no longer than $T_{RX-IDLE-DET-DIFF-ENTERING}$ to signal an unexpected idle condition. |
| $L_{TX-SKEW}$ | Total Skew | — | — | 20 | ns | Skew across all lanes on a Link. This includes variation in the length of SKP ordered set (for example, COM and one to five Symbols) at the RX as well as any delay differences arising from the interconnect itself. |

**Notes:**
1. No test load is necessarily associated with this value.
2. Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 52 should be used as the RX device when taking measurements (also refer to the Receiver compliance eye diagram shown in Figure 51). If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.
3. A $T_{RX-EYE}$ = 0.40 UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the Transmitter and interconnect collected any 250 consecutive UIs. The $T_{RX-EYE-MEDIAN-to-MAX-JITTER}$ specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total. UI jitter budget collected over any 250 consecutive TX UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as the reference for the eye diagram.
4. The Receiver input impedance shall result in a differential return loss greater than or equal to 15 dB with the D+ line biased to 300 mV and the D- line biased to -300 mV and a common mode return loss greater than or equal to 6 dB (no bias required) over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements for is 50 Ω to ground for both the D+ and D- line (that is, as measured by a Vector Network Analyzer with 50 ohm probes - see Figure 52). Note: that the series capacitors $C_{TX}$ is optional for the return loss measurement.
5. Impedance during all LTSSM states. When transitioning from a Fundamental Reset to Detect (the initial state of the LTSSM) there is a 5 ms transition time before Receiver termination values must be met on all un-configured Lanes of a Port.
6. The RX DC Common Mode Impedance that exists when no power is present or Fundamental Reset is asserted. This helps ensure that the Receiver Detect circuit will not falsely assume a Receiver is powered on when it is not. This term must be measured at 300 mV above the RX ground.
7. It is recommended that the recovered TX UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function. Least squares and median deviation fits have worked well with experimental and simulated data.

## 14.5 Receiver Compliance Eye Diagrams

The RX eye diagram in Figure 51 is specified using the passive compliance/test measurement load (see Figure 52) in place of any real PCI Express RX component.

Note: In general, the minimum Receiver eye diagram measured with the compliance/test measurement load (see Figure 52) will be larger than the minimum Receiver eye diagram measured over a range of systems at the input Receiver of any real PCI Express component. The degraded eye diagram at the input Receiver is due to traces internal to the package as well as silicon parasitic characteristics which cause the real PCI Express component to vary in impedance from the compliance/test measurement load. The input Receiver eye diagram is implementation specific and is not specified. RX component designer should

**Table 57. Long Run Transmitter AC Timing Specifications—3.125 GBaud**

| Characteristic | Symbol | Range | | Unit | Notes |
|---|---|---|---|---|---|
| | | Min | Max | | |
| Output Voltage, | $V_O$ | –0.40 | 2.30 | Volts | Voltage relative to COMMON of either signal comprising a differential pair |
| Differential Output Voltage | $V_{DIFFPP}$ | 800 | 1600 | mV p-p | — |
| Deterministic Jitter | $J_D$ | — | 0.17 | UI p-p | — |
| Total Jitter | $J_T$ | — | 0.35 | UI p-p | — |
| Multiple output skew | $S_{MO}$ | — | 1000 | ps | Skew at the transmitter output between lanes of a multilane link |
| Unit Interval | UI | 320 | 320 | ps | +/– 100 ppm |

For each baud rate at which an LP-Serial transmitter is specified to operate, the output eye pattern of the transmitter shall fall entirely within the unshaded portion of the Transmitter Output Compliance Mask shown in Figure 54 with the parameters specified in Table 58 when measured at the output pins of the device and the device is driving a 100 Ω +/–5% differential resistive load. The output eye pattern of an LP-Serial transmitter that implements pre-emphasis (to equalize the link and reduce inter-symbol interference) need only comply with the Transmitter Output Compliance Mask when pre-emphasis is disabled or minimized.

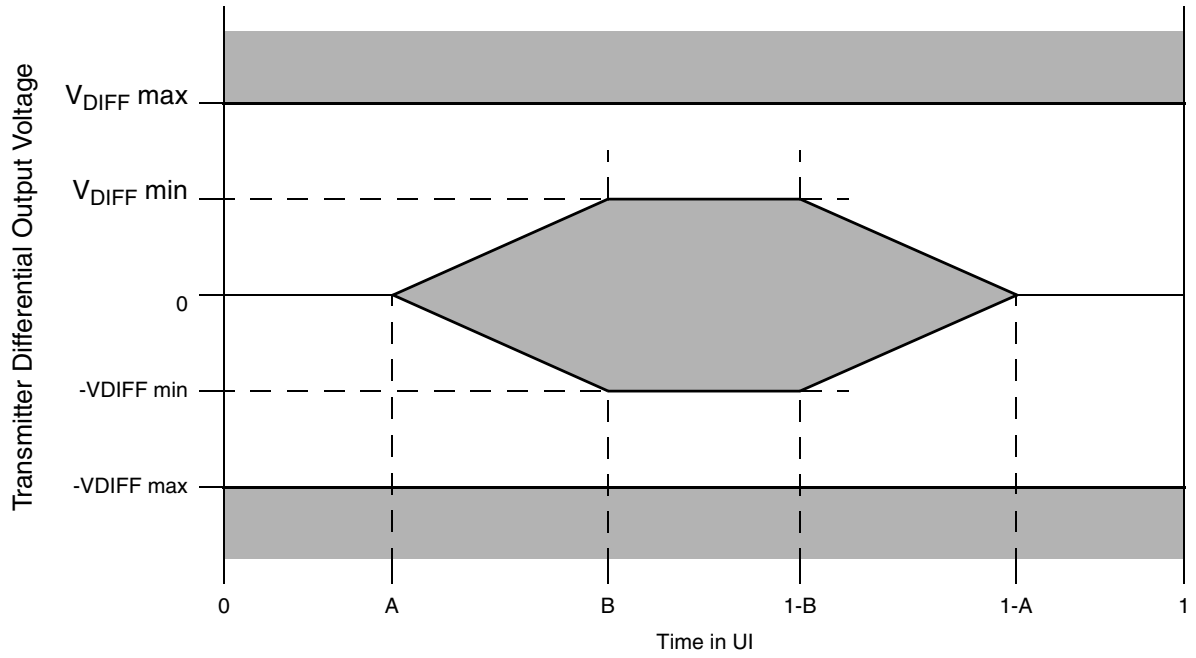



**Figure 54. Transmitter Output Compliance Mask**

# 16 Package

This section details package parameters and dimensions.

## 16.1 Package Parameters for the MPC8641

The package parameters are as provided in the following list. The package type is 33 mm × 33 mm, 1023 pins. There are two package options: high-lead Flip Chip-Ceramic Ball Grid Array (FC-CBGA), and lead-free (FC-CBGA).

For all package types:

| | |
|---|---|
| Die size | 12.1 mm × 14.7 mm |
| Package outline | 33 mm × 33 mm |
| Interconnects | 1023 |
| Pitch | 1 mm |
| Total Capacitor count | 43 caps; 100 nF each |

For high-lead FC-CBGA (package option: HCTE[1] HX)

| | |
|---|---|
| Maximum module height | 2.97 mm |
| Minimum module height | 2.47 mm |
| Solder Balls | 89.5% Pb 10.5% Sn |
| Ball diameter (typical[2]) | 0.60 mm |

For RoHS lead-free FC-CBGA (package option: HCTE[1] VU) and lead-free FC-CBGA (package option: HCTE[1] VJ)

| | |
|---|---|
| Maximum module height | 2.77 mm |
| Minimum module height | 2.27 mm |
| Solder Balls | 95.5% Sn 4.0% Ag 0.5% Cu |
| Ball diameter (typical[2]) | 0.60 mm |

[1] High-coefficient of thermal expansion

[2] Typical ball diameter is before reflow

**Table 63. MPC8641 Signal Reference by Functional Block (continued)**

| Name[1] | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|
| $XV_{DD}$_SRDS2 | AA25, AB28, AC26, AD27, AE25, AF28, AH27, AK28, AM27, W24, Y27 | Serial I/O Power Supply for SerDes Port 2 | $XV_{DD}$_SRDS2 1.05/1.1 V | — |
| $V_{DD}$_Core0 | L12, L13, L14, M13, M15, N12, N14, P11, P13, P15, R12, R14, T11, T13, T15, U12, U14, V11, V13, V15, W12, W14, Y12, Y13, Y15, AA12, AA14, AB13 | Core 0 voltage supply | $V_{DD}$_Core0 0.95/1.05/1.1 V | — |
| $V_{DD}$_Core1 | R16, R18, R20, T17, T19, T21, T23, U16, U18, U22, V17, V19, V21, V23, W16, W18, W20, W22, Y17, Y19, Y21, Y23, AA16, AA18, AA20, AA22, AB23, AC24 | Core 1 voltage supply | $V_{DD}$_Core1 0.95/1.05/1.1 V | 12, *S1* |
| $V_{DD}$_PLAT | M16, M17, M18, N16, N20, N22, P17, P19, P21, P23, R22 | Platform supply voltage | $V_{DD}$_PLAT 1.05/1.1 V | — |
| $AV_{DD}$_Core0 | B20 | Core 0 PLL Supply | $AV_{DD}$_Core0 0.95/1.05/1.1 V | — |
| $AV_{DD}$_Core1 | A19 | Core 1 PLL Supply | $AV_{DD}$_Core1 0.95/1.05/1.1 V | 12, *S2* |
| $AV_{DD}$_PLAT | B19 | Platform PLL supply voltage | $AV_{DD}$_PLAT 1.05/1.1 V | — |
| $AV_{DD}$_LB | A20 | Local Bus PLL supply voltage | $AV_{DD}$_LB 1.05/1.1 V | — |
| $AV_{DD}$_SRDS1 | P32 | SerDes Port 1 PLL & DLL Power Supply | $AV_{DD}$_SRDS1 1.05/1.1 V | — |
| $AV_{DD}$_SRDS2 | AF32 | SerDes Port 2 PLL & DLL Power Supply | $AV_{DD}$_SRDS2 1.05/1.1 V | — |
| GND | C3, C6, C9, C12, C15, C23, C26, E5, E8, E11, E14, E18, E25, E28, F3, G7, G10, G13, G20, G23, G27, G30, H5, J3, J9, J12, J15, J22, J25, K7, L5, L20, M3, M9, M12, N7, N11, N13, N15, N17, N19, N21, N23, P5, P12, P16, P20, P22, R3, R9, R11, R13, R15, R17, R19, R21, R23, T7, T12, T14, T16, T18, T20, T22, U5, U11,U13, U15, U17, U19, U21, U23, V3, V9, V12, V14, V16, V18, V22, W7, W11, W13, W15, W17, W19, W21, W23,Y5, Y14, Y16, Y18, Y20, Y22, AA3, AA9, AA13, AA15, AA17, AA19, AA21, AA23, AB7, AB24, AC5, AC11, AD3, AD9, AD15, AE7, AE13, AE18, AF5, AF11, AF21, AF24, AG3, AG9, AH7, AH13, AJ5, AJ11, AK3, AK9, AK15, AK19, AK23, AL7, AL13 | GND | — | — |

**Table 63. MPC8641 Signal Reference by Functional Block (continued)**

| Name[1] | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|

37.This pin is only an output in FIFO mode when used as Rx Flow Control.

38.This pin functions as cfg_dram_type[0 or 1] at reset and MUST BE VALID BEFORE HRESET ASSERTION in device sleep mode.

39. Should be pulled to ground if unused (such as in FIFO, MII and RMII modes).

40. See Section 18.4.2, “Platform to FIFO Restrictions” for clock speed limitations for this pin when used in FIFO mode.

41. The phase between the output clocks TSEC1_GTX_CLK and TSEC2_GTX_CLK (ports 1 and 2) is no more than 100 ps. The phase between the output clocks TSEC3_GTX_CLK and TSEC4_GTX_CLK (ports 3 and 4) is no more than 100 ps.

42. For systems which boot from Local Bus (GPCM)-controlled flash, a pullup on LGPL4 is required.

**Special Notes for Single Core Device:**

*S1*. Solder ball for this signal will not be populated in the single core package.

*S2*. The PLL filter from $V_{DD}$_Core1 to $AV_{DD}$_Core1 should be removed. $AV_{DD}$_Core1 should be pulled to ground with a weak (2–10 kΩ) resistor. See Section 20.2.1, “PLL Power Supply Filtering” for more details.

*S3*. This pin should be pulled to GND for the single core device.

*S4*. No special requirement for this pin on single core device. Pin should be tied to power supply as directed for dual core.

# 18 Clocking

This section describes the PLL configuration of the MPC8641. Note that the platform clock is identical to the MPX clock.

## 18.1 Clock Ranges

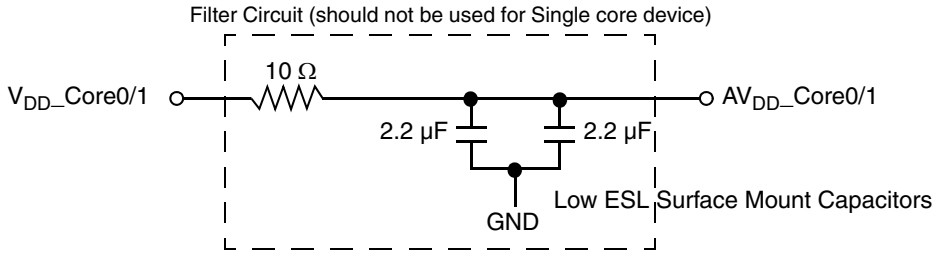
Table 64 provides the clocking specifications for the processor cores and Table 65 provides the clocking specifications for the memory bus. Table 66 provides the clocking for the Platform/MPX bus and Table 67 provides the clocking for the Local bus.

**Table 64. Processor Core Clocking Specifications**

| Characteristic | Maximum Processor Core Frequency | | | | | | | | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|---|
| | 1000 MHz | | 1250MHz | | 1333MHz | | 1500 MHz | | | |
| | Min | Max | Min | Max | Min | Max | Min | Max | | |
| e600 core processor frequency | 800 | 1000 | 800 | 1250 | 800 | 1333 | 800 | 1500 | MHz | 1, 2 |

**Notes**:

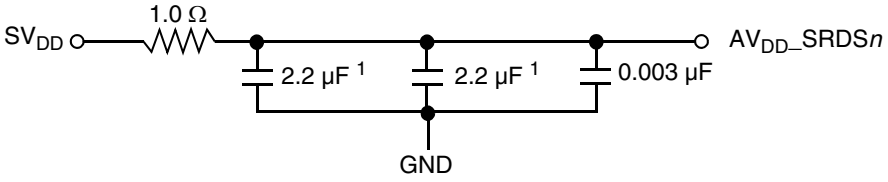
1. **Caution:** The MPX clock to SYSCLK ratio and e600 core to MPX clock ratio settings must be chosen such that the resulting SYSCLK frequency, e600 (core) frequency, and MPX clock frequency do not exceed their respective maximum or minimum operating frequencies. Refer to Section 18.2, “MPX to SYSCLK PLL Ratio,” and Section 18.3, “e600 to MPX clock PLL Ratio,” for ratio settings.
2. The minimum e600 core frequency is based on the minimum platform clock frequency of 400 MHz.




**Note:** For single core device the filter circuit (in the dashed box) should be removed and $AV_{DD}$_Core1 should be tied to ground with a weak (2-10 kΩ) pull-down resistor.

**Figure 64. MPC8641 PLL Power Supply Filter Circuit (for cores)**

The $AV_{DD}$_SRDS*n* signals provide power for the analog portions of the SerDes PLL. To ensure stability of the internal clock, the power supplied to the PLL is filtered using a circuit similar to the one shown in following figure. For maximum effectiveness, the filter circuit is placed as closely as possible to the $AV_{DD}$_SRDS*n* balls to ensure it filters out as much noise as possible. The ground connection should be near the $AV_{DD}$_SRDS*n* balls. The 0.003-µF capacitor is closest to the balls, followed by the two 2.2-µF capacitors, and finally the 1 Ω resistor to the board supply plane. The capacitors are connected from $AV_{DD}$_SRDS*n* to the ground plane. Use ceramic chip capacitors with the highest possible self-resonant frequency. All traces should be kept short, wide and direct.




1. An 0805 sized capacitor is recommended for system initial bring-up.

**Figure 65. SerDes PLL Power Supply Filter**

Note the following:

- $AV_{DD}$_SRDS*n* should be a filtered version of $SV_{DD}$.
- Signals on the SerDes interface are fed from the $SV_{DD}$ power plan.

## 20.2.2 PLL Power Supply Sequencing

For details on power sequencing for the $AV_{DD}$ type and supplies refer to Section 2.2, "Power Up/Down Sequence."

# 20.3 Decoupling Recommendations

Due to large address and data buses, and high operating frequencies, the device can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the MPC8641 system, and the device itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system

The following pins must be connected to GND:

- SD*n*_RX[7:0]
- $\overline{\text{SD}n\text{\_RX}}$[7:0]
- SD*n*_REF_CLK
- $\overline{\text{SD}n\text{\_REF\_CLK}}$

**NOTE**

It is recommended to power down the unused lane through SRDS1CR1[0:7] register (offset = 0xE_0F08) and SRDS2CR1[0:7] register (offset = 0xE_0F44.) (This prevents the oscillations and holds the receiver output in a fixed state.) that maps to SERDES lane 0 to lane 7 accordingly.

For other directions on reserved or no-connects pins see Section 17, "Signal Listings."

## 20.6 Pull-Up and Pull-Down Resistor Requirements

The MPC8641 requires weak pull-up resistors (2–10 kΩ is recommended) on all open drain type pins.

The following pins must NOT be pulled down during power-on reset: TSEC4_TXD[4], LGPL0/LSDA10, LGPL1/$\overline{\text{LSDWE}}$, TRIG_OUT/READY, and D1_MSRCID[2].

The following are factory test pins and require strong pull up resistors (100 Ω –1 kΩ) to OVDD

LSSD_MODE, TEST_MODE[0:3].The following pins require weak pull up resistors (2–10 kΩ) to their specific power supplies: LCS[0:4], LCS[5]/DMA_DREQ2, LCS[6]/DMA_DACK[2], LCS[7]/DMA_DDONE[2], IRQ_OUT, IIC1_SDA, IIC1_SCL, IIC2_SDA, IIC2_SCL, and CKSTP_OUT.

The following pins should be pulled to ground with a 100-Ω resistor: SD1_IMP_CAL_TX, SD2_IMP_CAL_TX. The following pins should be pulled to ground with a 200-Ω resistor: SD1_IMP_CAL_RX, SD2_IMP_CAL_RX.

TSEC*n*_TX_EN signals require an external 4.7-kΩ pull down resistor to prevent PHY from seeing a valid Transmit Enable before it is actively driven.

When the platform frequency is 400 MHz, TSEC1_TXD[1] must be pulled down at reset.

TSEC2_TXD[4] and TSEC2_TX_ER pins function as cfg_dram_type[0 or 1] at reset and MUST BE VALID BEFORE HRESET ASSERTION when coming out of device sleep mode.

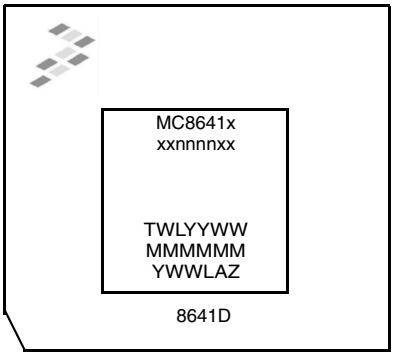
### 20.6.1 Special instructions for Single Core device

The mechanical drawing for the single core device does not have all the solder balls that exist on the single core device. This includes all the balls for VDD_Core1 and $\text{SENSEV}_{\text{DD}}$_Core1 which exist on the package for the dual core device, but not on the single core package. A solder ball is present for $\text{SENSEV}_{\text{SS}}$_Core1 and needs to be connected to ground with a weak (2-10 kΩ) pull down resistor. Likewise, $\text{AV}_{\text{DD}}$_Core1 needs to be pulled to ground as shown in Figure 64.

The mechanical drawing for the single core device is located in Section 16.2, "Mechanical Dimensions of the MPC8641 FC-CBGA."

## 21.2 Part Marking

Parts are marked as the example shown in Figure 70.




NOTE:
TWLYYWW is the test code
MMMMMM is the M00 (mask) number.
YWWLAZ is the assembly traceability code.

**Figure 70. Part Marking for FC-CBGA Device**

# 22 Document Revision History

Table 76 provides a revision history for the MPC8641D hardware specification.

**Table 76. Document Revision History**

| Revision | Date | Substantive Change(s) |
|---|---|---|
| 3 | 05/2014 | • Updated the Serial RapidIO equation in Section 4.4, “Platform Frequency Requirements for PCI-Express and Serial RapidIO”<br>• Updated Section 19.2.4, “Temperature Diode,” by removing the ideality factor value.<br>• Added VJ package type designator and footnotes to Table 74, “Part Numbering Nomenclature” and Section 16.1, “Package Parameters for the MPC8641.” |
| 2 | 07/2009 | • Added note 8 to Table 49, “Differential Transmitter (TX) Output Specifications.”<br>• Added Revision E to Table 74, “Part Numbering Nomenclature.” |
| 1 | 11/2008 | • Added Section 4.4, “Platform Frequency Requirements for PCI-Express and Serial RapidIO.”<br>• Removed the statement “Note that core processor speed of 1500 MHz is only available for the MPC8641D (dual core)” from Note 2 in Table 74 because a 1500 MHz core is offered for both MPC8641D (dual core) and MPC8641 (single core).<br>• Added Note 8 to Figure 57 and Figure 58. |
| 0 | 07/2008 | • Initial Release |