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Understanding Embedded - Microprocessors

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Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e600
Number of Cores/Bus Width	2 Core, 32-Bit
Speed	1.333GHz
Co-Processors/DSP	-
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (4)
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	1023-BBGA, FCBGA
Supplier Device Package	1023-FCCBGA (33x33)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc8641dhx1333jc

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



1.1 Key Features

The following lists an overview of the MPC8641 key feature set:

- Major features of the e600 core are as follows:
 - High-performance, 32-bit superscalar microprocessor that implements the PowerPC ISA
 - Eleven independent execution units and three register files
 - Branch processing unit (BPU)
 - Four integer units (IUs) that share 32 GPRs for integer operands
 - 64-bit floating-point unit (FPU)
 - Four vector units and a 32-entry vector register file (VRs)
 - Three-stage load/store unit (LSU)
 - Three issue queues, FIQ, VIQ, and GIQ, can accept as many as one, two, and three instructions, respectively, in a cycle.
 - Rename buffers
 - Dispatch unit
 - Completion unit
 - Two separate 32-Kbyte instruction and data level 1 (L1) caches
 - Integrated 1-Mbyte, eight-way set-associative unified instruction and data level 2 (L2) cache with ECC
 - 36-bit real addressing
 - Separate memory management units (MMUs) for instructions and data
 - Multiprocessing support features
 - Power and thermal management
 - Performance monitor
 - In-system testability and debugging features
 - Reliability and serviceability
- MPX coherency module (MCM)
 - Ten local address windows plus two default windows
 - Optional low memory offset mode for core 1 to allow for address disambiguation
- Address translation and mapping units (ATMUs)
 - Eight local access windows define mapping within local 36-bit address space
 - Inbound and outbound ATMUs map to larger external address spaces
 - Three inbound windows plus a configuration window on PCI Express
 - Four inbound windows plus a default window on serial RapidIO
 - Four outbound windows plus default translation for PCI Express
 - Eight outbound windows plus default translation for serial RapidIO with segmentation and sub-segmentation support



Table 2. Recommended Operating Conditions (continued)

Characteristic	Symbol	Recommended Value	Unit	Notes
Junction temperature range	TJ	0 to 105	°C	

Notes:

- 1. Core 1 characteristics apply only to MPC8641D
- 2. If two separate power supplies are used for V_{DD}_Core0 and V_{DD}_Core1, they must be at the same nominal voltage and the individual power supplies must be tracked and kept within 100 mV of each other during normal run time.
- 3. Caution: Dn_MV_{IN} must meet the overshoot/undershoot requirements for Dn_GV_{DD} as shown in Figure 2.
- 4. Caution: L/TV_{IN} must meet the overshoot/undershoot requirements for L/TV_{DD} as shown in Figure 2 during regular run time.
- 5. Caution: OV_{IN} must meet the overshoot/undershoot requirements for OV_{DD} as shown in Figure 2 during regular run time.
- 6. Timing limitations for M,L,T,O)V_{IN} and Dn_MV_{REF} during regular run time is provided in Figure 2
- 7. Applies to devices marked with a core frequency of 1333 MHz and below. Refer to Table 74 Part Numbering Nomenclature to determine if the device has been marked for a core frequency of 1333 MHz and below.
- 8. Applies to devices marked with a core frequency above 1333 MHz. Refer to Table 74 Part Numbering Nomenclature to determine if the device has been marked for a core frequency above 1333 MHz.
- 9. The 2.5 V \pm 125 mV range is for DDR and 1.8 V \pm 90 mV range is for DDR2.
- 10. See Section 8.2, "FIFO, GMII, MII, TBI, RGMII, RMII, and RTBI AC Timing Specifications," for details on the recommended operating conditions per protocol.
- 11. The PCI Express interface of the device is expected to receive signals from 0.175 to 1.2 V. For more information refer to Section 14.4.3, "Differential Receiver (RX) Input Specifications."
- 12. Applies to Part Number MC8641xxx1000NX only. V_{DD} _Core n = 0.95 V and V_{DD} _PLAT = 1.05 V devices. Refer to Table 74 Part Numbering Nomenclature to determine if the device has been marked for V_{DD} _Core n = 0.95 V.
- 13. This voltage is the input to the filter discussed in Section 20.2, "Power Supply Design and Sequencing," and not necessarily the voltage at the AV_{DD}_Core*n* pin, which may be reduced from V_{DD}_Core*n* by the filter.

Electrical Characteristics

NOTE

There is no required order sequence between the individual rails for this item (# 1). However, V_{DD} _PLAT, AV_{DD} _PLAT rails must reach 90% of their recommended value before the rail for Dn_GV_DD, and Dn_MV_{REF} (in next step) reaches 10% of their recommended value. AV_{DD} type supplies must be delayed with respect to their source supplies by the RC time constant of the PLL filter circuit described in Section 20.2.1, "PLL Power Supply Filtering."

2. Dn_GV_{DD} , Dn_MV_{REF}

NOTE

It is possible to leave the related power supply $(Dn_GV_{DD}, Dn_MV_{REF})$ turned off at reset for a DDR port that will not be used. Note that these power supplies can only be powered up again at reset for functionality to occur on the DDR port.

3. SYSCLK

The recommended order of power down is as follows:

- 1. Dn_GV_{DD}, Dn_MV_{REF}
- 2. All power rails other than DDR I/O (Dn_GV_{DD} , Dn_MV_{REF}).

NOTE

SYSCLK may be powered down simultaneous to either of item # 1 or # 2 in the power down sequence. Beyond this, the power supplies may power down simultaneously if the preservation of DDRn memory is not a concern.

See Figure 3 for more details on the Power and Reset Sequencing details.



Power Characteristics

3 Power Characteristics

The power dissipation for the dual core MPC8641D device is shown in Table 4.

Power Mode	Core Frequency (MHz)	Platform Frequency (MHz)	V _{DD} _Coren, V _{DD} _PLAT (Volts)	Junction Temperature	Power (Watts)	Notes
Typical				65 °C	32.1	1, 2
Thermal	1500 MHz	600 MHz	1.1 V		43.4	1, 3
Maximum				105 °C	49.9	1, 4
Typical				65 °C	23.9	1, 2
Thermal	1333 MHz	533 MHz	1.05 V		30.0	1, 3
Maximum				105 °C	34.1	1, 4
Typical				65 °C	23.9	1, 2
Thermal	1250 MHz	500 MHz	1.05 V		30.0	1, 3
Maximum				105 °C	34.1	1, 4
Typical				65 °C	23.9	1, 2
Thermal	1000 MHz	400 MHz	1.05 V		30.0	1, 3
Maximum				105 °C	34.1	1, 4
Typical			/	65 °C	16.2	1, 2, 5
Thermal	1000 MHz	500 MHz	0.95 V, 1.05 V		21.8	1, 3, 5
Maximum				105 °C	25.0	1, 4, 5

Table 4. MPC8641D Power Dissipation (Dual Core)

Notes:

1. These values specify the power consumption at nominal voltage and apply to all valid processor bus frequencies and configurations. The values do not include power dissipation for I/O supplies.

- Typical power is an average value measured at the nominal recommended core voltage (V_{DD}_Core*n*) and 65°C junction temperature (see Table 2)while running the Dhrystone 2.1 benchmark and achieving 2.3 Dhrystone MIPs/MHz with one core at 100% efficiency and the second core at 65% efficiency.
- 3. Thermal power is the average power measured at nominal core voltage (V_{DD}_Core*n*) and maximum operating junction temperature (see Table 2) while running the Dhrystone 2.1 benchmark and achieving 2.3 Dhrystone MIPs/MHz on both cores and a typical workload on platform interfaces.
- 4. Maximum power is the maximum power measured at nominal core voltage (V_{DD}_Core*n*) and maximum operating junction temperature (see Table 2) while running a test which includes an entirely L1-cache-resident, contrived sequence of instructions which keep all the execution units maximally busy on both cores.
- 5. These power numbers are for Part Number MC8641Dxx1000NX only. V_{DD} -Coren = 0.95 V and V_{DD} -PLAT = 1.05 V.



6 DDR and DDR2 SDRAM

This section describes the DC and AC electrical specifications for the DDR SDRAM interface of the MPC8641. Note that DDR SDRAM is $Dn_GV_{DD}(typ) = 2.5$ V and DDR2 SDRAM is $Dn_GV_{DD}(typ) = 1.8$ V.

6.1 DDR SDRAM DC Electrical Characteristics

Table 13 provides the recommended operating conditions for the DDR2 SDRAM component(s) of the MPC8641 when $Dn_GV_{DD}(typ) = 1.8 \text{ V}$.

Parameter/Condition	Symbol	Min	Мах	Unit	Notes
I/O supply voltage	D <i>n_</i> GV _{DD}	1.71	1.89	V	1
I/O reference voltage	Dn_MV _{REF}	$0.49 \times Dn_GV_{DD}$	$0.51 imes Dn_{DD}$	V	2
I/O termination voltage	V _{TT}	D <i>n</i> _MV _{REF} – 0.0 4	D <i>n_</i> MV _{REF} + 0.04	V	3
Input high voltage	V _{IH}	D <i>n_</i> MV _{REF} + 0.1 25	D <i>n_</i> GV _{DD} + 0.3	V	_
Input low voltage	V _{IL}	-0.3	D <i>n</i> _MV _{REF} - 0.125	V	_
Output leakage current	I _{OZ}	-50	50	μA	4
Output high current (V _{OUT} = 1.420 V)	I _{ОН}	-13.4	_	mA	_
Output low current (V _{OUT} = 0.280 V)	I _{OL}	13.4	—	mA	—

Table 13. DDR2 SDRAM DC Electrical Characteristics for Dn_GV_{DD}(typ) = 1.8 V

Notes:

1. $Dn_{GV_{DD}}$ is expected to be within 50 mV of the DRAM $Dn_{GV_{DD}}$ at all times.

2. Dn_MV_{REF} is expected to be equal to $0.5 \times Dn_GV_{DD}$, and to track Dn_GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on Dn_MV_{REF} may not exceed ±2% of the DC value.

3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to Dn_MV_{REF}. This rail should track variations in the DC level of Dn_MV_{REF}.

4. Output leakage is measured with all outputs disabled, 0 V \leq V_{OUT} \leq Dn_GV_{DD}.

Table 14 provides the DDR2 capacitance when $Dn_{GV_{DD}(typ)} = 1.8 \text{ V}$.

Parameter/Condition	Symbol	Min	Мах	Unit	Notes
Input/output capacitance: DQ, DQS, DQS	C _{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS, DQS	C _{DIO}	—	0.5	pF	1

Note:

1. This parameter is sampled. $Dn_GV_{DD} = 1.8 \text{ V} \pm 0.090 \text{ V}$, f = 1 MHz, $T_A = 25^{\circ}C$, $V_{OUT} = Dn_GV_{DD}/2$, V_{OUT} (peak-to-peak) = 0.2 V.



Ethernet: Enhanced Three-Speed Ethernet (eTSEC), MII Management



Timing diagrams for FIFO appear in Figure 8 and Figure 9.

Figure 9. FIFO Receive AC Timing Diagram

8.2.2 GMII AC Timing Specifications

This section describes the GMII transmit and receive AC timing specifications.

8.2.2.1 GMII Transmit AC Timing Specifications

Table 28 provides the GMII transmit AC timing specifications.

Table 28. GMII Transmit AC Timing Specifications

At recommended operating conditions with L/TV_DD of 3.3 V \pm 5% and 2.5 V \pm 5%.

Parameter/Condition	Symbol ¹	Min	Тур	Max	Unit
GMII data TXD[7:0], TX_ER, TX_EN setup time	t _{GTKHDV}	2.5	—	—	ns
GTX_CLK to GMII data TXD[7:0], TX_ER, TX_EN delay	t _{GTKHDX}	0.5	—	5.0	ns
GTX_CLK data clock rise time (20%-80%)	t _{GTXR} 2	_	_	1.0	ns



8.2.4 TBI AC Timing Specifications

This section describes the TBI transmit and receive AC timing specifications.

8.2.4.1 TBI Transmit AC Timing Specifications

Table 32 provides the TBI transmit AC timing specifications.

Table 32. TBI Transmit AC Timing Specifications

At recommended operating conditions with L/TV_{DD} of 3.3 V \pm 5% and 2.5 V \pm 5%.

Parameter/Condition	Symbol ¹	Min	Тур	Мах	Unit
TCG[9:0] setup time GTX_CLK going high	t _{TTKHDV}	2.0	—	—	ns
TCG[9:0] hold time from GTX_CLK going high	t _{TTKHDX}	1.0	—	—	ns
GTX_CLK rise time (20%-80%)	t _{TTXR} ²	—	—	1.0	ns
GTX_CLK fall time (80%–20%)	t _{TTXF} 2	—	—	1.0	ns

Notes:

1. The symbols used for timing specifications herein follow the pattern of t_{(first two letters of functional block)(signal)(state)(reference)(state)} for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{TTKHDV} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the valid state (V) or setup time. Also, t_{TTKHDX} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the valid state (V) or setup time. Also, t_{TTKHDX} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the invalid state (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{TTX} represents the TBI (T) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

2. Guaranteed by design.

Figure 16 shows the TBI transmit AC timing diagram.



Figure 16. TBI Transmit AC Timing Diagram



Parameter	Symbol ¹	Min	Max	Unit	Notes
Local bus clock to LALE assertion	t _{LBKHOV4}	_	2.3	ns	3
Output hold from local bus clock (except LAD/LDP and LALE)	t _{LBKHOX1}	0.7	—	ns	—
Output hold from local bus clock for LAD/LDP	t _{LBKHOX2}	0.7	—	ns	3
Local bus clock to output high Impedance (except LAD/LDP and LALE)	t _{LBKHOZ1}		2.5	ns	5
Local bus clock to output high impedance for LAD/LDP	t _{LBKHOZ2}	_	2.5	ns	5

Table 41. Local Bus Timing Parameters (OV_{DD} = 3.3 V)m - PLL Enabled (continued)

Note:

- The symbols used for timing specifications herein follow the pattern of t_{(First two letters of functional block)(signal)(state)} (reference)(state) for inputs and t_(First two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{LBIXKH1} symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one(1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
- 2. All timings are in reference to LSYNC_IN for PLL enabled and internal local bus clock for PLL bypass mode.
- 3. All signals are measured from $OV_{DD}/2$ of the rising edge of LSYNC_IN for PLL enabled or internal local bus clock for PLL bypass mode to $0.4 \times OV_{DD}$ of the signal in question for 3.3-V signaling levels.
- 4. Input timings are measured at the pin.
- 5. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
- t_{LBOTOT} is a measurement of the minimum time between the negation of LALE and any change in LAD. t_{LBOTOT} is programmed with the LBCR[AHD] parameter.
- 7. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at BV_{DD}/2.
- 8. Guaranteed by design.

Figure 25 provides the AC test load for the local bus.



Figure 25. Local Bus AC Test Load



Figure 26 to Figure 31 show the local bus signals.



Figure 26. Local Bus Signals (PLL Enabled)

NOTE

PLL bypass mode is recommended when LBIU frequency is at or below 83 MHz. When LBIU operates above 83 MHz, LBIU PLL is recommended to be enabled.

Table 42 describes the general timing parameters of the local bus interface at $OV_{DD} = 3.3$ V with PLL bypassed.

Table 42. Local Bus	Timing Parameters—F	LL Bypassed
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Parameter	Symbol ¹	Min	Мах	Unit	Notes
Local bus cycle time	t _{LBK}	12	_	ns	2
Local bus duty cycle	t _{LBKH/} t _{LBK}	45	55	%	—
Internal launch/capture clock to LCLK delay	t _{LBKHKT}	2.3	3.9	ns	8
Input setup to local bus clock (except LGTA/LUPWAIT)	t _{LBIVKH1}	5.7	_	ns	4, 5
LGTA/LUPWAIT input setup to local bus clock	t _{LBIVKL2}	5.6	_	ns	4, 5
Input hold from local bus clock (except LGTA/LUPWAIT)	t _{LBIXKH1}	-1.8	_	ns	4, 5

l²C

Table 46. I²C AC Electrical Specifications (continued)

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 45).

Parameter	Symbol ¹	Min	Мах	Unit
Noise margin at the HIGH level for each connected device (including hysteresis)	V _{NH}	$0.2 \times OV_{DD}$	_	V

Note:

- 1. The symbols used for timing specifications herein follow the pattern of t_{(first two letters of functional block)(signal)(state) (reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{12DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{12C} clock reference (K) going to the high (H) state or setup time. Also, t_{12SXKL} symbolizes I²C timing (I2) for the time that the data with respect to the start condition (S) went invalid (X) relative to the t_{12C} clock reference (K) going to the low (L) state or hold time. Also, t_{12PVKH} symbolizes I²C timing (I2) for the time that the data with respect to the stop condition (P) reaching the valid state (V) relative to the t_{12C} clock reference (K) going to the stop condition (P) reaching the valid state (V) relative to the t_{12C} clock reference (K) going to the latter convention is used with the appropriate letter: R (rise) or F (fall).}
- 2. As a transmitter, the MPC8641 provides a delay time of at least 300 ns for the SDA signal (referred to the Vihmin of the SCL signal) to bridge the undefined region of the falling edge of SCL to avoid unintended generation of Start or Stop condition. When MPC8641 acts as the I²C bus master while transmitting, MPC8641 drives both SCL and SDA. As long as the load on SCL and SDA are balanced, MPC8641 would not cause unintended generation of Start or Stop condition. Therefore, the 300 ns SDA output delay time is not a concern. If, under some rare condition, the 300 ns SDA output delay time is required for MPC8641 as transmitter, the following setting is recommended for the FDR bit field of the I2CFDR register to ensure both the desired I²C SCL clock frequency and SDA output delay time are achieved, assuming that the desired I²C SCL clock frequency is 400 KHz and the Digital Filter Sampling Rate Register (I2CDFSRR) is programmed with its default setting of 0x10 (decimal 16):

I ² C Source Clock Frequency	333 MHz	266 MHz	200 MHz	133 MHz
FDR Bit Setting	0x2A	0x05	0x26	0x00
Actual FDR Divider Selected	896	704	512	384
Actual I ² C SCL Frequency Generated	371 KHz	378 KHz	390 KHz	346 KHz

For the detail of I²C frequency calculation, refer to the application note AN2919 "Determining the I²C Frequency Divider Ratio for SCL". Note that the I²C Source Clock Frequency is half of the MPX clock frequency for MPC8641.

- 3. The maximum t_{I2DXKL} has only to be met if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.
- 4. Guaranteed by design.
- 5. C_B = capacitance of one bus line in pF.

Figure 32 provides the AC test load for the I^2C .



Figure 36. I²C AC Test Load



High-Speed Serial Interfaces (HSSI)

13.2.3 Interfacing With Other Differential Signaling Levels

With on-chip termination to SGND, the differential reference clocks inputs are HCSL (High-Speed Current Steering Logic) compatible DC-coupled.

Many other low voltage differential type outputs like LVDS (Low Voltage Differential Signaling) can be used but may need to be AC-coupled due to the limited common mode input range allowed (100 to 400 mV) for DC-coupled connection.

LVPECL outputs can produce signal with too large amplitude and may need to be DC-biased at clock driver output first, then followed with series attenuation resistor to reduce the amplitude, in addition to AC-coupling.

NOTE

Figure 43 to Figure 46 below are for conceptual reference only. Due to the fact that clock driver chip's internal structure, output impedance and termination requirements are different between various clock driver chip manufacturers, it is very possible that the clock circuit reference designs provided by clock driver chip vendor are different from what is shown below. They might also vary from one vendor to the other. Therefore, Freescale Semiconductor can neither provide the optimal clock driver reference circuits, nor guarantee the correctness of the following clock driver connection reference circuits. The system designer is recommended to contact the selected clock driver chip vendor for the optimal reference circuits with the MPC8641D SerDes reference clock receiver requirement provided in this document.



High-Speed Serial Interfaces (HSSI)

MPC8641D SerDes reference clock input's DC requirement, AC-coupling has to be used. Figure 45 assumes that the LVPECL clock driver's output impedance is 50 Ω . R1 is used to DC-bias the LVPECL outputs prior to AC-coupling. Its value could be ranged from 140 Ω to 240 Ω depending on clock driver vendor's requirement. R2 is used together with the SerDes reference clock receiver's 50- Ω termination resistor to attenuate the LVPECL output's differential peak level such that it meets the MPC8641D SerDes reference clock's differential input amplitude requirement (between 200 mV and 800 mV differential peak). For example, if the LVPECL output's differential peak is 900 mV and the desired SerDes reference clock input amplitude is selected as 600mV, the attenuation factor is 0.67, which requires R2 = 25 Ω . Please consult clock driver chip manufacturer to verify whether this connection scheme is compatible with a particular clock driver chip.



Figure 45. AC-Coupled Differential Connection with LVPECL Clock Driver (Reference Only)



PCI Express

14.1 DC Requirements for PCI Express SD*n*_REF_CLK and SD*n*_REF_CLK

For more information, see Section 13.2, "SerDes Reference Clocks."

14.2 AC Requirements for PCI Express SerDes Clocks

Table 48 lists AC requirements.

Table 48. SDn_REF_CLK and SDn_REF_CLK AC Requirements

Symbol	Parameter Description	Min	Typical	Max	Units	Notes
t _{REF}	REFCLK cycle time	_	10	_	ns	_
t _{REFCJ}	REFCLK cycle-to-cycle jitter. Difference in the period of any two adjacent REFCLK cycles	—	—	100	ps	_
t _{REFPJ}	Phase jitter. Deviation in edge location with respect to mean edge location	-50	—	50	ps	

14.3 Clocking Dependencies

The ports on the two ends of a link must transmit data at a rate that is within 600 parts per million (ppm) of each other at all times. This is specified to allow bit rate clock sources with a +/-300 ppm tolerance.

14.4 Physical Layer Specifications

The following is a summary of the specifications for the physical layer of PCI Express on this device. For further details as well as the specifications of the Transport and Data Link layer please use the PCI EXPRESS Base Specification. REV. 1.0a document.

14.4.1 Differential Transmitter (TX) Output

Table 49 defines the specifications for the differential output at all transmitters (TXs). The parameters are specified at the component pins.

Symbol	Parameter	Min	Nom	Max	Units	Comments
UI	Unit Interval	399.88	400	400.12	ps	Each UI is 400 ps \pm 300 ppm. UI does not account for Spread Spectrum Clock dictated variations. See Note 1.
V _{TX-DIFFp-p}	Differential Peak-to-Peak Output Voltage	0.8	—	1.2	V	$V_{TX-DIFFp-p} = 2^* V_{TX-D+} - V_{TX-D-} $ See Note 2.
V _{TX-DE-RATIO}	De- Emphasized Differential Output Voltage (Ratio)	-3.0	-3.5	-4.0	dB	Ratio of the $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the $V_{TX-DIFFp-p}$ of the first bit after a transition. See Note 2.

Table 49. Differential Transmitter (TX) Output Specifications



16.2 Mechanical Dimensions of the MPC8641 FC-CBGA

The mechanical dimensions and bottom surface nomenclature of the MPC8641D (dual core) and MPC8641 (single core) high-lead FC-CBGA (package option: HCTE HX) and lead-free FC-CBGA (package option: HCTE VU) are shown respectfully in Figure 57 and Figure 58.





NOTES for Figure 57

- 1. All dimensions are in millimeters.
- 2. Dimensions and tolerances per ASME Y14.5M-1994.
- 3. Maximum solder ball diameter measured parallel to datum A.
- 4. Datum A, the seating plane, is defined by the spherical crowns of the solder balls.
- 5. Capacitors may not be present on all devices.
- 6. Caution must be taken not to short capacitors or expose metal capacitor pads on package top.
- 7. All dimensions symmetrical about centerlines unless otherwise specified.



Name ¹	Package Pin Number	Pin Type	Power Supply	Notes			
SD1_PLL_TPA	T28	Analog	SV _{DD}	13, 18			
SD1_DLL_TPD	N28	0	SV _{DD}	13, 17			
SD1_DLL_TPA	P31	Analog	SV _{DD}	13, 18			
High Speed I/O Interface 2 (SERDES 2) ⁴							
SD2_TX[0:3]	Y24, AA27, AB25, AC27	0	SV _{DD}	_			
SD2_TX[4:7]	AE27, AG27, AJ27, AL27	0	SV _{DD}	34			
SD2_TX[0:3]	Y25, AA28, AB26, AC28	0	SV _{DD}	—			
SD2_TX[4:7]	AE28, AG28, AJ28, AL28	0	SV _{DD}	34			
SD2_RX[0:3]	Y30, AA32, AB30, AC32	I	SV _{DD}	32			
SD2_RX[4:7]	AH30, AJ32, AK30, AL32	I	SV _{DD}	32, 35			
SD2_RX[0:3]	Y29, AA31, AB29, AC31	I	SV _{DD}	_			
SD2_RX[4:7]	AH29, AJ31, AK29, AL31	I	SV _{DD}	35			
SD2_REF_CLK	AE32	I	SV _{DD}	_			
SD2_REF_CLK	AE31	I	SV _{DD}	_			
SD2_IMP_CAL_TX	AM29	Analog	SV _{DD}	19			
SD2_IMP_CAL_RX	AA26	Analog	SV _{DD}	30			
SD2_PLL_TPD	AF29	0	SV _{DD}	13, 17			
SD2_PLL_TPA	AF31	Analog	SV _{DD}	13, 18			
SD2_DLL_TPD	AD29	0	SV _{DD}	13, 17			
SD2_DLL_TPA	AD30	Analog	SV _{DD}	13, 18			
	Special Connection Requir	ement pins	<u> </u>				
No Connects	K24, K25, P28, P29, W26, W27, AD25, AD26	_	-	13			
Reserved	H30, R32, V28, AG32	—	—	14			
Reserved	H29, R31, W28, AG31	—	—	15			
Reserved	AD24, AG26	—	—	16			
	Ethernet Miscellaneous	Signals ⁵					
EC1_GTX_CLK125	AL23	I	LV _{DD}	39			
EC2_GTX_CLK125	AM23	I	TV _{DD}	39			
EC_MDC	G31	0	OV _{DD}	_			
EC_MDIO	G32	I/O	OV _{DD}	_			
eTSEC Port 1 Signals ⁵							

Table 63. MPC8641 Signal Reference by Functional Block (continued)



Signal Listings

Name ¹	Package Pin Number	Pin Type	Power Supply	Notes		
TSEC1_TXD[0:7]/ GPOUT[0:7]	AF25, AC23,AG24, AG23, AE24, AE23, AE22, AD22	0	LV _{DD}	6, 10		
TSEC1_TX_EN	AB22	0	LV _{DD}	36		
TSEC1_TX_ER	AH26	0	LV _{DD}	_		
TSEC1_TX_CLK	AC22	I	LV _{DD}	40		
TSEC1_GTX_CLK	AH25	0	LV _{DD}	41		
TSEC1_CRS	AM24	I/O	LV _{DD}	37		
TSEC1_COL	AM25	I	LV _{DD}	—		
TSEC1_RXD[0:7]/ GPIN[0:7]	AL25, AL24, AK26, AK25, AM26, AF26, AH24, AG25	I	LV _{DD}	10		
TSEC1_RX_DV	AJ24	I	LV _{DD}	_		
TSEC1_RX_ER	AJ25	I	LV _{DD}	_		
TSEC1_RX_CLK	AK24	I	LV _{DD}	40		
	eTSEC Port 2 Signals ⁵					
TSEC2_TXD[0:3]/ GPOUT[8:15]	AB20, AJ23, AJ22, AD19	0	LV _{DD}	6, 10		
TSEC2_TXD[4]/ GPOUT[12]	AH23	0	LV _{DD}	6,10, 38		
TSEC2_TXD[5:7]/ GPOUT[13:15]	AH21, AG22, AG21	0	LV _{DD}	6, 10		
TSEC2_TX_EN	AB21	0	LV _{DD}	36		
TSEC2_TX_ER	AB19	0	LV _{DD}	6, 38		
TSEC2_TX_CLK	AC21	I	LV _{DD}	40		
TSEC2_GTX_CLK	AD20	0	LV _{DD}	41		
TSEC2_CRS	AE20	I/O	LV _{DD}	37		
TSEC2_COL	AE21	I	LV _{DD}	—		
TSEC2_RXD[0:7]/ GPIN[8:15]	AL22, AK22, AM21, AH20, AG20, AF20, AF23, AF22	I	LV _{DD}	10		
TSEC2_RX_DV	AC19	I	LV _{DD}	—		
TSEC2_RX_ER	AD21	I	LV _{DD}	_		
TSEC2_RX_CLK	AM22	I	LV _{DD}	40		
eTSEC Port 3 Signals ⁵						
TSEC3_TXD[0:3]	AL21, AJ21, AM20, AJ20	0	TV _{DD}	6		
TSEC3_TXD[4]/	AM19	0	TV _{DD}	_		
TSEC3_TXD[5:7]	AK21, AL20, AL19	0	TV _{DD}	6		

Table 63. MPC8641 Signal Reference by Functional Block (continued)



Tyco Electronics800-522-6752Chip CoolersTMP.O. Box 3668Harrisburg, PA 17105-3668Internet: www.chipcoolers.comWakefield Engineering603-635-510233 Bridge St.Pelham, NH 03076Internet: www.wakefield.comInternet: www.wakefield.com

Ultimately, the final selection of an appropriate heat sink depends on many factors, such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost.

19.2.1 Internal Package Conduction Resistance

For the exposed-die packaging technology described in Table 71, the intrinsic conduction thermal resistance paths are as follows:

- The die junction-to-case thermal resistance (the case is actually the top of the exposed silicon die)
- The die junction-to-board thermal resistance

Figure 60 depicts the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.



Figure 60. C4 Package with Heat Sink Mounted to a Printed-Circuit Board

Heat generated on the active side of the chip is conducted through the silicon, through the heat sink attach material (or thermal interface material), and finally to the heat sink where it is removed by forced-air convection.

Because the silicon thermal resistance is quite small, the temperature drop in the silicon may be neglected for a first-order analysis. Thus the thermal interface material and the heat sink conduction/convective thermal resistances are the dominant terms.





Top View of Model (Not to Scale)

Figure 62. Recommended Thermal Model of MPC8641

19.2.4 Temperature Diode

The MPC8641 has a temperature diode on the microprocessor that can be used in conjunction with other system temperature monitoring devices (such as Analog Devices, ADT7461TM). These devices use the negative temperature coefficient of a diode operated at a constant current to determine the temperature of the microprocessor and its environment. It is recommended that each device be individually calibrated.

The following are the specifications of the MPC8641 on-board temperature diode:

 $V_{f} > 0.40 V$

 $V_{f} < 0.90 V$

An approximate value of the ideality may be obtained by calibrating the device near the expected operating temperature.

Ideality factor is defined as the deviation from the ideal diode equation:

$$\mathbf{I}_{\text{fw}} = \mathbf{I}_{s} \left[\mathbf{e}^{\frac{\mathbf{q}\mathbf{V}_{f}}{\mathbf{n}\mathbf{K}\mathbf{T}}} - \mathbf{1} \right]$$



System Design Information

20 System Design Information

This section provides electrical and thermal design recommendations for successful application of the MPC8641.

20.1 System Clocking

This device includes six PLLs, as follows:

- 1. The platform PLL generates the platform clock from the externally supplied SYSCLK input. The frequency ratio between the platform and SYSCLK is selected using the platform PLL ratio configuration bits as described in Section 18.2, "MPX to SYSCLK PLL Ratio."
- 2. The dual e600 Core PLLs generate the e600 clock from the externally supplied input.
- 3. The local bus PLL generates the clock for the local bus.
- 4. There are two internal PLLs for the SerDes block.

20.2 Power Supply Design and Sequencing

20.2.1 PLL Power Supply Filtering

Each of the PLLs listed above is provided with power through independent power supply pins.

There are a number of ways to reliably provide power to the PLLs, but the recommended solution is to provide independent filter circuits per PLL power supply as illustrated in Figure 64, one to each of the AV_{DD} type pins. By providing independent filters to each PLL the opportunity to cause noise injection from one PLL to the other is reduced.

This circuit is intended to filter noise in the PLLs resonant frequency range from a 500 kHz to 10 MHz range. It should be built with surface mount capacitors with minimum Effective Series Inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

Each circuit should be placed as close as possible to the specific AV_{DD} type pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the AV_{DD} type pin, which is on the periphery of the footprint, without the inductance of vias.

Figure 63 and Figure 64 show the PLL power supply filter circuits for the platform and cores, respectively.



Figure 63. MPC8641 PLL Power Supply Filter Circuit (for platform and Local Bus)



For other pin pull-up or pull-down recommendations of signals, please see Section 17, "Signal Listings."

20.7 Output Buffer DC Impedance

The MPC8641 drivers are characterized over process, voltage, and temperature. For all buses, the driver is a push-pull single-ended driver type (open drain for I^2C).

To measure Z_0 for the single-ended drivers, an external resistor is connected from the chip pad to OV_{DD} or GND. Then, the value of each resistor is varied until the pad voltage is $OV_{DD}/2$ (see Figure 66). The output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held high, SW1 is closed (SW2 is open) and R_p is trimmed until the voltage at the pad equals $OV_{DD}/2$. R_p then becomes the resistance of the pull-up devices. R_p and R_N are designed to be close to each other in value. Then, $Z_0 = (R_p + R_N)/2$.



Figure 66. Driver Impedance Measurement

Table 73 summarizes the signal impedance targets. The driver impedances are targeted at minimum V_{DD} , nominal OV_{DD} , 105°C.

Impedance	DUART, Control, Configuration, Power Management	PCI Express	DDR DRAM	Symbol	Unit
R _N	43 Target	25 Target	20 Target	Z ₀	W
R _P	43 Target	25 Target	20 Target	Z ₀	W

Table 73. Impedance Characteristics

Note: Nominal supply voltages. See Table 1, $T_i = 105^{\circ}C$.