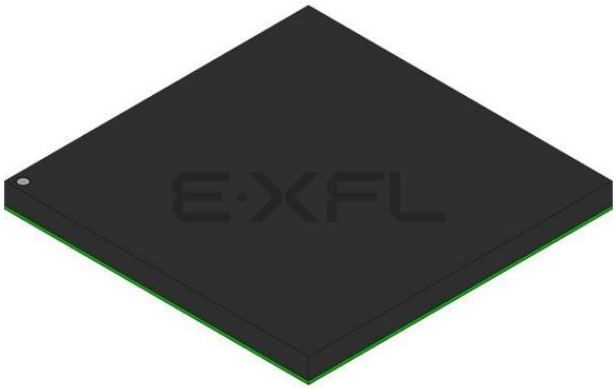

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Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	PowerPC e600
Number of Cores/Bus Width	2 Core, 32-Bit
Speed	1.333GHz
Co-Processors/DSP	-
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (4)
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	1023-BCBGA, FCCBGA
Supplier Device Package	1023-FCCBGA (33x33)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc8641dhx1333je

2 Electrical Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC8641. The MPC8641 is currently targeted to these specifications.

2.1 Overall DC Electrical Characteristics

This section covers the ratings, conditions, and other characteristics.

2.1.1 Absolute Maximum Ratings

Table 1 provides the absolute maximum ratings.

Table 1. Absolute Maximum Ratings[1]

Characteristic	Symbol	Absolute Maximum Value	Unit	Notes
Cores supply voltages	V_{DD}_Core0, V_{DD}_Core1	–0.3 to 1.21 V	V	2
Cores PLL supply	AV_{DD}_Core0, AV_{DD}_Core1	–0.3 to 1.21 V	V	—
SerDes Transceiver Supply (Ports 1 and 2)	SV_{DD}	–0.3 to 1.21 V	V	—
SerDes Serial I/O Supply Port 1	XV_{DD}_SRDS1	–0.3 to 1.21V	V	—
SerDes Serial I/O Supply Port 2	XV_{DD}_SRDS2	–0.3 to 1.21 V	V	—
SerDes DLL and PLL supply voltage for Port 1 and Port 2	AV_{DD}_SRDS1, AV_{DD}_SRDS2	–0.3 to 1.21V	V	—
Platform Supply voltage	V_{DD}_PLAT	–0.3 to 1.21V	V	—
Local Bus and Platform PLL supply voltage	AV_{DD}_LB, AV_{DD}_PLAT	–0.3 to 1.21V	V	—
DDR and DDR2 SDRAM I/O supply voltages	D1_GV_{DD}, D2_GV_{DD}	–0.3 to 2.75 V	V	3
		–0.3 to 1.98 V	V	3
eTSEC 1 and 2 I/O supply voltage	LV_{DD}	–0.3 to 3.63 V	V	4
		–0.3 to 2.75 V	V	4
eTSEC 3 and 4 I/O supply voltage	TV_{DD}	–0.3 to 3.63 V	V	4
		–0.3 to 2.75 V	V	4
Local Bus, DUART, DMA, Multiprocessor Interrupts, System Control & Clocking, Debug, Test, Power management, I^2C, JTAG and Miscellaneous I/O voltage	OV_{DD}	–0.3 to 3.63 V	V	—

Table 2. Recommended Operating Conditions (continued)

Characteristic		Symbol	Recommended Value	Unit	Notes
SerDes Serial I/O Supply Port 1		XV_{DD}_SRDS1	1.10 ± 50 mV	V	8
			1.05 ± 50 mV		7
SerDes Serial I/O Supply Port 2		XV_{DD}_SRDS2	1.10 ± 50 mV	V	8
			1.05 ± 50 mV		7
SerDes DLL and PLL supply voltage for Port 1 and Port 2		AV_{DD}_SRDS1, AV_{DD}_SRDS2	1.10 ± 50 mV	V	8
			1.05 ± 50 mV		7
Platform Supply voltage		V_{DD}_PLAT	1.10 ± 50 mV	V	8
			1.05 ± 50 mV		7
Local Bus and Platform PLL supply voltage		AV_{DD}_LB, AV_{DD}_PLAT	1.10 ± 50 mV	V	8
			1.05 ± 50 mV		7
DDR and DDR2 SDRAM I/O supply voltages		D1_GV_{DD}, D2_GV_{DD}	2.5 V ± 125 mV	V	9
			1.8 V ± 90 mV	V	9
eTSEC 1 and 2 I/O supply voltage		LV_{DD}	3.3 V ± 165 mV	V	10
			2.5 V ± 125 mV	V	10
eTSEC 3 and 4 I/O supply voltage		TV_{DD}	3.3 V ± 165 mV	V	10
			2.5 V ± 125 mV	V	10
Local Bus, DUART, DMA, Multiprocessor Interrupts, System Control & Clocking, Debug, Test, Power management, I^2C, JTAG and Miscellaneous I/O voltage		OV_{DD}	3.3 V ± 165 mV	V	5
Input voltage	DDR and DDR2 SDRAM signals	D*n*_MV_{IN}	GND to D*n*_GV_{DD}	V	3, 6
	DDR and DDR2 SDRAM reference	D*n*_MV_{REF}	D*n*_GV_{DD}/2 ± 1%	V	
	Three-speed Ethernet signals	LV_{IN} TV_{IN}	GND to LV_{DD} GND to TV_{DD}	V	4, 6
	DUART, Local Bus, DMA, Multiprocessor Interrupts, System Control & Clocking, Debug, Test, Power management, I^2C, JTAG and Miscellaneous I/O voltage	OV_{IN}	GND to OV_{DD}	V	5,6

2.1.3 Output Driver Characteristics

Table 3 provides information on the characteristics of the output driver strengths. The values are preliminary estimates.

Table 3. Output Drive Capability

Driver Type	Programmable Output Impedance (Ω)	Supply Voltage	Notes
DDR1 signal	18 36 (half strength mode)	D*n*_GV_{DD} = 2.5 V	4, 9
DDR2 signal	18 36 (half strength mode)	D*n*_GV_{DD} = 1.8 V	1, 5, 9
Local Bus signals	45 25	OV_{DD} = 3.3 V	2, 6
eTSEC/10/100 signals	45	T/LV_{DD} = 3.3 V	6
	30	T/LV_{DD} = 2.5 V	6
DUART, DMA, Multiprocessor Interrupts, System Control & Clocking, Debug, Test, Power management, JTAG and Miscellaneous I/O voltage	45	OV_{DD} = 3.3 V	6
I^2C	150	OV_{DD} = 3.3 V	7
SRIO, PCI Express	100	SV_{DD} = 1.1/1.05 V	3, 8

Notes:
1. See the DDR Control Driver registers in the MPC8641D reference manual for more information.
2. Only the following local bus signals have programmable drive strengths: LALE, LAD[0:31], LDP[0:3], LA[27:31], LCKE, LCS[1:2], LWE[0:3], LGPL1, LGPL2, LGPL3, LGPL4, LGPL5, LCLK[0:2]. The other local bus signals have a fixed drive strength of 45 Ω. See the POR Impedance Control register in the MPC8641D reference manual for more information about local bus signals and their drive strength programmability.
3. See Section 17, "Signal Listings," for details on resistor requirements for the calibration of SD*n*_IMP_CAL_TX and SD*n*_IMP_CAL_RX transmit and receive signals.
4. Stub Series Terminated Logic (SSTL-25) type pins.
5. Stub Series Terminated Logic (SSTL-18) type pins.
6. Low Voltage Transistor-Transistor Logic (LVTTL) type pins.
7. Open Drain type pins.
8. Low Voltage Differential Signaling (LVDS) type pins.
9. The drive strength of the DDR interface in half strength mode is at T_j = 105C and at D*n*_GV_{DD} (min).

2.2 Power Up/Down Sequence

The MPC8641 requires its power rails to be applied in a specific sequence in order to ensure proper device operation.

NOTE

The recommended maximum ramp up time for power supplies is 20 milliseconds.

The chronological order of power up is as follows:

1. All power rails other than DDR I/O (D*n*_GV_{DD}, and D*n*_MV_{REF}).

The maximum power dissipation for individual power supplies of the MPC8641D is shown in Table 5.

Table 5. MPC8641D Individual Supply Maximum Power Dissipation [1]

Component Description	Supply Voltage (Volts)	Power (Watts)	Notes
Per Core voltage Supply	V_{DD}_Core0/V_{DD}_Core1 = 1.1 V @ 1500 MHz	21.00	
Per Core PLL voltage supply	AV_{DD}_Core0/AV_{DD}_Core1 = 1.1 V @ 1500 MHz	0.0125	
Per Core voltage Supply	V_{DD}_Core0/V_{DD}_Core1 = 1.05 V @ 1333 MHz	17.00	
Per Core PLL voltage supply	AV_{DD}_Core0/AV_{DD}_Core1 = 1.05 V @ 1333 MHz	0.0125	
Per Core voltage Supply	V_{DD}_Core0/V_{DD}_Core1 = 0.95 V @ 1000 MHz	11.50	5
Per Core PLL voltage supply	AV_{DD}_Core0/AV_{DD}_Core1 = 0.95 V @ 1000 MHz	0.0125	5
DDR Controller I/O voltage supply	D*n*_GV_{DD} = 2.5 V @ 400 MHz	0.80	2
	D*n*_GV_{DD} = 1.8 V @ 533 MHz	0.68	2
	D*n*_GV_{DD} = 1.8 V @ 600 MHz	0.77	2
16-bit FIFO @ 200 MHz eTsec 1&2/3&4 Voltage Supply	L/TV_{DD} = 3.3 V	0.11	2, 3
non-FIFO eTsec*n* Voltage Supply	L/TV_{DD} = 3.3 V	0.08	2
x8 SerDes transceiver Supply	SV_{DD} = 1.1 V	0.70	2
x8 SerDes I/O Supply	XV_{DD}_SRDS*n* = 1.1 V	0.66	2
SerDes PLL voltage supply Port 1 or 2	AV_{DD}_SRDS1/AV_{DD}_SRDS2 = 1.1 V	0.10	
Platform I/O Supply	OV_{DD} = 3.3 V	0.45	4
Platform source Supply	V_{DD}_PLAT = 1.1 V @ 600 MHz	12.00	
Platform source Supply	V_{DD}_PLAT = 1.05 Vn @ 500 MHz	9.80	5
Platform source Supply	V_{DD}_PLAT = 1.05 Vn @ 400 MHz	7.70	
Platform, Local Bus PLL voltage Supply	AV_{DD}_PLAT, AV_{DD}_LB = 1.1 V	0.0125	

Notes:

1. This is a maximum power supply number which is provided for power supply and board design information. The numbers are based on 100% bus utilization for each component. The components listed are not expected to have 100% bus usage simultaneously for all components. Actual numbers may vary based on activity.
2. Number is based on a per port/interface value.
3. This is based on one eTSEC port used. Since 16-bit FIFO mode involves two ports, the number will need to be multiplied by two for the total. The other eTSEC protocols dissipate less than this number per port. Note that the power needs to be multiplied by the number of ports used for the protocol for the total eTSEC port power dissipation.
4. This includes Local Bus, DUART, I^2C, DMA, Multiprocessor Interrupts, System Control & Clocking, Debug, Test, Power management, JTAG and Miscellaneous I/O voltage.
5. These power numbers are for Part Number MC8641xxx1000NX only. V_{DD}_Core*n* = 0.95 V and V_{DD}_PLAT = 1.05 V.

Table 28. GMII Transmit AC Timing Specifications (continued)

At recommended operating conditions with L/TV_{DD} of 3.3 V ± 5% and 2.5 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
GTX_CLK data clock fall time (80%-20%)	t_{GTXF}[2]	—	—	1.0	ns

Notes:

1. The symbols used for timing specifications herein follow the pattern $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{GTKHDV} symbolizes GMII transmit timing (GT) with respect to the t_{GTX} clock reference (K) going to the high state (H) relative to the time date input signals (D) reaching the valid state (V) to state or setup time. Also, t_{GTKHDX} symbolizes GMII transmit timing (GT) with respect to the t_{GTX} clock reference (K) going to the high state (H) relative to the time date input signals (D) going invalid (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{GTX} represents the GMII(G) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Guaranteed by design.

Figure 10 shows the GMII transmit AC timing diagram.

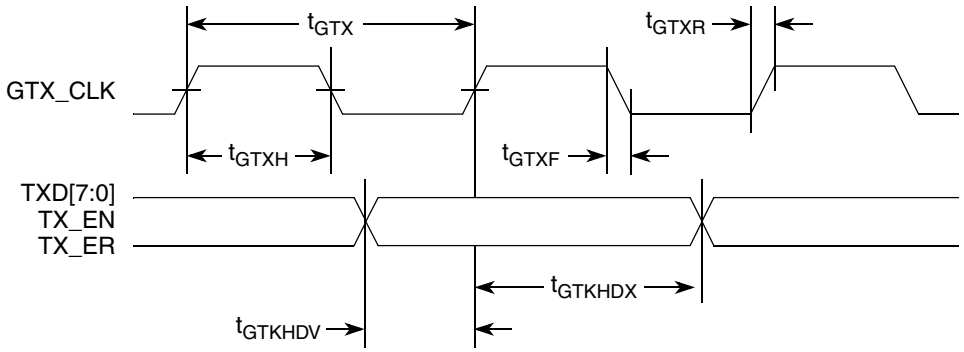


Figure 10. GMII Transmit AC Timing Diagram

8.2.2.2 GMII Receive AC Timing Specifications

Table 29 provides the GMII receive AC timing specifications.

Table 29. GMII Receive AC Timing Specifications

At recommended operating conditions with L/TV_{DD} of 3.3 V ± 5% and 2.5 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
RX_CLK clock period	t_{GRX}[3]	—	8.0	—	ns
RX_CLK duty cycle	t_{GRXH}/t_{GRX}	40	—	60	ns
RXD[7:0], RX_DV, RX_ER setup time to RX_CLK	t_{GRDVKH}	2.0	—	—	ns
RXD[7:0], RX_DV, RX_ER hold time to RX_CLK	t_{GRDXKH}	0.5	—	—	ns
RX_CLK clock rise time (20%-80%)	t_{GRXR}[2]	—	—	1.0	ns

8.2.4 TBI AC Timing Specifications

This section describes the TBI transmit and receive AC timing specifications.

8.2.4.1 TBI Transmit AC Timing Specifications

Table 32 provides the TBI transmit AC timing specifications.

Table 32. TBI Transmit AC Timing Specifications

At recommended operating conditions with L/TV_{DD} of 3.3 V ± 5% and 2.5 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
TCG[9:0] setup time GTX_CLK going high	t_{TTKHDV}	2.0	—	—	ns
TCG[9:0] hold time from GTX_CLK going high	t_{TTKHDX}	1.0	—	—	ns
GTX_CLK rise time (20%–80%)	t_{TTXR}[2]	—	—	1.0	ns
GTX_CLK fall time (80%–20%)	t_{TTXF}[2]	—	—	1.0	ns

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{TTKHDV} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the valid state (V) or setup time. Also, t_{TTKHDX} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the invalid state (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{TTX} represents the TBI (T) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Guaranteed by design.

Figure 16 shows the TBI transmit AC timing diagram.

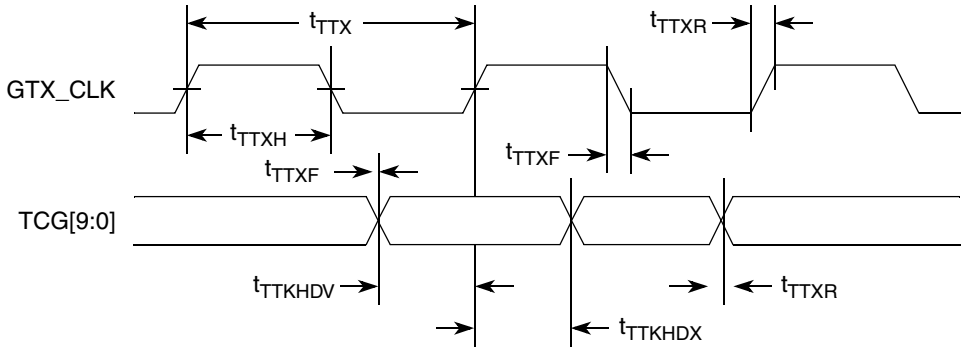


Figure 16. TBI Transmit AC Timing Diagram

8.2.7 RMII AC Timing Specifications

This section describes the RMII transmit and receive AC timing specifications.

8.2.7.1 RMII Transmit AC Timing Specifications

The RMII transmit AC timing specifications are in Table 36.

Table 36. RMII Transmit AC Timing Specifications

At recommended operating conditions with L/TV_{DD} of 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
REF_CLK clock period	t_{RMT}	—	20.0	—	ns
REF_CLK duty cycle	t_{RMTH}/t_{RMT}	35	50	65	%
REF_CLK peak-to-peak jitter	t_{RMTJ}	—	—	250	ps
Rise time REF_CLK (20%–80%)	t_{RMTR}	1.0	—	2.0	ns
Fall time REF_CLK (80%–20%)	t_{RMTF}	1.0	—	2.0	ns
REF_CLK to RMII data TXD[1:0], TX_EN delay	t_{RMTDX}	1.0	—	10.0	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 20 shows the RMII transmit AC timing diagram.

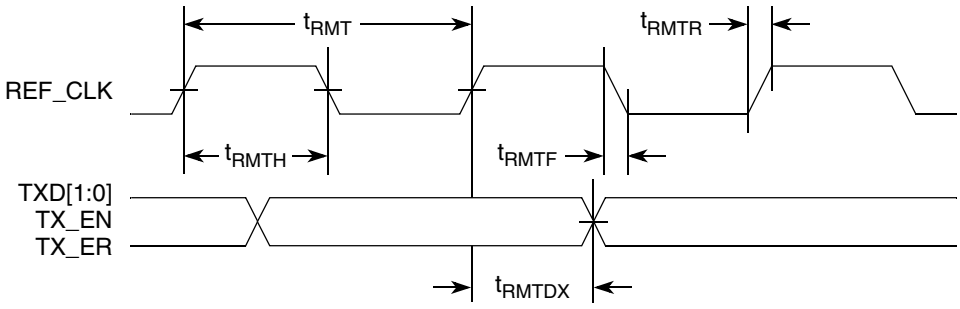


Figure 20. RMII Transmit AC Timing Diagram

Table 39. MII Management AC Timing Specifications (continued)

At recommended operating conditions with OV_{DD} is 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit	Notes
MDIO to MDC hold time	t_{MDDXKH}	0	—	—	ns	—
MDC rise time	t_{MDCR}	—	—	10	ns	4
MDC fall time	t_{MDHF}	—	—	10	ns	4

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. This parameter is dependent on the system clock speed. (The maximum frequency is the maximum platform frequency divided by 64.)
3. This parameter is dependent on the system clock speed. (That is, for a system clock of 267 MHz, the maximum frequency is 8.3 MHz and the minimum frequency is 1.2 MHz; for a system clock of 375 MHz, the maximum frequency is 11.7 MHz and the minimum frequency is 1.7 MHz.)
4. Guaranteed by design.
5. t_{MPXCLK} is the platform (MPX) clock

Figure 23 provides the AC test load for eTSEC.

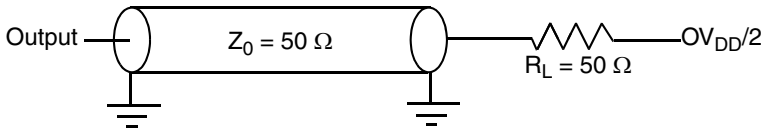


Figure 23. eTSEC AC Test Load

NOTE

Output will see a 50-Ω load since what it sees is the transmission line.

Figure 24 shows the MII management AC timing diagram.

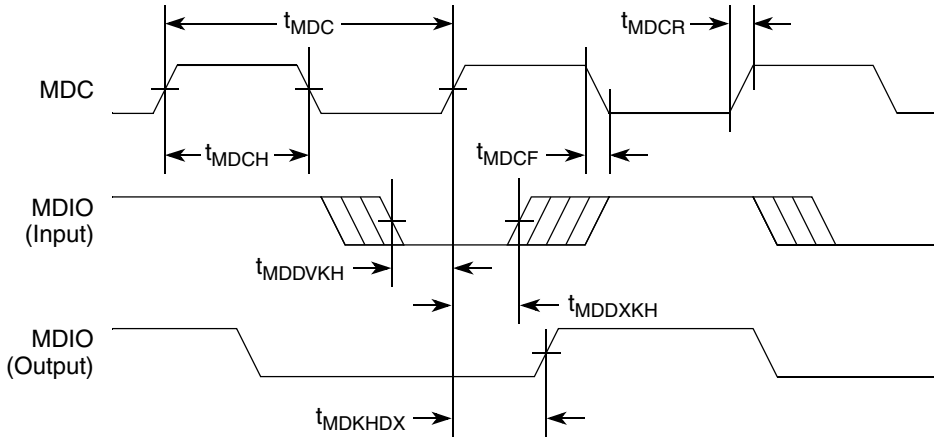


Figure 24. MII Management Interface Timing Diagram

Table 41. Local Bus Timing Parameters (OV_{DD} = 3.3 V)m - PLL Enabled (continued)

Parameter	Symbol [1]	Min	Max	Unit	Notes
Local bus clock to LALE assertion	$t_{LBKHOV4}$	—	2.3	ns	3
Output hold from local bus clock (except LAD/LDP and LALE)	$t_{LBKHOX1}$	0.7	—	ns	—
Output hold from local bus clock for LAD/LDP	$t_{LBKHOX2}$	0.7	—	ns	3
Local bus clock to output high Impedance (except LAD/LDP and LALE)	$t_{LBKHOZ1}$	—	2.5	ns	5
Local bus clock to output high impedance for LAD/LDP	$t_{LBKHOZ2}$	—	2.5	ns	5

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(First two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(First two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one(1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to LSYNC_IN for PLL enabled and internal local bus clock for PLL bypass mode.
3. All signals are measured from $OV_{DD}/2$ of the rising edge of LSYNC_IN for PLL enabled or internal local bus clock for PLL bypass mode to $0.4 \times OV_{DD}$ of the signal in question for 3.3-V signaling levels.
4. Input timings are measured at the pin.
5. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
6. t_{LBOTOT} is a measurement of the minimum time between the negation of LALE and any change in LAD. t_{LBOTOT} is programmed with the LBCR[AHD] parameter.
7. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at $BV_{DD}/2$.
8. Guaranteed by design.

Figure 25 provides the AC test load for the local bus.

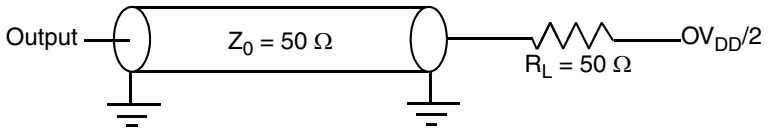


Figure 25. Local Bus AC Test Load

Table 45. I²C DC Electrical Characteristics (continued)

At recommended operating conditions with OV_{DD} of 3.3 V ± 5%.

Parameter	Symbol	Min	Max	Unit	Notes
Capacitance for each I/O pin	C_I	—	10	pF	—

Notes:
1. Output voltage (open drain or open collector) condition = 3 mA sink current.
2. Refer to the *MPC8641 Integrated Host Processor Reference Manual* for information on the digital filter used.
3. I/O pins will obstruct the SDA and SCL lines if OV_{DD} is switched off.

12.2 I²C AC Electrical Specifications

Table 46 provides the AC timing parameters for the I²C interfaces.

Table 46. I²C AC Electrical Specifications

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 45).

Parameter	Symbol [1]	Min	Max	Unit
SCL clock frequency	f_{I2C}	0	400	kHz
Low period of the SCL clock	t_{I2CL} [4]	1.3	—	μs
High period of the SCL clock	t_{I2CH} [4]	0.6	—	μs
Setup time for a repeated START condition	t_{I2SVKH} [4]	0.6	—	μs
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t_{I2SXKL} [4]	0.6	—	μs
Data setup time	t_{I2DVKH} [4]	100	—	ns
Data input hold time: CBUS compatible masters I²C bus devices	t_{I2DXKL}	 — 0 [2]	 — —	 μs
Rise time of both SDA and SCL signals	t_{I2CR}	$20 + 0.1\ C_B$ [5]	300	ns
Fall time of both SDA and SCL signals	t_{I2CF}	$20 + 0.1\ C_b$ [5]	300	ns
Data output delay time	t_{I2OVKL}	—	0.9 [3]	μs
Set-up time for STOP condition	t_{I2PVKH}	0.6	—	μs
Bus free time between a STOP and START condition	t_{I2KHDX}	1.3	—	μs
Noise margin at the LOW level for each connected device (including hysteresis)	V_{NL}	$0.1 \times OV_{DD}$	—	V

The Differential Input Voltage (or Swing) of the receiver, V_{ID}, is defined as the difference of the two complimentary input voltages: $V_{SDn\_RX} - V_{\overline{SDn\_RX}}$. The V_{ID} value can be either positive or negative.

4. **Differential Peak Voltage, V_{DIFFp}**

   The peak value of the differential transmitter output signal or the differential receiver input signal is defined as Differential Peak Voltage, $V_{DIFFp} = |A - B|$ Volts.

5. **Differential Peak-to-Peak, $V_{DIFFp-p}$**

   Since the differential output signal of the transmitter and the differential input signal of the receiver each range from A – B to –(A – B) Volts, the peak-to-peak value of the differential transmitter output signal or the differential receiver input signal is defined as Differential Peak-to-Peak Voltage, $V_{DIFFp-p} = 2*V_{DIFFp} = 2 * |(A - B)|$ Volts, which is twice of differential swing in amplitude, or twice of the differential peak. For example, the output differential peak-peak voltage can also be calculated as $V_{TX-DIFFp-p} = 2*|V_{OD}|$.

6. **Differential Waveform**

   The differential waveform is constructed by subtracting the inverting signal ($\overline{SDn\_TX}$, for example) from the non-inverting signal (SD*n*_TX, for example) within a differential pair. There is only one signal trace curve in a differential waveform. The voltage represented in the differential waveform is not referenced to ground. Refer to Figure 47 as an example for differential waveform.

7. **Common Mode Voltage, V_{cm}**

   The Common Mode Voltage is equal to one half of the sum of the voltages between each conductor of a balanced interchange circuit and ground. In this example, for SerDes output, $V_{cm\_out} = (V_{SDn\_TX} + V_{\overline{SDn\_TX}})/2 = (A + B) / 2$, which is the arithmetic mean of the two complimentary output voltages within a differential pair. In a system, the common mode voltage may often differ from one component's output to the other's input. Sometimes, it may be even different between the receiver input and driver output circuits within the same component. It is also referred as the DC offset in some occasion.

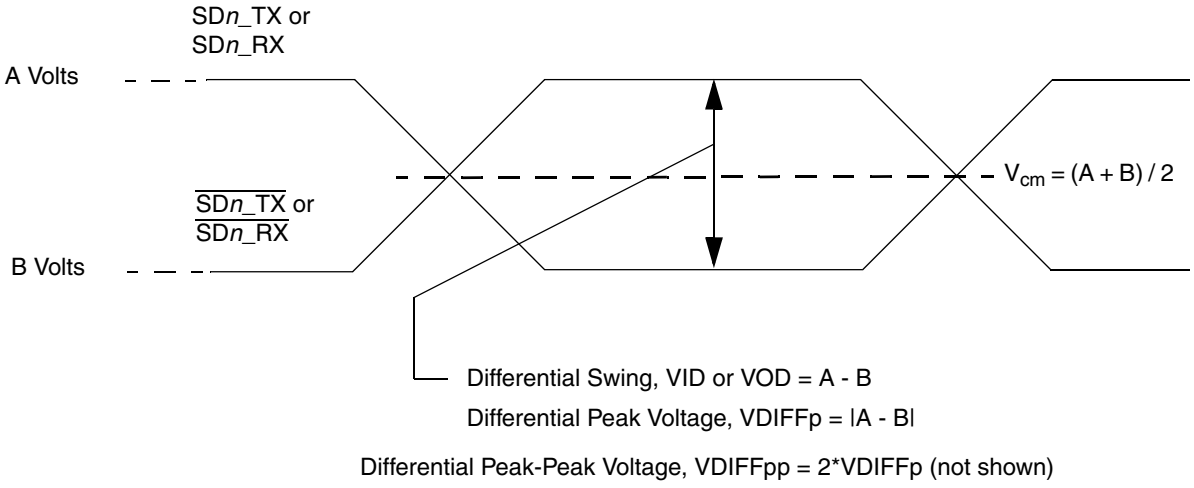


Figure 38. Differential Voltage Definitions for Transmitter or Receiver

- The input amplitude requirement
  - This requirement is described in detail in the following sections.

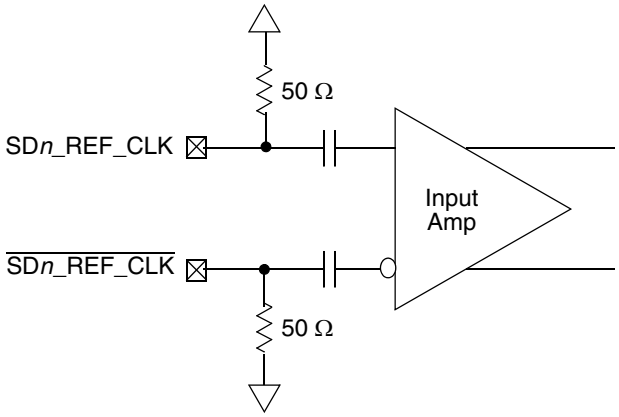


Figure 39. Receiver of SerDes Reference Clocks

13.2.2 DC Level Requirement for SerDes Reference Clocks

The DC level requirement for the MPC8641D SerDes reference clock inputs is different depending on the signaling mode used to connect the clock driver chip and SerDes reference clock inputs as described below.

- **Differential Mode**
  - The input amplitude of the differential clock must be between 400 mV and 1600 mV differential peak-peak (or between 200 mV and 800 mV differential peak). In other words, each signal wire of the differential pair must have a single-ended swing less than 800mV and greater than 200 mV. This requirement is the same for both external DC-coupled or AC-coupled connection.
  - For **external DC-coupled** connection, as described in Section 13.2.1, "SerDes Reference Clock Receiver Characteristics," the maximum average current requirements sets the requirement for average voltage (common mode voltage) to be between 100 mV and 400 mV. Figure 40 shows the SerDes reference clock input requirement for DC-coupled connection scheme.
  - For **external AC-coupled** connection, there is no common mode voltage requirement for the clock driver. Since the external AC-coupling capacitor blocks the DC level, the clock driver and the SerDes reference clock receiver operate in different command mode voltages. The SerDes reference clock receiver in this connection scheme has its common mode voltage set to SGND. Each signal wire of the differential inputs is allowed to swing below and above the command mode voltage (SGND). Figure 41 shows the SerDes reference clock input requirement for AC-coupled connection scheme.
- **Single-ended Mode**
  - The reference clock can also be single-ended. The SD*n*_REF_CLK input amplitude (single-ended swing) must be between 400 mV and 800 mV peak-peak (from Vmin to Vmax) with $\overline{\text{SD}n\text{\_REF\_CLK}}$ either left unconnected or tied to ground.

Table 49. Differential Transmitter (TX) Output Specifications (continued)

Symbol	Parameter	Min	Nom	Max	Units	Comments
T_{TX-EYE}	Minimum TX Eye Width	0.70	—	—	UI	The maximum Transmitter jitter can be derived as $T_{TX-MAX-JITTER}$ = 1 – T_{TX-EYE}= 0.3 UI. See Notes 2 and 3.
$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time between the jitter median and maximum deviation from the median.	—	—	0.15	UI	Jitter is defined as the measurement variation of the crossing points ($V_{TX-DIFFp-p}$ = 0 V) in relation to a recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI. See Notes 2 and 3.
$T_{TX-RISE}$, $T_{TX-FALL}$	D+/D– TX Output Rise/Fall Time	0.125	—	—	UI	See Notes 2 and 5
$V_{TX-CM-ACp}$	RMS AC Peak Common Mode Output Voltage	—	—	20	mV	$V_{TX-CM-ACp}$ = RMS(|V_{TXD+} + V_{TXD-}|/2 – $V_{TX-CM-DC}$) $V_{TX-CM-DC}$ = $DC_{(avg)}$ of |V_{TX-D+} + V_{TX-D-}|/2 See Note 2
$V_{TX-CM-DC-ACTIVE-IDLE-DELTA}$	Absolute Delta of DC Common Mode Voltage During L0 and Electrical Idle	0	—	100	mV	|$V_{TX-CM-DC\ (during\ L0)}$ – $V_{TX-CM-Idle-DC\ (During\ Electrical\ Idle)}$|<=100 mV $V_{TX-CM-DC}$ = $DC_{(avg)}$ of |V_{TX-D+} + V_{TX-D-}|/2 [L0] $V_{TX-CM-Idle-DC}$ = $DC_{(avg)}$ of |V_{TX-D+} + V_{TX-D-}|/2 [Electrical Idle] See Note 2.
$V_{TX-CM-DC-LINE-DELTA}$	Absolute Delta of DC Common Mode between D+ and D–	0	—	25	mV	|$V_{TX-CM-DC-D+}$ – $V_{TX-CM-DC-D-}$| <= 25 mV $V_{TX-CM-DC-D+}$ = $DC_{(avg)}$ of |V_{TX-D+}| $V_{TX-CM-DC-D-}$ = $DC_{(avg)}$ of |V_{TX-D-}| See Note 2.
$V_{TX-IDLE-DIFFp}$	Electrical Idle differential Peak Output Voltage	0	—	20	mV	$V_{TX-IDLE-DIFFp}$ = |$V_{TX-IDLE-D+}$ –$V_{TX-IDLE-D-}$| <= 20 mV See Note 2.
$V_{TX-RCV-DETECT}$	The amount of voltage change allowed during Receiver Detection	—	—	600	mV	The total amount of voltage change that a transmitter can apply to sense whether a low impedance Receiver is present. See Note 6.
$V_{TX-DC-CM}$	The TX DC Common Mode Voltage	0	—	3.6	V	The allowed DC Common Mode voltage under any conditions. See Note 6.
$I_{TX-SHORT}$	TX Short Circuit Current Limit	—	—	90	mA	The total current the Transmitter can provide when shorted to its ground
$T_{TX-IDLE-MIN}$	Minimum time spent in Electrical Idle	50	—	—	UI	Minimum time a Transmitter must be in Electrical Idle Utilized by the Receiver to start looking for an Electrical Idle Exit after successfully receiving an Electrical Idle ordered set

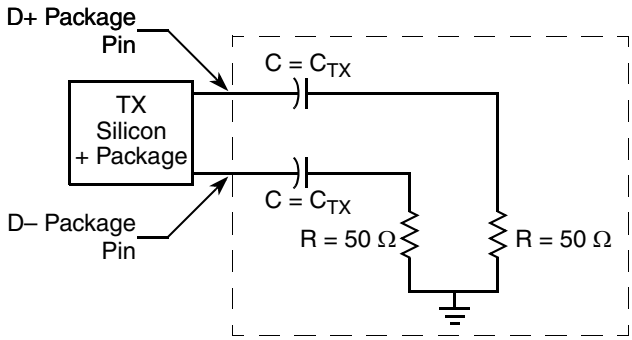


Figure 52. Compliance Test/Measurement Load

15 Serial RapidIO

This section describes the DC and AC electrical specifications for the RapidIO interface of the MPC8641, for the LP-Serial physical layer. The electrical specifications cover both single and multiple-lane links. Two transmitter types (short run and long run) on a single receiver are specified for each of three baud rates, 1.25, 2.50, and 3.125 GBaud.

Two transmitter specifications allow for solutions ranging from simple board-to-board interconnect to driving two connectors across a backplane. A single receiver specification is given that will accept signals from both the short run and long run transmitter specifications.

The short run transmitter specifications should be used mainly for chip-to-chip connections on either the same printed circuit board or across a single connector. This covers the case where connections are made to a mezzanine (daughter) card. The minimum swings of the short run specification reduce the overall power used by the transceivers.

The long run transmitter specifications use larger voltage swings that are capable of driving signals across backplanes. This allows a user to drive signals across two connectors and a backplane. The specifications allow a distance of at least 50 cm at all baud rates.

All unit intervals are specified with a tolerance of +/– 100 ppm. The worst case frequency difference between any transmit and receive clock will be 200 ppm.

To ensure interoperability between drivers and receivers of different vendors and technologies, AC coupling at the receiver input must be used.

15.1 DC Requirements for Serial RapidIO SD*n*_REF_CLK and SD*n*_REF_CLK

For more information, see Section 13.2, “SerDes Reference Clocks.”

15.2 AC Requirements for Serial RapidIO SD*n*_REF_CLK and SD*n*_REF_CLK

Table 51 lists AC requirements.

Table 63. MPC8641 Signal Reference by Functional Block (continued)

Name[1]	Package Pin Number	Pin Type	Power Supply	Notes
TSEC3_TXD[6:7]/ cfg_tsec3_prtcl[0:1]	AL20, AL19	—	LV_{DD}	—
TSEC4_TXD[0:3]/ cfg_io_ports[0:3]	AC18, AC16, AD18, AD17	—	LV_{DD}	—
TSEC4_TXD[5]/ cfg_tsec4_reduce	AB18	—	LV_{DD}	—
TSEC4_TXD[6:7]/ cfg_tsec4_prtcl[0:1]	AB17, AB16	—	LV_{DD}	—
LAD[0:31]/ cfg_gpporcr[0:31]	A30, E29, C29, D28, D29, H25, B29, A29, C28, L22, M22, A28, C27, H26, G26, B27, B26, A27, E27, G25, D26, E26, G24, F27, A26, A25, C25, H23, K22, D25, F25, H22	—	OV_{DD}	—
$\overline{\text{LWE[0]}}$/ cfg_cpu_boot	E21	—	OV_{DD}	—
$\overline{\text{LWE[1]}}$/ cfg_rio_sys_size	F21	—	OV_{DD}	—
$\overline{\text{LWE[2:3]}}$/ cfg_host_agt[0:1]	D22, E20	—	OV_{DD}	—
LDP[0:3], LA[27] / cfg_core_pll[0:4]	A24, E24, C24, B24, J21	—	OV_{DD}	22
LA[28:31]/ cfg_sys_pll[0:3]	K21, G22, F24, G21	—	OV_{DD}	22
LGPL[3], LGPL[5]/ cfg_boot_seq[0:1]	K20, J19	—	OV_{DD}	—
D1_MSRCID[0]/ cfg_mem_debug	F15	—	OV_{DD}	—
D1_MSRCID[1]/ cfg_ddr_debug	K15	—	OV_{DD}	—

- Binary value on LA[28:31] at power up

Note that there is no default for this PLL ratio; these signals must be pulled to the desired values. Also note that the DDR data rate is the determining factor in selecting the MPX bus frequency, since the MPX frequency must equal the DDR data rate.

Table 68. MPX:SYSCLK Ratio

Binary Value of LA[28:31] Signals	MPX:SYSCLK Ratio
0000	Reserved
0001	Reserved
0010	2:1
0011	3:1
0100	4:1
0101	5:1
0110	6:1
0111	Reserved
1000	8:1
1001	9:1

18.3 e600 to MPX clock PLL Ratio

Table 69 describes the clock ratio between the platform and the e600 core clock. This ratio is determined by the binary value of LDP[0:3], LA[27](cfg_core_pll[0:4] - reset config name) at power up, as shown in Table 69.

Table 69. e600 Core to MPX Clock Ratio

Binary Value of LDP[0:3], LA[27] Signals	e600 core: MPX Clock Ratio
01000	2:1
01100	2.5:1
10000	3:1
11100	3.5:1
10100	4:1
01110	4.5:1

18.4 Frequency Options

Conductivity	Value	Unit
Die (12.4x15.3x0.86 mm)		
Silicon	Temperature dependent	
Bump and Underfill (12.4 × 15.3 × 0.07 mm) Collapsed Resistance		
k_z	5.3	W/(m • K)
Substrate (33 × 33 × 1.2 mm)		
k_x	13.5	W/(m • K)
k_y	13.5	
k_z	5.3	
C5 Solder layer (33 × 33 × 0.4 mm)		
k_x	0.034	W/(m • K)
k_y	0.034	
k_z	9.6	

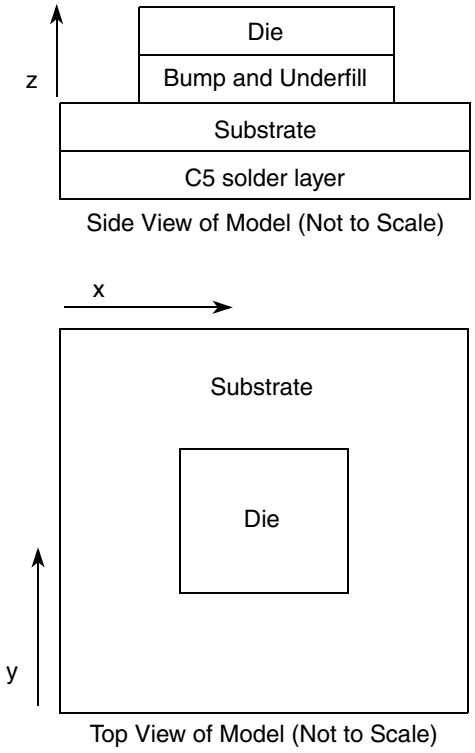


Figure 62. Recommended Thermal Model of MPC8641

19.2.4 Temperature Diode

The MPC8641 has a temperature diode on the microprocessor that can be used in conjunction with other system temperature monitoring devices (such as Analog Devices, ADT7461™). These devices use the negative temperature coefficient of a diode operated at a constant current to determine the temperature of the microprocessor and its environment. It is recommended that each device be individually calibrated.

The following are the specifications of the MPC8641 on-board temperature diode:

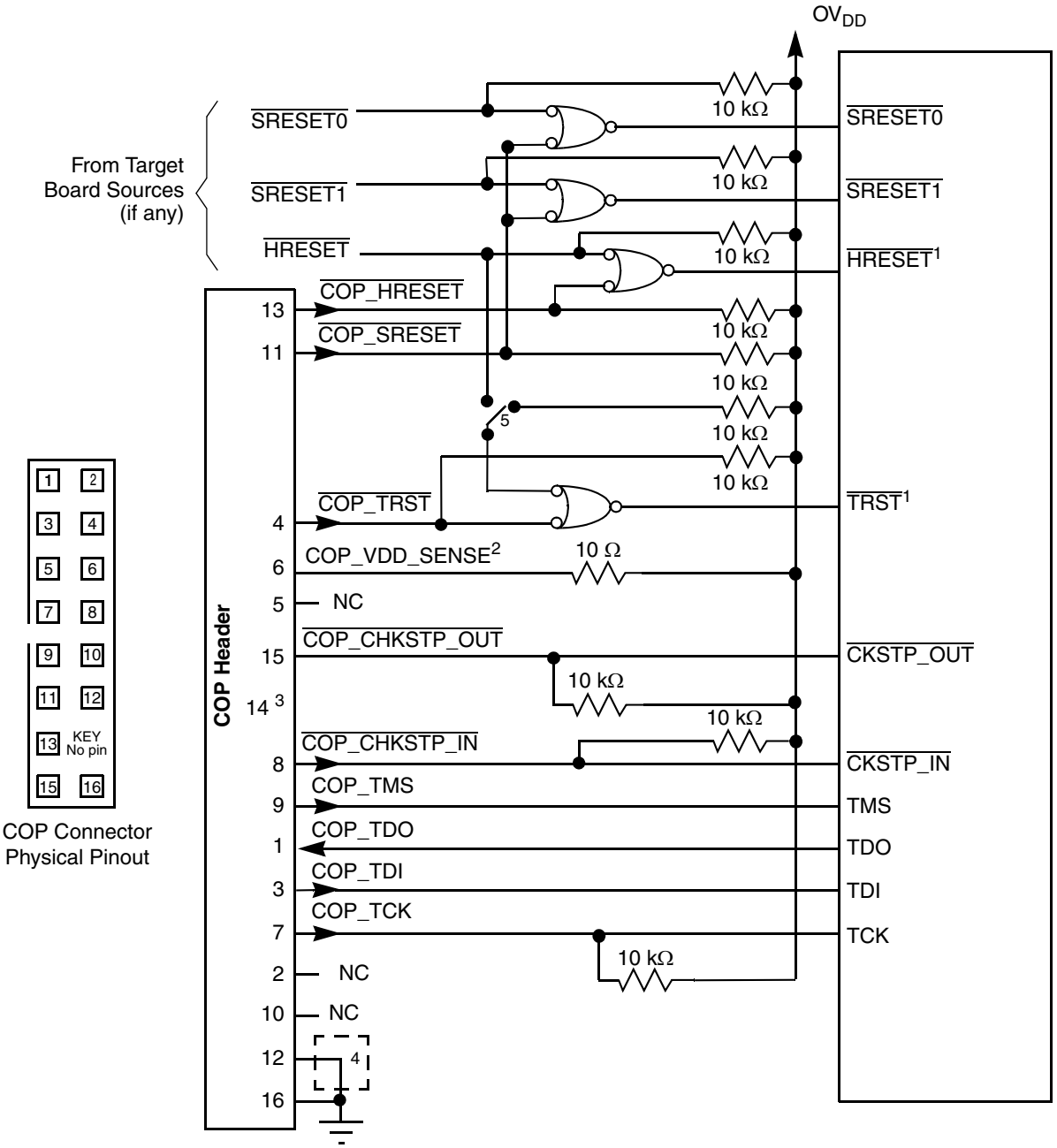
$V_f > 0.40$ V

$V_f < 0.90$ V

An approximate value of the ideality may be obtained by calibrating the device near the expected operating temperature.

Ideality factor is defined as the deviation from the ideal diode equation:

$$I_{fw} = I_s \left[e^{\frac{qV_f}{nKT}} - 1 \right]$$



Notes:

1. The COP port and target board should be able to independently assert $\overline{\text{HRESET}}$ and $\overline{\text{TRST}}$ to the processor in order to fully control the processor as shown here.
2. Populate this with a 10 Ω resistor for short-circuit/current-limiting protection.
3. The KEY location (pin 14) is not physically present on the COP header.
4. Although pin 12 is defined as a No-Connect, some debug tools may use pin 12 as an additional GND pin for improved signal integrity.
5. This switch is included as a precaution for BSDL testing. The switch should be open during BSDL testing to avoid accidentally asserting the $\overline{\text{TRST}}$ line. If BSDL testing is not being performed, this switch should be closed or removed.

Figure 68. JTAG/COP Interface Connection for one MPC8641 device

21 Ordering Information

Ordering information for the parts fully covered by this specification document is provided in Section 21.1, "Part Numbers Fully Addressed by This Document."

21.1 Part Numbers Fully Addressed by This Document

Table 74 provides the Freescale part numbering nomenclature for the MPC8641. Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Freescale sales office. In addition to the processor frequency, the part numbering scheme also includes an application modifier which may specify special application conditions. Each part number also contains a revision code which refers to the die mask revision number.

Table 74. Part Numbering Nomenclature

MC	nnnn	x	xx	nnnn	x	x
Product Code	**Part Identifier**	**Core Count**	**Package [1]**	**Core Processor Frequency [2] (MHz)**	**DDR speed (MHz)**	**Product Revision Level**
MC	8641	Blank = Single Core D = Dual Core	HX = High-lead HCTE FC-CBGA VU = RoHS lead-free HCTE FC-CBGA[5] VJ = lead-free HCTE FC-CBGA[6]	1000, 1250, 1333, 1500	N = 500 MHz[4] K = 600 MHz J = 533 MHz H = 500 MHz G = 400 MHz	Revision B = 2.0 System Version Register Value for Rev B: 0x8090_0020 - MPC8641 0x8090_0120 - MPC8641D Revision C = 2.1 System Version Register Value for Rev C: 0x8090_0021 - MPC8641 0x8090_0121 - MPC8641D Revision E = 3.0 System Version Register Value for Rev E: 0x8090_0030 - MPC8641 0x8090_0130 - MPC8641D

Notes:

1. See Section 16, "Package," for more information on available package types.
2. Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by part number specifications may support other maximum core frequencies.
3. The P prefix in a Freescale part number designates a "Pilot Production Prototype" as defined by Freescale SOP 3-13. These parts have only preliminary reliability and characterization data. Before pilot production prototypes may be shipped, written authorization from the customer must be on file in the applicable sales office acknowledging the qualification status and the fact that product changes may still occur while shipping pilot production prototypes.
4. Part Number MC8641xxx1000NX is our low V_{DD}_Core*n* device. V_{DD}_Core*n* = 0.95 V and V_{DD}_PLAT = 1.05 V.
5. VU part number is RoHS compliant with the permitted exception of the C4 die bumps.
6. VJ part number is entirely lead-free including the C4 die bumps.

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