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Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e600
Number of Cores/Bus Width	2 Core, 32-Bit
Speed	1.5GHz
Co-Processors/DSP	-
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (4)
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	1023-BBGA, FCBGA
Supplier Device Package	1023-FCCBGA (33x33)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc8641dhx1500kb

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8 Ethernet: Enhanced Three-Speed Ethernet (eTSEC), MII Management

This section provides the AC and DC electrical characteristics for enhanced three-speed and MII management.

8.1 Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1Gb Mbps)—GMII/MII/TBI/RGMII/RTBI/RMII Electrical Characteristics

The electrical characteristics specified here apply to all gigabit media independent interface (GMII), media independent interface (MII), ten-bit interface (TBI), reduced gigabit media independent interface (RGMII), reduced ten-bit interface (RTBI), and reduced media independent interface (RMII) signals except management data input/output (MDIO) and management data clock (MDC). The RGMII and RTBI interfaces are defined for 2.5 V, while the GMII and TBI interfaces can be operated at 3.3 or 2.5 V. Whether the GMII or TBI interface is operated at 3.3 or 2.5 V, the timing is compatible with IEEE 802.3. The RGMII and RTBI interfaces follow the Reduced Gigabit Media-Independent Interface (RGMII) Specification Version 1.3 (12/10/2000). The RMII interface follows the RMII Consortium RMII Specification Version 1.2 (3/20/1998). The electrical characteristics for MDIO and MDC are specified in Section 9, "Ethernet Management Interface Electrical Characteristics."

8.1.1 eTSEC DC Electrical Characteristics

All GMII, MII, TBI, RGMII, RMII and RTBI drivers and receivers comply with the DC parametric attributes specified in Table 24 and Table 25. The potential applied to the input of a GMII, MII, TBI, RGMII, RMII or RTBI receiver may exceed the potential of the receiver's power supply (that is, a GMII driver powered from a 3.6-V supply driving V_{OH} into a GMII receiver powered from a 2.5-V supply). Tolerance for dissimilar GMII driver and receiver supply potentials is implicit in these specifications. The RGMII and RTBI signals are based on a 2.5-V CMOS interface voltage as defined by JEDEC EIA/JESD8-5.

Parameter	Symbol	Min	Мах	Unit	Notes
Supply voltage 3.3 V	LV _{DD} TV _{DD}	3.135	3.465	V	1, 2
Output high voltage $(LV_{DD}/TV_{DD} = Min, I_{OH} = -4.0 \text{ mA})$	V _{OH}	2.40	_	V	—
Output low voltage $(LV_{DD}/TV_{DD} = Min, I_{OL} = 4.0 \text{ mA})$	V _{OL}	_	0.50	V	_
Input high voltage	V _{IH}	2.0	—	V	_
Input low voltage	V _{IL}	—	0.90	V	_
Input high current $(V_{IN} = LV_{DD}, V_{IN} = TV_{DD})$	IIH	_	40	μA	1, 2,3

Table 24. GMII, MII, RMII, TBI and FIFO DC Electrical Characteristics



8.2.4 TBI AC Timing Specifications

This section describes the TBI transmit and receive AC timing specifications.

8.2.4.1 TBI Transmit AC Timing Specifications

Table 32 provides the TBI transmit AC timing specifications.

Table 32. TBI Transmit AC Timing Specifications

At recommended operating conditions with L/TV_{DD} of 3.3 V \pm 5% and 2.5 V \pm 5%.

Parameter/Condition	Symbol ¹	Min	Тур	Мах	Unit
TCG[9:0] setup time GTX_CLK going high	t _{TTKHDV}	2.0	—	—	ns
TCG[9:0] hold time from GTX_CLK going high	t _{TTKHDX}	1.0	—	—	ns
GTX_CLK rise time (20%-80%)	t _{TTXR} ²	—	—	1.0	ns
GTX_CLK fall time (80%–20%)	t _{TTXF} 2	—	—	1.0	ns

Notes:

1. The symbols used for timing specifications herein follow the pattern of t_{(first two letters of functional block)(signal)(state)(reference)(state)} for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{TTKHDV} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the valid state (V) or setup time. Also, t_{TTKHDX} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the valid state (V) or setup time. Also, t_{TTKHDX} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the invalid state (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{TTX} represents the TBI (T) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

2. Guaranteed by design.

Figure 16 shows the TBI transmit AC timing diagram.



Figure 16. TBI Transmit AC Timing Diagram



8.2.5 TBI Single-Clock Mode AC Specifications

When the eTSEC is configured for TBI modes, all clocks are supplied from external sources to the relevant eTSEC interface. In single-clock TBI mode, when TBICON[CLKSEL] = 1 a 125-MHz TBI receive clock is supplied on TSEC n_RX_CLK pin (no receive clock is used on TSEC n_TX_CLK in this mode, whereas for the dual-clock mode this is the PMA1 receive clock). The 125-MHz transmit clock is applied on the TSEC GTX CLK125 pin in all TBI modes.

A summary of the single-clock TBI mode AC specifications for receive appears in Table 34.

Table 34. TBI single-clock Mode Receive AC Timing Specification

At recommended operating conditions with L/TV_{DD} of 3.3 V \pm 5% and 2.5 V \pm 5%.

Parameter/Condition	Symbol	Min	Тур	Max	Unit
RX_CLK clock period	t _{TRR} ¹	7.5	8.0	8.5	ns
RX_CLK duty cycle	t _{TRRH/} t _{TRR}	40	50	60	%
RX_CLK peak-to-peak jitter	t _{TRRJ}		—	250	ps
Rise time RX_CLK (20%–80%)	t _{TRRR}	-	—	1.0	ns
Fall time RX_CLK (80%–20%)	t _{TRRF}	_	—	1.0	ns
RCG[9:0] setup time to RX_CLK rising edge	t _{TRRDVKH}	2.0	—	—	ns
RCG[9:0] hold time to RX_CLK rising edge	t _{TRRDXKH}	1.0	_	_	ns

¹ ±100 ppm tolerance on RX_CLK frequency

A timing diagram for TBI receive appears in Figure 18.



Figure 18. TBI Single-Clock Mode Receive AC Timing Diagram

8.2.6 RGMII and RTBI AC Timing Specifications

Table 35 presents the RGMII and RTBI AC timing specifications.

Table 35. RGMII and RTBI AC Timing Specifications

At recommended operating conditions with L/TV_{DD} of 2.5 V ± 5%.

Parameter/Condition	Symbol ¹	Min	Тур	Мах	Unit
Data to clock output skew (at transmitter)	t _{SKRGT} ⁵	-500	0	500	ps
Data to clock input skew (at receiver) ²	t _{SKRGT}	1.0		2.8	ns



Ethernet: Enhanced Three-Speed Ethernet (eTSEC), MII Management

Table 35. RGMII and RTBI AC Timing Specifications (continued)

At recommended operating conditions with L/TV_{DD} of 2.5 V \pm 5%.

Parameter/Condition	Symbol ¹	Min	Тур	Мах	Unit
Clock period duration ³	t _{RGT} ^{5,6}	7.2	8.0	8.8	ns
Duty cycle for 10BASE-T and 100BASE-TX $^{3, 4}$	t _{RGTH} /t _{RGT} 5	40	50	60	%
Rise time (20%–80%)	t _{RGTR} 5	—	-	0.75	ns
Fall time (80%-20%)	t _{RGTF} 5	—		0.75	ns

Notes:

1. Note that, in general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII and RTBI timing. For example, the subscript of t_{RGT} represents the TBI (T) receive (RX) clock. Note also that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).

- 2. This implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 1.5 ns will be added to the associated clock signal.
- 3. For 10 and 100 Mbps, t_{RGT} scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
- 4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned between.
- 5. Guaranteed by characterization
- 6. ±100 ppm tolerance on RX_CLK frequency

Figure 19 shows the RGMII and RTBI AC timing and multiplexing diagrams.



Figure 19. RGMII and RTBI AC Timing and Multiplexing Diagrams



Figure 26 to Figure 31 show the local bus signals.



Figure 26. Local Bus Signals (PLL Enabled)

NOTE

PLL bypass mode is recommended when LBIU frequency is at or below 83 MHz. When LBIU operates above 83 MHz, LBIU PLL is recommended to be enabled.

Table 42 describes the general timing parameters of the local bus interface at $OV_{DD} = 3.3$ V with PLL bypassed.

Table 42. Local Bus	Timing Parameters—F	LL Bypassed
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Parameter	Symbol ¹	Min	Мах	Unit	Notes
Local bus cycle time	t _{LBK}	12	_	ns	2
Local bus duty cycle	t _{LBKH/} t _{LBK}	45	55	%	—
Internal launch/capture clock to LCLK delay	t _{LBKHKT}	2.3	3.9	ns	8
Input setup to local bus clock (except LGTA/LUPWAIT)	t _{LBIVKH1}	5.7	_	ns	4, 5
LGTA/LUPWAIT input setup to local bus clock	t _{LBIVKL2}	5.6	_	ns	4, 5
Input hold from local bus clock (except LGTA/LUPWAIT)	t _{LBIXKH1}	-1.8	_	ns	4, 5



Local Bus



Figure 27. Local Bus Signals (PLL Bypass Mode)

NOTE

In PLL bypass mode, LCLK[n] is the inverted version of the internal clock with the delay of t_{LBKHKT} . In this mode, signals are launched at the rising edge of the internal clock and are captured at falling edge of the internal clock, with the exception of the LGTA/LUPWAIT signal, which is captured at the rising edge of the internal clock.



Local Bus



Figure 30. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 4 or 8 (clock ratio of 8 or 16) (PLL Enabled)



Table 44. JTAG AC Timing Specifications (Independent of SYSCLK)¹ (continued)

At recommended operating conditions (see Table 3).

Parameter	Symbol ²	Min	Мах	Unit	Notes
Output hold times: Boundary-scan data TDO	t _{JTKLDX} t _{JTKLOX}	30 30		ns	5, 6
JTAG external clock to output high impedance: Boundary-scan data TDO	t _{jtkldz} t _{jtkloz}	3 3	19 9	ns	5, 6

Notes:

- All outputs are measured from the midpoint voltage of the falling/rising edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 32). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
- 2. The symbols used for timing specifications herein follow the pattern of t_{(first two letters of functional block)(signal)(state) (reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).}
- 3. TRST is an asynchronous level sensitive signal. The setup time is for test purposes only.
- 4. Non-JTAG signal input timing with respect to t_{TCLK} .
- 5. Non-JTAG signal output timing with respect to t_{TCLK}.
- 6. Guaranteed by design.

Figure 32 provides the AC test load for TDO and the boundary-scan outputs.



Figure 32. AC Test Load for the JTAG Interface

Figure 33 provides the JTAG clock input timing diagram.



VM = Midpoint Voltage (OV_{DD}/2)

Figure 33. JTAG Clock Input Timing Diagram

High-Speed Serial Interfaces (HSSI)

The Differential Input Voltage (or Swing) of the receiver, V_{ID} , is defined as the difference of the two complimentary input voltages: $V_{SDn_RX} - V_{\overline{SDn_RX}}$. The V_{ID} value can be either positive or negative.

4. Differential Peak Voltage, VDIFFp

The peak value of the differential transmitter output signal or the differential receiver input signal is defined as Differential Peak Voltage, $V_{DIFFp} = |A - B|$ Volts.

5. Differential Peak-to-Peak, VDIFFp-p

Since the differential output signal of the transmitter and the differential input signal of the receiver each range from A – B to –(A – B) Volts, the peak-to-peak value of the differential transmitter output signal or the differential receiver input signal is defined as Differential Peak-to-Peak Voltage, $V_{DIFFp-p} = 2*V_{DIFFp} = 2*|(A – B)|$ Volts, which is twice of differential swing in amplitude, or twice of the differential peak. For example, the output differential peak-peak voltage can also be calculated as $V_{TX-DIFFp-p} = 2*|V_{OD}|$.

6. Differential Waveform

The differential waveform is constructed by subtracting the inverting signal ($\overline{\text{SD}n_{TX}}$, for example) from the non-inverting signal ($\overline{\text{SD}n_{TX}}$, for example) within a differential pair. There is only one signal trace curve in a differential waveform. The voltage represented in the differential waveform is not referenced to ground. Refer to Figure 47 as an example for differential waveform.

7. Common Mode Voltage, V_{cm}

The Common Mode Voltage is equal to one half of the sum of the voltages between each conductor of a balanced interchange circuit and ground. In this example, for SerDes output, $V_{cm_out} = (V_{SDn_TX} + V_{\overline{SDn_TX}})/2 = (A + B) / 2$, which is the arithmetic mean of the two complimentary output voltages within a differential pair. In a system, the common mode voltage may often differ from one component's output to the other's input. Sometimes, it may be even different between the receiver input and driver output circuits within the same component. It is also referred as the DC offset in some occasion.



Figure 38. Differential Voltage Definitions for Transmitter or Receiver



PCI Express

Table 49. Differential Transmitter	(TX) Output Spe	ecifications (continued)
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Symbol	Parameter	Min	Nom	Мах	Units	Comments
T _{TX-IDLE-SET-TO-IDLE}	Maximum time to transition to a valid Electrical idle after sending an Electrical Idle ordered set		_	20	UI	After sending an Electrical Idle ordered set, the Transmitter must meet all Electrical Idle Specifications within this time. This is considered a debounce time for the Transmitter to meet Electrical Idle after transitioning from L0.
T _{TX-IDLE-TO-DIFF-DATA}	Maximum time to transition to valid TX specifications after leaving an Electrical idle condition			20	UI	Maximum time to meet all TX specifications when transitioning from Electrical Idle to sending differential data. This is considered a debounce time for the TX to meet all TX specifications after leaving Electrical Idle
RL _{TX-DIFF}	Differential Return Loss	12	—	—	dB	Measured over 50 MHz to 1.25 GHz. See Note 4
RL _{TX-CM}	Common Mode Return Loss	6	—	—	dB	Measured over 50 MHz to 1.25 GHz. See Note 4
Z _{TX-DIFF-DC}	DC Differential TX Impedance	80	100	120	Ω	TX DC Differential mode Low Impedance
Z _{TX-DC}	Transmitter DC Impedance	40	—	—	Ω	Required TX D+ as well as D- DC Impedance during all states
L _{TX-SKEW}	Lane-to-Lane Output Skew	_	—	500 + 2 UI	ps	Static skew between any two Transmitter Lanes within a single Link
C _{TX}	AC Coupling Capacitor	75	—	—	nF	All Transmitters shall be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. See Note 8.
T _{crosslink}	Crosslink Random Timeout	0			ms	This random timeout helps resolve conflicts in crosslink configuration by eventually resulting in only one Downstream and one Upstream Port. See Note 7.

Notes:

1. No test load is necessarily associated with this value.

- 2. Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 52 and measured over any 250 consecutive TX UIs. (Also refer to the transmitter compliance eye diagram shown in Figure 50)
- 3. A T_{TX-EYE} = 0.70 UI provides for a total sum of deterministic and random jitter budget of T_{TX-JITTER-MAX} = 0.30 UI for the Transmitter collected over any 250 consecutive TX UIs. The T_{TX-EYE-MEDIAN-to-MAX-JITTER} median is less than half of the total TX jitter budget collected over any 250 consecutive TX UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.
- 4. The Transmitter input impedance shall result in a differential return loss greater than or equal to 12 dB and a common mode return loss greater than or equal to 6 dB over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements is 50 Ω to ground for both the D+ and D- line (that is, as measured by a Vector Network Analyzer with 50 ohm probes—see Figure 52). Note that the series capacitors C_{TX} is optional for the return loss measurement.
- 5. Measured between 20-80% at transmitter package pins into a test load as shown in Figure 52 for both V_{TX-D+} and V_{TX-D-} .
- 6. See Section 4.3.1.8 of the PCI Express Base Specifications Rev 1.0a
- 7. See Section 4.2.6.3 of the PCI Express Base Specifications Rev 1.0a
- 8. MPC8641D SerDes transmitter does not have C_{TX} built-in. An external AC Coupling capacitor is required.



Transmitter Type	V _{DIFF} min (mV)	V _{DIFF} max (mV)	A (UI)	B (UI)
1.25 GBaud short range	250	500	0.175	0.39
1.25 GBaud long range	400	800	0.175	0.39
2.5 GBaud short range	250	500	0.175	0.39
2.5 GBaud long range	400	800	0.175	0.39
3.125 GBaud short range	250	500	0.175	0.39
3.125 GBaud long range	400	800	0.175	0.39

Table 58. Transmitter Differential Output Eye Diagram Parameters

15.7 Receiver Specifications

LP-Serial receiver electrical and timing specifications are stated in the text and tables of this section.

Receiver input impedance shall result in a differential return loss better that 10 dB and a common mode return loss better than 6 dB from 100 MHz to (0.8)*(Baud Frequency). This includes contributions from on-chip circuitry, the chip package and any off-chip components related to the receiver. AC coupling components are included in this requirement. The reference impedance for return loss measurements is 100 Ohm resistive for differential return loss and 25 Ohm resistive for common mode.

Characteristic	Symbol	Range		Unit	Notoo	
Characteristic	Min Max		Unit	notes		
Differential Input Voltage	V _{IN}	200	1600	mV p-p	Measured at receiver	
Deterministic Jitter Tolerance	J _D	0.37	—	UI p-p	Measured at receiver	
Combined Deterministic and Random Jitter Tolerance	J _{DR}	0.55	_	UI p-p	Measured at receiver	
Total Jitter Tolerance ¹	J _T	0.65	—	UI p-p	Measured at receiver	
Multiple Input Skew	S _{MI}	—	24	ns	Skew at the receiver input between lanes of a multilane link	
Bit Error Rate	BER	—	10 ⁻¹²	—	—	
Unit Interval	UI	800	800	ps	+/- 100 ppm	

Table 59. Receiver AC Timing Specifications—1.25 GBaud

Note:

1. Total jitter is composed of three components, deterministic jitter, random jitter and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 55. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects.



17 Signal Listings

Table 63 provides the pin assignments for the signals. Notes for the signal changes on the single core device (MPC8641) are italicized and prefixed by "*S*".

Name ¹	Package Pin Number	Pin Type	Power Supply	Notes				
DDR Memory Interface 1 Signals ^{2,3}								
D1_MDQ[0:63]	D15, A14, B12, D12, A15, B15, B13, C13, C11, D11, D9, A8, A12, A11, A9, B9, F11, G12, K11, K12, E10, E9, J11, J10, G8, H10, L9, L7, F10, G9, K9, K8, AC6, AC7, AG8, AH9, AB6, AB8, AE9, AF9, AL8, AM8, AM10, AK11, AH8, AK8, AJ10, AK10, AL12, AJ12, AL14, AM14, AL11, AM11, AM13, AK14, AM15, AJ16, AK18, AL18, AJ15, AL15, AL17, AM17	I/O	D1_GV _{DD}					
D1_MECC[0:7]	M8, M7, R8, T10, L11, L10, P9, R10	I/O	D1_GV _{DD}	_				
D1_MDM[0:8]	C14, A10, G11, H9, AD7, AJ9, AM12, AK16, N10	0	D1_GV _{DD}	_				
D1_MDQS[0:8]	A13, C10, H12, J7, AE8, AM9, AK13, AK17, N9	I/O	D1_GV _{DD}	_				
D1_MDQS[0:8]	D14, B10, H13, J8, AD8, AL9, AJ13, AM16, P10	I/O	D1_GV _{DD}	_				
D1_MBA[0:2]	AA8, AA10, T9	0	D1_GV _{DD}	_				
D1_MA[0:15]	Y10, W8, W9, V7, V8, U6, V10, U9, U7, U10, Y9, T6, T8, AE12, R7, P6	0	D1_GV _{DD}	_				
D1_MWE	AB11	0	D1_GV _{DD}	_				
D1_MRAS	AB12	0	D1_GV _{DD}	_				
D1_MCAS	AC10	0	D1_GV _{DD}	_				
D1_MCS[0:3]	AB9, AD10, AC12, AD11	0	D1_GV _{DD}	_				
D1_MCKE[0:3]	P7, M10, N8, M11	0	D1_GV _{DD}	23				
D1_MCK[0:5]	W6, E13, AH11, Y7, F14, AG10	0	D1_GV _{DD}	—				
D1_MCK[0:5]	Y6, E12, AH12, AA7, F13, AG11	0	D1_GV _{DD}	—				
D1_MODT[0:3]	AC9, AF12, AE11, AF10	0	D1_GV _{DD}	—				
D1_MDIC[0:1]	E15, G14	IO	D1_GV _{DD}	27				
D1_MV _{REF}	AM18	DDR Port 1 reference voltage	D1_GV _{DD} /2	3				
DDR Memory Interface 2 Signals ^{2,3}								

Table 63. MPC8641 Signal Reference by Functional Block



Table 65. Memory Bus Clocking Specifications

Characteristic	Maximum Pro Frequ	ocessor Core Jency	Unit	Notes	
Unaracteristic	1000, 1250, 1	333, 1500MHz		notes	
	Min	Мах			
Memory bus clock frequency	200	300	MHz	1, 2	

Notes:

1. Caution: The MPX clock to SYSCLK ratio and e600 core to MPX clock ratio settings must be chosen such that the resulting SYSCLK frequency, e600 (core) frequency, and MPX clock frequency do not exceed their respective maximum or minimum operating frequencies. Refer to Section 18.2, "MPX to SYSCLK PLL Ratio," and Section 18.3, "e600 to MPX clock PLL Ratio," for ratio settings.

2. The memory bus clock speed is half the DDR/DDR2 data rate, hence, half the MPX clock frequency.

Table 66.	Platform/MPX	bus Clocking	Specifications	

	Maximum Pro Frequ	ocessor Core Jency	Unit		
Characteristic	1000, 1250, 13	333, 1500MHz		Notes	
	Min	Мах			
Platform/MPX bus clock frequency	400	500-600	MHz	1, 2	

Notes:

1. **Caution:** The MPX clock to SYSCLK ratio and e600 core to MPX clock ratio settings must be chosen such that the resulting SYSCLK frequency, e600 (core) frequency, and MPX clock frequency do not exceed their respective maximum or minimum operating frequencies. Refer to Section 18.2, "MPX to SYSCLK PLL Ratio," and Section 18.3, "e600 to MPX clock PLL Ratio," for ratio settings.

2. Platform/MPX frequencies between 400 and 500 MHz are not supported.

Table 67. Local Bus Clocking Specifications

	Maximum Pro Frequ	ocessor Core Jency			
Characteristic	1000, 1250, 1333, 1500MHz		Unit	Notes	
	Min	Мах			
Local bus clock speed (for Local Bus Controller)	25	133	MHz	1	

Notes:

1. The Local bus clock speed on LCLK[0:2] is determined by MPX clock divided by the Local Bus PLL ratio programmed in LCRR[CLKDIV]. See the reference manual for the MPC8641D for more information on this.

18.2 MPX to SYSCLK PLL Ratio

The MPX clock is the clock that drives the MPX bus, and is also called the platform clock. The frequency of the MPX is set using the following reset signals, as shown in Table 68:

• SYSCLK input signal



Tyco Electronics800-522-6752Chip CoolersTMP.O. Box 3668Harrisburg, PA 17105-3668Internet: www.chipcoolers.comWakefield Engineering603-635-510233 Bridge St.Pelham, NH 03076Internet: www.wakefield.comInternet: www.wakefield.com

Ultimately, the final selection of an appropriate heat sink depends on many factors, such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost.

19.2.1 Internal Package Conduction Resistance

For the exposed-die packaging technology described in Table 71, the intrinsic conduction thermal resistance paths are as follows:

- The die junction-to-case thermal resistance (the case is actually the top of the exposed silicon die)
- The die junction-to-board thermal resistance

Figure 60 depicts the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.



Figure 60. C4 Package with Heat Sink Mounted to a Printed-Circuit Board

Heat generated on the active side of the chip is conducted through the silicon, through the heat sink attach material (or thermal interface material), and finally to the heat sink where it is removed by forced-air convection.

Because the silicon thermal resistance is quite small, the temperature drop in the silicon may be neglected for a first-order analysis. Thus the thermal interface material and the heat sink conduction/convective thermal resistances are the dominant terms.



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Dow-Corning Corporation Corporate Center PO Box 994 Midland, MI 48686-0994 Internet: www.dowcorning.com	800-248-2481
Shin-Etsu MicroSi, Inc. 10028 S. 51st St. Phoenix, AZ 85044 Internet: www.microsi.com	888-642-7674
Thermagon Inc. 4707 Detroit Ave. Cleveland, OH 44102 Internet: www.thermagon.com	888-246-9050

The following section provides a heat sink selection example using one of the commercially available heat sinks.

19.2.3 Heat Sink Selection Example

For preliminary heat sink sizing, the die-junction temperature can be expressed as follows:

 $T_j = T_i + T_r + (R_{\theta JC} + R_{\theta int} + R_{\theta sa}) \times P_d$

where:

T_i is the die-junction temperature

T_i is the inlet cabinet ambient temperature

 T_r is the air temperature rise within the computer cabinet

 $R_{\theta JC}$ is the junction-to-case thermal resistance

 $R_{\theta int}$ is the adhesive or interface material thermal resistance

 $R_{\theta sa}$ is the heat sink base-to-ambient thermal resistance

P_d is the power dissipated by the device

During operation, the die-junction temperatures (T_j) should be maintained less than the value specified in Table 2. The temperature of air cooling the component greatly depends on the ambient inlet air temperature and the air temperature rise within the electronic cabinet. An electronic cabinet inlet-air temperature (T_j) may range from 30° to 40°C. The air temperature rise within a cabinet (T_r) may be in the range of 5° to 10°C. The thermal resistance of the thermal interface material (R_{0int}) is typically about 0.2°C/W. For



Another useful equation is:

$$\mathbf{V}_{H} - \mathbf{V}_{L} = \mathbf{n} \frac{\mathbf{KT}}{\mathbf{q}} \left[\mathbf{In} \frac{\mathbf{I}_{H}}{\mathbf{I}_{L}} \right]$$

Where:

 $I_{fw} = Forward current$ $I_s = Saturation current$ $V_d = Voltage at diode$ $V_f = Voltage forward biased$ $V_H = Diode voltage while I_H is flowing$ $V_L = Diode voltage while I_L is flowing$ $I_H = Larger diode bias current$ $I_L = Smaller diode bias current$ $q = Charge of electron (1.6 \times 10^{-19} \text{ C})$ n = Ideality factor (normally 1.0) $K = Boltzman's constant (1.38 \times 10^{-23} \text{ Joules/K})$ T = Temperature (Kelvins)

The ratio of I_H to I_L is usually selected to be 10:1. The above simplifies to the following:

$$V_{H}-V_{L}=~1.986\times10^{-4}\times nT$$

Solving for T, the equation becomes:

$$\mathbf{nT} = \frac{\mathbf{V}_{\mathsf{H}} - \mathbf{V}_{\mathsf{L}}}{1.986 \times 10^{-4}}$$



System Design Information

20 System Design Information

This section provides electrical and thermal design recommendations for successful application of the MPC8641.

20.1 System Clocking

This device includes six PLLs, as follows:

- 1. The platform PLL generates the platform clock from the externally supplied SYSCLK input. The frequency ratio between the platform and SYSCLK is selected using the platform PLL ratio configuration bits as described in Section 18.2, "MPX to SYSCLK PLL Ratio."
- 2. The dual e600 Core PLLs generate the e600 clock from the externally supplied input.
- 3. The local bus PLL generates the clock for the local bus.
- 4. There are two internal PLLs for the SerDes block.

20.2 Power Supply Design and Sequencing

20.2.1 PLL Power Supply Filtering

Each of the PLLs listed above is provided with power through independent power supply pins.

There are a number of ways to reliably provide power to the PLLs, but the recommended solution is to provide independent filter circuits per PLL power supply as illustrated in Figure 64, one to each of the AV_{DD} type pins. By providing independent filters to each PLL the opportunity to cause noise injection from one PLL to the other is reduced.

This circuit is intended to filter noise in the PLLs resonant frequency range from a 500 kHz to 10 MHz range. It should be built with surface mount capacitors with minimum Effective Series Inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

Each circuit should be placed as close as possible to the specific AV_{DD} type pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the AV_{DD} type pin, which is on the periphery of the footprint, without the inductance of vias.

Figure 63 and Figure 64 show the PLL power supply filter circuits for the platform and cores, respectively.



Figure 63. MPC8641 PLL Power Supply Filter Circuit (for platform and Local Bus)



The COP interface has a standard header, shown in Figure 67, for connection to the target system, and is based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

The COP header adds many benefits such as breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features. An inexpensive option can be to leave the COP header unpopulated until needed.

There is no standardized way to number the COP header shown in Figure 67; consequently, many different pin numbers have been observed from emulator vendors. Some are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom, while still others number the pins counter clockwise from pin 1 (as with an IC). Regardless of the numbering, the signal placement recommended in Figure 67 is common to all known emulators.

For a multi-processor non-daisy chain configuration, Figure 68, can be duplicated for each processor. The recommended daisy chain configuration is shown in Figure 69. Please consult with your tool vendor to determine which configuration is supported by their emulator.

20.9.1 Termination of Unused Signals

If the JTAG interface and COP header will not be used, Freescale recommends the following connections:

- TRST should be tied to HRESET through a 0 k Ω isolation resistor so that it is asserted when the system reset signal (HRESET) is asserted, ensuring that the JTAG scan chain is initialized during the power-on reset flow. Freescale recommends that the COP header be designed into the system as shown in Figure 68. If this is not possible, the isolation resistor will allow future access to TRST in case a JTAG interface may need to be wired onto the system in future debug situations.
- Tie TCK to OV_{DD} through a 10 k Ω resistor. This will prevent TCK from changing state and reading incorrect data into the device.
- No connection is required for TDI, TMS, or TDO.



Figure 67. COP Connector Physical Pinout



System Design Information



Notes:

- 1. The COP port and target board should be able to independently assert HRESET and TRST to the processor in order to fully control the processor as shown here.
- 2. Populate this with a 10 Ω resistor for short-circuit/current-limiting protection.
- 3. The KEY location (pin 14) is not physically present on the COP header.
- 4. Although pin 12 is defined as a No-Connect, some debug tools may use pin 12 as an additional GND pin for improved signal integrity.
- This switch is included as a precaution for BSDL testing. The switch should be open during BSDL testing to avoid accidentally asserting the TRST line. If BSDL testing is not being performed, this switch should be closed or removed.

Figure 68. JTAG/COP Interface Connection for one MPC8641 device



Ordering Information

21 Ordering Information

Ordering information for the parts fully covered by this specification document is provided in Section 21.1, "Part Numbers Fully Addressed by This Document."

21.1 Part Numbers Fully Addressed by This Document

Table 74 provides the Freescale part numbering nomenclature for the MPC8641. Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Freescale sales office. In addition to the processor frequency, the part numbering scheme also includes an application modifier which may specify special application conditions. Each part number also contains a revision code which refers to the die mask revision number.

MC	nnnn	x	XX	nnnn	x	x
Product Code	Part Identifier	Core Count	Package ¹	Core Processor Frequency ² (MHz)	DDR speed (MHz)	Product Revision Level
MC	8641	Blank = Single Core D = Dual Core	HX = High-lead HCTE FC-CBGA VU = RoHS lead-free HCTE FC-CBGA ⁵ VJ = lead-free HCTE FC-CBGA ⁶	1000, 1250, 1333, 1500	N = 500 MHz ⁴ K = 600 MHz J = 533 MHz H = 500 MHz G = 400 MHz	Revision B = 2.0 System Version Register Value for Rev B: 0x8090_0020 - MPC8641 0x8090_0120 - MPC8641D Revision C = 2.1 System Version Register Value for Rev C: 0x8090_0021 - MPC8641 0x8090_0121 - MPC8641D Revision E = 3.0 System Version Register Value for Rev E: 0x8090_0030 - MPC86411 0x8090_0130 - MPC8641D

Table 74. Part Numbering Nomenclature

Notes:

- 1. See Section 16, "Package," for more information on available package types.
- Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by part number specifications may support other maximum core frequencies.
- 3. The P prefix in a Freescale part number designates a "Pilot Production Prototype" as defined by Freescale SOP 3-13. These parts have only preliminary reliability and characterization data. Before pilot production prototypes may be shipped, written authorization from the customer must be on file in the applicable sales office acknowledging the qualification status and the fact that product changes may still occur while shipping pilot production prototypes.
- 4. Part Number MC8641xxx1000NX is our low V_{DD} _Core*n* device. V_{DD} _Core*n* = 0.95 V and V_{DD} _PLAT = 1.05 V.
- 5. VU part number is RoHS compliant with the permitted exception of the C4 die bumps.
- 6. VJ part number is entirely lead-free including the C4 die bumps.