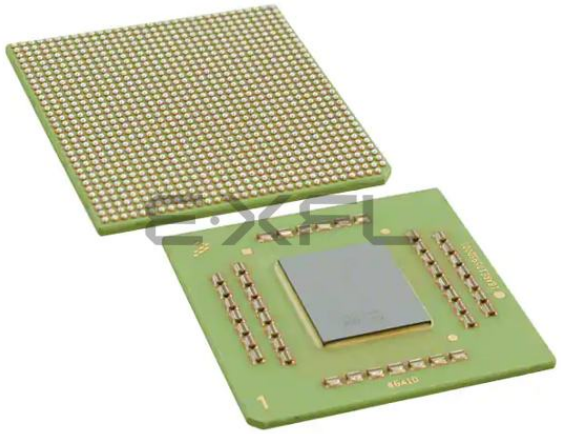

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e600
Number of Cores/Bus Width	2 Core, 32-Bit
Speed	1.5GHz
Co-Processors/DSP	-
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (4)
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	1023-BBGA, FCBGA
Supplier Device Package	1023-FCCBGA (33x33)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc8641dhx1500kc

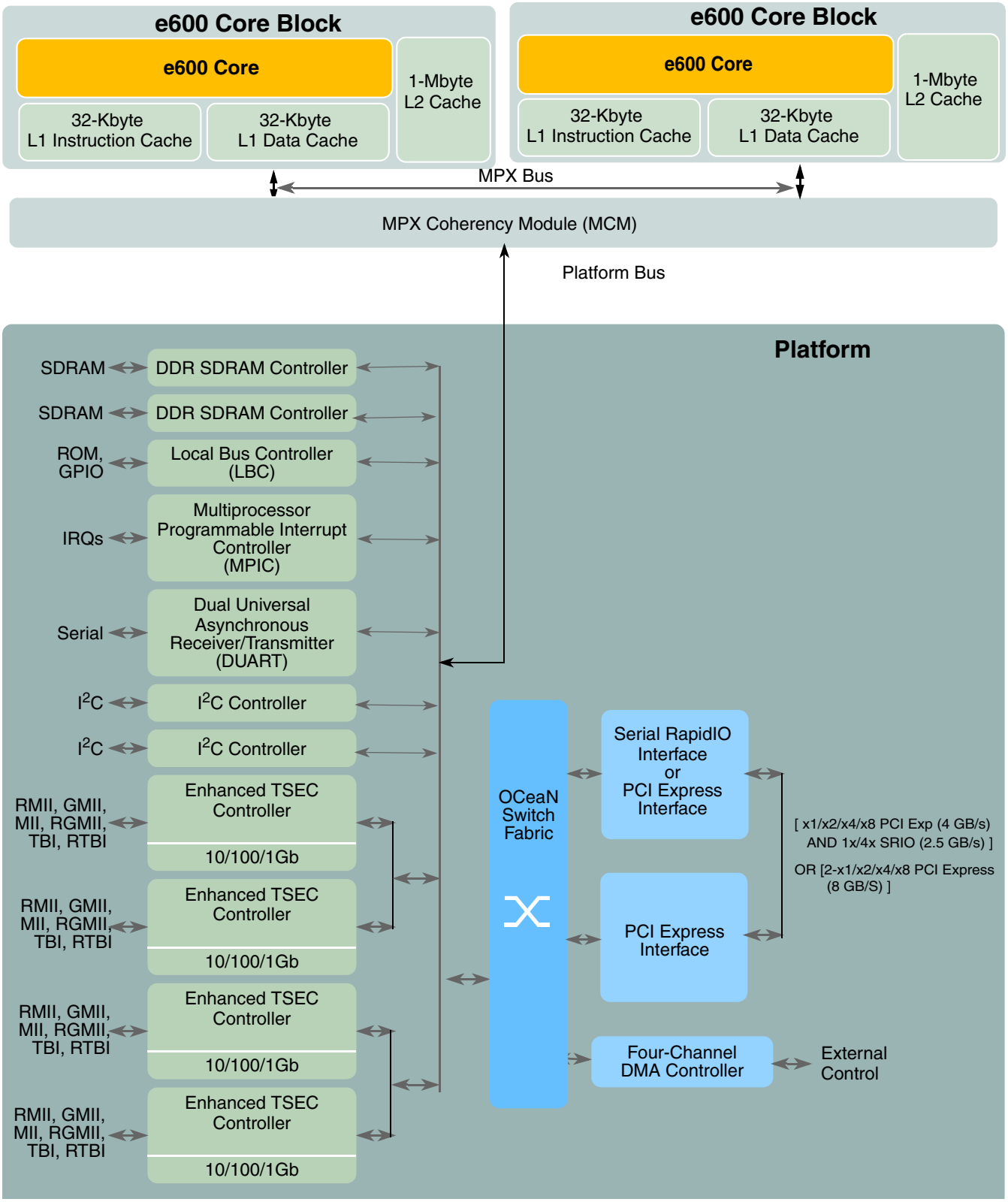


Figure 1. MPC8641 and MPC8641D

2 Electrical Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC8641. The MPC8641 is currently targeted to these specifications.

2.1 Overall DC Electrical Characteristics

This section covers the ratings, conditions, and other characteristics.

2.1.1 Absolute Maximum Ratings

Table 1 provides the absolute maximum ratings.

Table 1. Absolute Maximum Ratings[1]

Characteristic	Symbol	Absolute Maximum Value	Unit	Notes
Cores supply voltages	V_{DD}_Core0, V_{DD}_Core1	–0.3 to 1.21 V	V	2
Cores PLL supply	AV_{DD}_Core0, AV_{DD}_Core1	–0.3 to 1.21 V	V	—
SerDes Transceiver Supply (Ports 1 and 2)	SV_{DD}	–0.3 to 1.21 V	V	—
SerDes Serial I/O Supply Port 1	XV_{DD}_SRDS1	–0.3 to 1.21V	V	—
SerDes Serial I/O Supply Port 2	XV_{DD}_SRDS2	–0.3 to 1.21 V	V	—
SerDes DLL and PLL supply voltage for Port 1 and Port 2	AV_{DD}_SRDS1, AV_{DD}_SRDS2	–0.3 to 1.21V	V	—
Platform Supply voltage	V_{DD}_PLAT	–0.3 to 1.21V	V	—
Local Bus and Platform PLL supply voltage	AV_{DD}_LB, AV_{DD}_PLAT	–0.3 to 1.21V	V	—
DDR and DDR2 SDRAM I/O supply voltages	D1_GV_{DD}, D2_GV_{DD}	–0.3 to 2.75 V	V	3
		–0.3 to 1.98 V	V	3
eTSEC 1 and 2 I/O supply voltage	LV_{DD}	–0.3 to 3.63 V	V	4
		–0.3 to 2.75 V	V	4
eTSEC 3 and 4 I/O supply voltage	TV_{DD}	–0.3 to 3.63 V	V	4
		–0.3 to 2.75 V	V	4
Local Bus, DUART, DMA, Multiprocessor Interrupts, System Control & Clocking, Debug, Test, Power management, I^2C, JTAG and Miscellaneous I/O voltage	OV_{DD}	–0.3 to 3.63 V	V	—

4 Input Clocks

Table 7 provides the system clock (SYSCLK) DC specifications for the MPC8641.

Table 7. SYSCLK DC Electrical Characteristics (OVDD = 3.3 V ± 165 mV)

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	–0.3	0.8	V
Input current (V_{IN} [1] = 0 V or V_{IN} = V_{DD})	I_{IN}	—	±5	μA

Note:
1. Note that the symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

4.1 System Clock Timing

Table 8 provides the system clock (SYSCLK) AC timing specifications for the MPC8641.

Table 8. SYSCLK AC Timing Specifications

At recommended operating conditions (see Table 2) with OV_{DD} = 3.3 V ± 165 mV.

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
SYSCLK frequency	f_{SYSCLK}	66	—	166.66	MHz	1
SYSCLK cycle time	t_{SYSCLK}	6	—	—	ns	—
SYSCLK rise and fall time	t_{KH}, t_{KL}	0.6	1.0	1.2	ns	2
SYSCLK duty cycle	t_{KHK}/t_{SYSCLK}	40	—	60	%	3
SYSCLK jitter	—	—	—	150	ps	4, 5

Notes:
1. **Caution:** The MPX clock to SYSCLK ratio and e600 core to MPX clock ratio settings must be chosen such that the resulting SYSCLK frequency, e600 (core) frequency, and MPX clock frequency do not exceed their respective maximum or minimum operating frequencies. See Section 18.2, “MPX to SYSCLK PLL Ratio,” and Section 18.3, “e600 to MPX clock PLL Ratio,” for ratio settings.
2. Rise and fall times for SYSCLK are measured at 0.4 V and 2.7 V.
3. Timing is guaranteed by design and characterization.
4. This represents the short term jitter only and is guaranteed by design.
5. The SYSCLK driver’s closed loop jitter bandwidth should be <500 kHz at –20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track SYSCLK drivers with the specified jitter. Note that the frequency modulation for SYSCLK reduces significantly for the spread spectrum source case. This is to guarantee what is supported based on design.

4.1.1 SYSCLK and Spread Spectrum Sources

Spread spectrum clock sources are an increasingly popular way to control electromagnetic interference emissions (EMI) by spreading the emitted noise to a wider spectrum and reducing the peak noise magnitude in order to meet industry and government requirements. These clock sources intentionally add long-term jitter in order to diffuse the EMI spectral content. The jitter specification given in Table 8 considers short-term (cycle-to-cycle) jitter only and the clock generator’s cycle-to-cycle output jitter

Figure 7 provides the AC test load for the DDR bus.

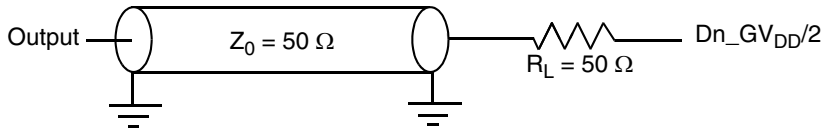


Figure 7. DDR AC Test Load

7 DUART

This section describes the DC and AC electrical specifications for the DUART interface of the MPC8641.

7.1 DUART DC Electrical Characteristics

Table 22 provides the DC electrical characteristics for the DUART interface.

Table 22. DUART DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	–0.3	0.8	V
Input current (V_{IN} [1] = 0 V or V_{IN} = V_{DD})	I_{IN}	—	±5	μA
High-level output voltage (OV_{DD} = min, I_{OH} = –100 μA)	V_{OH}	OV_{DD} – 0.2	—	V
Low-level output voltage (OV_{DD} = min, I_{OL} = 100 μA)	V_{OL}	—	0.2	V

Note:
1. Note that the symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

7.2 DUART AC Electrical Specifications

Table 23 provides the AC timing parameters for the DUART interface.

Table 23. DUART AC Timing Specifications

Parameter	Value	Unit	Notes
Minimum baud rate	MPX clock/1,048,576	baud	1,2
Maximum baud rate	MPX clock/16	baud	1,3
Oversample rate	16	—	1,4

Notes:
1. Guaranteed by design.
2. MPX clock refers to the platform clock.
3. Actual attainable baud rate will be limited by the latency of interrupt processing.
4. The middle of a start bit is detected as the 8th sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16th sample.

clock to synchronously generate transmit data and outputs an echoed copy of the transmit clock back out onto the TSEC*n*_GTX_CLK pin (while transmit data appears on TSEC*n*_TXD[7:0], for example). It is intended that external receivers capture eTSEC transmit data using the clock on TSEC*n*_GTX_CLK as a source-synchronous timing reference. Typically, the clock edge that launched the data can be used, since the clock is delayed by the eTSEC to allow acceptable set-up margin at the receiver. Note that there is relationship between the maximum FIFO speed and the platform speed. For more information see Section 18.4.2, "Platform to FIFO Restrictions."

NOTE

The phase between the output clocks TSEC1_GTX_CLK and TSEC2_GTX_CLK (ports 1 and 2) is no more than 100 ps. The phase between the output clocks TSEC3_GTX_CLK and TSEC4_GTX_CLK (ports 3 and 4) is no more than 100 ps.

A summary of the FIFO AC specifications appears in Table 26 and Table 27.

Table 26. FIFO Mode Transmit AC Timing Specification

At recommended operating conditions with L/TV_{DD} of 3.3 V ± 5% and 2.5 V ± 5%.

Parameter/Condition	Symbol	Min	Typ	Max	Unit
TX_CLK, GTX_CLK clock period (GMII mode)	t_{FIT}	7.0	8.0	100	ns
TX_CLK, GTX_CLK clock period (Encoded mode)	t_{FIT}	5.3	8.0	100	ns
TX_CLK, GTX_CLK duty cycle	t_{FITH}/t_{FIT}	45	50	55	%
TX_CLK, GTX_CLK peak-to-peak jitter	t_{FITJ}	—	—	250	ps
Rise time TX_CLK (20%–80%)	t_{FITR}	—	—	0.75	ns
Fall time TX_CLK (80%–20%)	t_{FITF}	—	—	0.75	ns
FIFO data TXD[7:0], TX_ER, TX_EN setup time to GTX_CLK	t_{FITDV}	2.0	—	—	ns
GTX_CLK to FIFO data TXD[7:0], TX_ER, TX_EN hold time	t_{FITDX}	0.5	—	3.0	ns

Table 27. FIFO Mode Receive AC Timing Specification

At recommended operating conditions with L/TV_{DD} of 3.3 V ± 5% and 2.5 V ± 5%.

Parameter/Condition	Symbol	Min	Typ	Max	Unit
RX_CLK clock period (GMII mode)	t_{FIR}[1]	7.0	8.0	100	ns
RX_CLK clock period (Encoded mode)	t_{FIR}[1]	5.3	8.0	100	ns
RX_CLK duty cycle	t_{FIRH}/t_{FIR}	45	50	55	%
RX_CLK peak-to-peak jitter	t_{FIRJ}	—	—	250	ps
Rise time RX_CLK (20%–80%)	t_{FIRR}	—	—	0.75	ns
Fall time RX_CLK (80%–20%)	t_{FIRF}	—	—	0.75	ns
RXD[7:0], RX_DV, RX_ER setup time to RX_CLK	t_{FIRDV}	1.5	—	—	ns
RXD[7:0], RX_DV, RX_ER hold time to RX_CLK	t_{FIRDX}	0.5	—	—	ns

[1] ±100 ppm tolerance on RX_CLK frequency

8.2.7.2 RMII Receive AC Timing Specifications

Table 37. RMII Receive AC Timing Specifications

At recommended operating conditions with LV_{DD} of 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
REF_CLK clock period	t_{RMR}	15.0	20.0	25.0	ns
REF_CLK duty cycle	t_{RMRH}/t_{RMR}	35	50	65	%
REF_CLK peak-to-peak jitter	t_{RMRJ}	—	—	250	ps
Rise time REF_CLK (20%–80%)	t_{RMRR}	1.0	—	2.0	ns
Fall time REF_CLK (80%–20%)	t_{RMRF}	1.0	—	2.0	ns
RXD[1:0], CRS_DV, RX_ER setup time to REF_CLK rising edge	t_{RMRDV}	4.0	—	—	ns
RXD[1:0], CRS_DV, RX_ER hold time to REF_CLK rising edge	t_{RMRDX}	2.0	—	—	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 21 provides the AC test load for eTSEC.

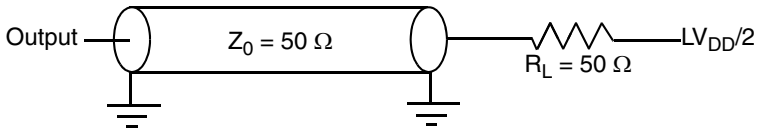


Figure 21. eTSEC AC Test Load

Figure 22 shows the RMII receive AC timing diagram.

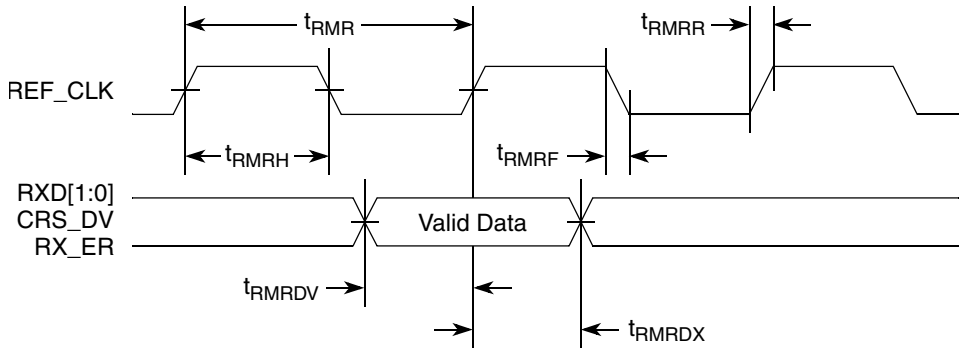


Figure 22. RMII Receive AC Timing Diagram

10 Local Bus

This section describes the DC and AC electrical specifications for the local bus interface of the MPC8641.

10.1 Local Bus DC Electrical Characteristics

Table 40 provides the DC electrical characteristics for the local bus interface operating at OV_{DD} = 3.3 V DC.

Table 40. Local Bus DC Electrical Characteristics (3.3 V DC)

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	–0.3	0.8	V
Input current (V_{IN} [1] = 0 V or V_{IN} = OV_{DD})	I_{IN}	—	±5	μA
High-level output voltage (OV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	OV_{DD} – 0.2	—	V
Low-level output voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.2	V

Note:
1. Note that the symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

10.2 Local Bus AC Electrical Specifications

Table 41 describes the timing parameters of the local bus interface at OV_{DD} = 3.3 V with PLL enabled. For information about the frequency range of local bus see Section 18.1, "Clock Ranges."

Table 41. Local Bus Timing Parameters (OV_{DD} = 3.3 V)m - PLL Enabled

Parameter	Symbol [1]	Min	Max	Unit	Notes
Local bus cycle time	t_{LBK}	7.5	—	ns	2
Local Bus Duty Cycle	t_{LBKH}/t_{LBK}	45	55	%	—
LCLK[n] skew to LCLK[m] or LSYNC_OUT	$t_{LBKSKEW}$	—	150	ps	7, 8
Input setup to local bus clock (except $\overline{\text{LGTA}}$/LUPWAIT)	$t_{LBIVKH1}$	1.8	—	ns	3, 4
$\overline{\text{LGTA}}$/LUPWAIT input setup to local bus clock	$t_{LBIVKH2}$	1.7	—	ns	3, 4
Input hold from local bus clock (except $\overline{\text{LGTA}}$/LUPWAIT)	$t_{LBIXKH1}$	1.0	—	ns	3, 4
$\overline{\text{LGTA}}$/LUPWAIT input hold from local bus clock	$t_{LBIXKH2}$	1.0	—	ns	3, 4
LALE output transition to LAD/LDP output transition (LATCH hold time)	t_{LBOTOT}	1.5	—	ns	6
Local bus clock to output valid (except LAD/LDP and LALE)	$t_{LBKHOV1}$	—	2.0	ns	—
Local bus clock to data valid for LAD/LDP	$t_{LBKHOV2}$	—	2.2	ns	—
Local bus clock to address valid for LAD	$t_{LBKHOV3}$	—	2.3	ns	—

Table 42. Local Bus Timing Parameters—PLL Bypassed (continued)

Parameter	Symbol [1]	Min	Max	Unit	Notes
$\overline{\text{LGTA}}$/LUPWAIT input hold from local bus clock	$t_{LBIXKL2}$	–1.3	—	ns	4, 5
LALE output transition to LAD/LDP output transition (LATCH hold time)	t_{LBOTOT}	1.5	—	ns	6
Local bus clock to output valid (except LAD/LDP and LALE)	$t_{LBKLOV1}$	—	–0.3	ns	
Local bus clock to data valid for LAD/LDP	$t_{LBKLOV2}$	—	–0.1	ns	4
Local bus clock to address valid for LAD	$t_{LBKLOV3}$	—	0	ns	4
Local bus clock to LALE assertion	$t_{LBKLOV4}$	—	0	ns	4
Output hold from local bus clock (except LAD/LDP and LALE)	$t_{LBKLOX1}$	–3.2	—	ns	4
Output hold from local bus clock for LAD/LDP	$t_{LBKLOX2}$	–3.2	—	ns	4
Local bus clock to output high Impedance (except LAD/LDP and LALE)	$t_{LBKLOZ1}$	—	0.2	ns	7
Local bus clock to output high impedance for LAD/LDP	$t_{LBKLOZ2}$	—	0.2	ns	7

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(First two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(First two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one(1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to local bus clock for PLL bypass mode. Timings may be negative with respect to the local bus clock because the actual launch and capture of signals is done with the internal launch/capture clock, which precedes LCLK by t_{LBKHKT}.
3. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at $BV_{DD}/2$.
4. All signals are measured from BVDD/2 of the rising edge of local bus clock for PLL bypass mode to 0.4 x BVDD of the signal in question for 3.3-V signaling levels.
5. Input timings are measured at the pin.
6. The value of t_{LBOTOT} is the measurement of the minimum time between the negation of LALE and any change in LAD
7. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
8. Guaranteed by characterization.

11 JTAG

This section describes the DC and AC electrical specifications for the IEEE 1149.1 (JTAG) interface of the MPC8641/D.

11.1 JTAG DC Electrical Characteristics

Table 43 provides the DC electrical characteristics for the JTAG interface.

Table 43. JTAG DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	– 0.3	0.8	V
Input current (V_{IN} [1] = 0 V or V_{IN} = V_{DD})	I_{IN}	—	±5	μA
High-level output voltage (OV_{DD} = min, I_{OH} = –100 μA)	V_{OH}	OV_{DD} – 0.2	—	V
Low-level output voltage (OV_{DD} = min, I_{OL} = 100 μA)	V_{OL}	—	0.2	V

Note:
1. Note that the symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

11.2 JTAG AC Electrical Specifications

Table 44 provides the JTAG AC timing specifications as defined in Figure 33 through Figure 35.

Table 44. JTAG AC Timing Specifications (Independent of SYSCLK) [1]

At recommended operating conditions (see Table 3).

Parameter	Symbol [2]	Min	Max	Unit	Notes
JTAG external clock frequency of operation	f_{JTG}	0	33.3	MHz	—
JTAG external clock cycle time	t_{JTG}	30	—	ns	—
JTAG external clock pulse width measured at 1.4 V	t_{JTKHKL}	15	—	ns	—
JTAG external clock rise and fall times	t_{JTGR} & t_{JTGF}	0	2	ns	6
$\overline{TRST}$ assert time	t_{TRST}	25	—	ns	3
Input setup times: Boundary-scan data TMS, TDI	 t_{JTDVKH} t_{JTIVKH}	 4 0	 — —	ns	4
Input hold times: Boundary-scan data TMS, TDI	 t_{JTDXKH} t_{JTIXKH}	 20 25	 — —	ns	4
Valid times: Boundary-scan data TDO	 t_{JTKLDV} t_{JTKLOV}	 4 4	 20 25	ns	5

Table 45. I²C DC Electrical Characteristics (continued)

At recommended operating conditions with OV_{DD} of 3.3 V ± 5%.

Parameter	Symbol	Min	Max	Unit	Notes
Capacitance for each I/O pin	C_I	—	10	pF	—

Notes:
1. Output voltage (open drain or open collector) condition = 3 mA sink current.
2. Refer to the *MPC8641 Integrated Host Processor Reference Manual* for information on the digital filter used.
3. I/O pins will obstruct the SDA and SCL lines if OV_{DD} is switched off.

12.2 I²C AC Electrical Specifications

Table 46 provides the AC timing parameters for the I²C interfaces.

Table 46. I²C AC Electrical Specifications

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 45).

Parameter	Symbol [1]	Min	Max	Unit
SCL clock frequency	f_{I2C}	0	400	kHz
Low period of the SCL clock	t_{I2CL} [4]	1.3	—	μs
High period of the SCL clock	t_{I2CH} [4]	0.6	—	μs
Setup time for a repeated START condition	t_{I2SVKH} [4]	0.6	—	μs
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t_{I2SXKL} [4]	0.6	—	μs
Data setup time	t_{I2DVKH} [4]	100	—	ns
Data input hold time: CBUS compatible masters I²C bus devices	t_{I2DXKL}	 — 0 [2]	 — —	 μs
Rise time of both SDA and SCL signals	t_{I2CR}	$20 + 0.1\ C_B$ [5]	300	ns
Fall time of both SDA and SCL signals	t_{I2CF}	$20 + 0.1\ C_b$ [5]	300	ns
Data output delay time	t_{I2OVKL}	—	0.9 [3]	μs
Set-up time for STOP condition	t_{I2PVKH}	0.6	—	μs
Bus free time between a STOP and START condition	t_{I2KHDX}	1.3	—	μs
Noise margin at the LOW level for each connected device (including hysteresis)	V_{NL}	$0.1 \times OV_{DD}$	—	V

14.1 DC Requirements for PCI Express SD*n*_REF_CLK and $\overline{\text{SD}n\text{\_REF\_CLK}}$

For more information, see Section 13.2, "SerDes Reference Clocks."

14.2 AC Requirements for PCI Express SerDes Clocks

Table 48 lists AC requirements.

Table 48. SD*n*_REF_CLK and $\overline{\text{SD}n\text{\_REF\_CLK}}$ AC Requirements

Symbol	Parameter Description	Min	Typical	Max	Units	Notes
t_{REF}	REFCLK cycle time	—	10	—	ns	—
t_{REFCJ}	REFCLK cycle-to-cycle jitter. Difference in the period of any two adjacent REFCLK cycles	—	—	100	ps	—
t_{REFPJ}	Phase jitter. Deviation in edge location with respect to mean edge location	–50	—	50	ps	—

14.3 Clocking Dependencies

The ports on the two ends of a link must transmit data at a rate that is within 600 parts per million (ppm) of each other at all times. This is specified to allow bit rate clock sources with a +/– 300 ppm tolerance.

14.4 Physical Layer Specifications

The following is a summary of the specifications for the physical layer of PCI Express on this device. For further details as well as the specifications of the Transport and Data Link layer please use the PCI EXPRESS Base Specification. REV. 1.0a document.

14.4.1 Differential Transmitter (TX) Output

Table 49 defines the specifications for the differential output at all transmitters (TXs). The parameters are specified at the component pins.

Table 49. Differential Transmitter (TX) Output Specifications

Symbol	Parameter	Min	Nom	Max	Units	Comments
UI	Unit Interval	399.88	400	400.12	ps	Each UI is 400 ps ± 300 ppm. UI does not account for Spread Spectrum Clock dictated variations. See Note 1.
$V_{TX\text{-}DIFFp\text{-}p}$	Differential Peak-to-Peak Output Voltage	0.8	—	1.2	V	$V_{TX\text{-}DIFFp\text{-}p} = 2*\lvert V_{TX\text{-}D+} - V_{TX\text{-}D-}\rvert$ See Note 2.
$V_{TX\text{-}DE\text{-}RATIO}$	De- Emphasized Differential Output Voltage (Ratio)	–3.0	–3.5	–4.0	dB	Ratio of the $V_{TX\text{-}DIFFp\text{-}p}$ of the second and following bits after a transition divided by the $V_{TX\text{-}DIFFp\text{-}p}$ of the first bit after a transition. See Note 2.

Table 50. Differential Receiver (RX) Input Specifications (continued)

Symbol	Parameter	Min	Nom	Max	Units	Comments
$T_{RX-IDLE-DET-DIFF-ENTERTIME}$	Unexpected Electrical Idle Enter Detect Threshold Integration Time	—	—	10	ms	An unexpected Electrical Idle ($V_{RX-DIFFp-p} < V_{RX-IDLE-DET-DIFFp-p}$) must be recognized no longer than $T_{RX-IDLE-DET-DIFF-ENTERING}$ to signal an unexpected idle condition.
$L_{TX-SKEW}$	Total Skew	—	—	20	ns	Skew across all lanes on a Link. This includes variation in the length of SKP ordered set (for example, COM and one to five Symbols) at the RX as well as any delay differences arising from the interconnect itself.

Notes:
1. No test load is necessarily associated with this value.
2. Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 52 should be used as the RX device when taking measurements (also refer to the Receiver compliance eye diagram shown in Figure 51). If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.
3. A T_{RX-EYE} = 0.40 UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the Transmitter and interconnect collected any 250 consecutive UIs. The $T_{RX-EYE-MEDIAN-to-MAX-JITTER}$ specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total. UI jitter budget collected over any 250 consecutive TX UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as the reference for the eye diagram.
4. The Receiver input impedance shall result in a differential return loss greater than or equal to 15 dB with the D+ line biased to 300 mV and the D- line biased to -300 mV and a common mode return loss greater than or equal to 6 dB (no bias required) over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements for is 50 Ω to ground for both the D+ and D- line (that is, as measured by a Vector Network Analyzer with 50 ohm probes - see Figure 52). Note: that the series capacitors C_{TX} is optional for the return loss measurement.
5. Impedance during all LTSSM states. When transitioning from a Fundamental Reset to Detect (the initial state of the LTSSM) there is a 5 ms transition time before Receiver termination values must be met on all un-configured Lanes of a Port.
6. The RX DC Common Mode Impedance that exists when no power is present or Fundamental Reset is asserted. This helps ensure that the Receiver Detect circuit will not falsely assume a Receiver is powered on when it is not. This term must be measured at 300 mV above the RX ground.
7. It is recommended that the recovered TX UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function. Least squares and median deviation fits have worked well with experimental and simulated data.

14.5 Receiver Compliance Eye Diagrams

The RX eye diagram in Figure 51 is specified using the passive compliance/test measurement load (see Figure 52) in place of any real PCI Express RX component.

Note: In general, the minimum Receiver eye diagram measured with the compliance/test measurement load (see Figure 52) will be larger than the minimum Receiver eye diagram measured over a range of systems at the input Receiver of any real PCI Express component. The degraded eye diagram at the input Receiver is due to traces internal to the package as well as silicon parasitic characteristics which cause the real PCI Express component to vary in impedance from the compliance/test measurement load. The input Receiver eye diagram is implementation specific and is not specified. RX component designer should

Table 52. Short Run Transmitter AC Timing Specifications—1.25 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output Voltage,	V_O	–0.40	2.30	Volts	Voltage relative to COMMON of either signal comprising a differential pair
Differential Output Voltage	V_{DIFFPP}	500	1000	mV p-p	—
Deterministic Jitter	J_D	—	0.17	UI p-p	—
Total Jitter	J_T	—	0.35	UI p-p	—
Multiple output skew	S_{MO}	—	1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	800	800	ps	+/– 100 ppm

Table 53. Short Run Transmitter AC Timing Specifications—2.5 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output Voltage,	V_O	–0.40	2.30	Volts	Voltage relative to COMMON of either signal comprising a differential pair
Differential Output Voltage	V_{DIFFPP}	500	1000	mV p-p	—
Deterministic Jitter	J_D	—	0.17	UI p-p	—
Total Jitter	J_T	—	0.35	UI p-p	—
Multiple Output skew	S_{MO}	—	1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	400	400	ps	+/– 100 ppm

Table 54. Short Run Transmitter AC Timing Specifications—3.125 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output Voltage,	V_O	–0.40	2.30	Volts	Voltage relative to COMMON of either signal comprising a differential pair
Differential Output Voltage	V_{DIFFPP}	500	1000	mV p-p	—
Deterministic Jitter	J_D	—	0.17	UI p-p	—
Total Jitter	J_T	—	0.35	UI p-p	—

Continuous Jitter Test Pattern (CJPAT) defined in Annex 48A of IEEE 802.3ae. All lanes of the LP-Serial link shall be active in both the transmit and receive directions, and opposite ends of the links shall use asynchronous clocks. Four lane implementations shall use CJPAT as defined in Annex 48A. Single lane implementations shall use the CJPAT sequence specified in Annex 48A for transmission on lane 0. The amount of data represented in the eye shall be adequate to ensure that the bit error ratio is less than 10^{-12}. The eye pattern shall be measured with AC coupling and the compliance template centered at 0 Volts differential. The left and right edges of the template shall be aligned with the mean zero crossing points of the measured data eye. The load for this test shall be 100 Ω resistive +/– 5% differential to 2.5 GHz.

15.9.2 Jitter Test Measurements

For the purpose of jitter measurement, the effects of a single-pole high pass filter with a 3 dB point at (Baud Frequency)/1667 is applied to the jitter. The data pattern for jitter measurements is the Continuous Jitter Test Pattern (CJPAT) pattern defined in Annex 48A of IEEE 802.3ae. All lanes of the LP-Serial link shall be active in both the transmit and receive directions, and opposite ends of the links shall use asynchronous clocks. Four lane implementations shall use CJPAT as defined in Annex 48A. Single lane implementations shall use the CJPAT sequence specified in Annex 48A for transmission on lane 0. Jitter shall be measured with AC coupling and at 0 Volts differential. Jitter measurement for the transmitter (or for calibration of a jitter tolerance setup) shall be performed with a test procedure resulting in a BER curve such as that described in Annex 48B of IEEE 802.3ae.

15.9.3 Transmit Jitter

Transmit jitter is measured at the driver output when terminated into a load of 100 Ω resistive +/– 5% differential to 2.5 GHz.

15.9.4 Jitter Tolerance

Jitter tolerance is measured at the receiver using a jitter tolerance test signal. This signal is obtained by first producing the sum of deterministic and random jitter defined in Section 8.6 and then adjusting the signal amplitude until the data eye contacts the 6 points of the minimum eye opening of the receive template shown in Figure 8-4 and Table 8-11. Note that for this to occur, the test signal must have vertical waveform symmetry about the average value and have horizontal symmetry (including jitter) about the mean zero crossing. Eye template measurement requirements are as defined above. Random jitter is calibrated using a high pass filter with a low frequency corner at 20 MHz and a 20 dB/decade roll-off below this. The required sinusoidal jitter specified in Section 8.6 is then added to the signal and the test load is replaced by the receiver being tested.

Table 63. MPC8641 Signal Reference by Functional Block (continued)

Name[1]	Package Pin Number	Pin Type	Power Supply	Notes
TSEC1_TXD[0:7]/ GPOUT[0:7]	AF25, AC23,AG24, AG23, AE24, AE23, AE22, AD22	O	LV_{DD}	6, 10
TSEC1_TX_EN	AB22	O	LV_{DD}	36
TSEC1_TX_ER	AH26	O	LV_{DD}	—
TSEC1_TX_CLK	AC22	I	LV_{DD}	40
TSEC1_GTX_CLK	AH25	O	LV_{DD}	41
TSEC1_CRS	AM24	I/O	LV_{DD}	37
TSEC1_COL	AM25	I	LV_{DD}	—
TSEC1_RXD[0:7]/ GPIN[0:7]	AL25, AL24, AK26, AK25, AM26, AF26, AH24, AG25	I	LV_{DD}	10
TSEC1_RX_DV	AJ24	I	LV_{DD}	—
TSEC1_RX_ER	AJ25	I	LV_{DD}	—
TSEC1_RX_CLK	AK24	I	LV_{DD}	40
eTSEC Port 2 Signals[5]				
TSEC2_TXD[0:3]/ GPOUT[8:15]	AB20, AJ23, AJ22, AD19	O	LV_{DD}	6, 10
TSEC2_TXD[4]/ GPOUT[12]	AH23	O	LV_{DD}	6,10, 38
TSEC2_TXD[5:7]/ GPOUT[13:15]	AH21, AG22, AG21	O	LV_{DD}	6, 10
TSEC2_TX_EN	AB21	O	LV_{DD}	36
TSEC2_TX_ER	AB19	O	LV_{DD}	6, 38
TSEC2_TX_CLK	AC21	I	LV_{DD}	40
TSEC2_GTX_CLK	AD20	O	LV_{DD}	41
TSEC2_CRS	AE20	I/O	LV_{DD}	37
TSEC2_COL	AE21	I	LV_{DD}	—
TSEC2_RXD[0:7]/ GPIN[8:15]	AL22, AK22, AM21, AH20, AG20, AF20, AF23, AF22	I	LV_{DD}	10
TSEC2_RX_DV	AC19	I	LV_{DD}	—
TSEC2_RX_ER	AD21	I	LV_{DD}	—
TSEC2_RX_CLK	AM22	I	LV_{DD}	40
eTSEC Port 3 Signals[5]				
TSEC3_TXD[0:3]	AL21, AJ21, AM20, AJ20	O	TV_{DD}	6
TSEC3_TXD[4]/	AM19	O	TV_{DD}	—
TSEC3_TXD[5:7]	AK21, AL20, AL19	O	TV_{DD}	6

Table 63. MPC8641 Signal Reference by Functional Block (continued)

Name[1]	Package Pin Number	Pin Type	Power Supply	Notes
$SENSEV_{SS}$_Core0	P14	Core0 GND sensing pin	—	31
$SENSEV_{SS}$_Core1	V20	Core1 GND sensing pin	—	12, 31, *S3*
$SENSEV_{DD}$_PLAT	N18	V_{DD}_PLAT sensing pin	—	28
$SENSEV_{SS}$_PLAT	P18	Platform GND sensing pin	—	29
$D1\_GV_{DD}$	B11, B14, D10, D13, F9, F12, H8, H11, H14, K10, K13, L8, P8, R6, U8, V6, W10, Y8, AA6, AB10, AC8, AD12, AE10, AF8, AG12, AH10, AJ8, AJ14, AK12, AL10, AL16	SDRAM 1 I/O supply	$D1\_GV_{DD}$ 2.5 - DDR 1.8 DDR2	—
$D2\_GV_{DD}$	B2, B5, B8, D4, D7, E2, F6, G4, H2, J6, K4, L2, M6, N4, P2, T4, U2, W4, Y2, AB4, AC2, AD6, AE4, AF2, AG6, AH4, AJ2, AK6, AL4, AM2	SDRAM 2 I/O supply	$D2\_GV_{DD}$ 2.5 V - DDR 1.8 V - DDR2	—
OV_{DD}	B22, B25, B28, D17, D24, D27, F19, F22, F26, F29, G17, H21, H24, K19, K23, M21, AM30	DUART, Local Bus, DMA, Multiprocessor Interrupts, System Control & Clocking, Debug, Test, JTAG, Power management, I^2C, JTAG and Miscellaneous I/O voltage	OV_{DD} 3.3 V	—
LV_{DD}	AC20, AD23, AH22	TSEC1 and TSEC2 I/O voltage	LV_{DD} 2.5/3.3 V	—
TV_{DD}	AC17, AG18, AK20	TSEC3 and TSEC4 I/O voltage	TV_{DD} 2.5/3.3 V	—
SV_{DD}	H31, J29, K28, K32, L30, M28, M31, N29, R30, T31, U29, V32, W30, Y31, AA29, AB32, AC30, AD31, AE29, AG30, AH31, AJ29, AK32, AL30, AM31	Transceiver Power Supply SerDes	SV_{DD} 1.05/1.1 V	—
XV_{DD}_SRDS1	K26, L24, M27, N25, P26, R24, R28, T27, U25, V26	Serial I/O Power Supply for SerDes Port 1	XV_{DD}_SRDS1 1.05/1.1 V	—

Table 63. MPC8641 Signal Reference by Functional Block (continued)

Name[1]	Package Pin Number	Pin Type	Power Supply	Notes

37.This pin is only an output in FIFO mode when used as Rx Flow Control.

38.This pin functions as cfg_dram_type[0 or 1] at reset and MUST BE VALID BEFORE HRESET ASSERTION in device sleep mode.

39. Should be pulled to ground if unused (such as in FIFO, MII and RMII modes).

40. See Section 18.4.2, “Platform to FIFO Restrictions” for clock speed limitations for this pin when used in FIFO mode.

41. The phase between the output clocks TSEC1_GTX_CLK and TSEC2_GTX_CLK (ports 1 and 2) is no more than 100 ps. The phase between the output clocks TSEC3_GTX_CLK and TSEC4_GTX_CLK (ports 3 and 4) is no more than 100 ps.

42. For systems which boot from Local Bus (GPCM)-controlled flash, a pullup on LGPL4 is required.

Special Notes for Single Core Device:

S1. Solder ball for this signal will not be populated in the single core package.

S2. The PLL filter from V_{DD}_Core1 to AV_{DD}_Core1 should be removed. AV_{DD}_Core1 should be pulled to ground with a weak (2–10 kΩ) resistor. See Section 20.2.1, “PLL Power Supply Filtering” for more details.

S3. This pin should be pulled to GND for the single core device.

S4. No special requirement for this pin on single core device. Pin should be tied to power supply as directed for dual core.

18 Clocking

This section describes the PLL configuration of the MPC8641. Note that the platform clock is identical to the MPX clock.

18.1 Clock Ranges

Table 64 provides the clocking specifications for the processor cores and Table 65 provides the clocking specifications for the memory bus. Table 66 provides the clocking for the Platform/MPX bus and Table 67 provides the clocking for the Local bus.

Table 64. Processor Core Clocking Specifications

Characteristic	Maximum Processor Core Frequency								Unit	Notes
	1000 MHz		1250MHz		1333MHz		1500 MHz			
	Min	Max	Min	Max	Min	Max	Min	Max		
e600 core processor frequency	800	1000	800	1250	800	1333	800	1500	MHz	1, 2

Notes:

1. **Caution:** The MPX clock to SYSCLK ratio and e600 core to MPX clock ratio settings must be chosen such that the resulting SYSCLK frequency, e600 (core) frequency, and MPX clock frequency do not exceed their respective maximum or minimum operating frequencies. Refer to Section 18.2, “MPX to SYSCLK PLL Ratio,” and Section 18.3, “e600 to MPX clock PLL Ratio,” for ratio settings.
2. The minimum e600 core frequency is based on the minimum platform clock frequency of 400 MHz.

Conductivity	Value	Unit
Die (12.4x15.3x0.86 mm)		
Silicon	Temperature dependent	
Bump and Underfill (12.4 × 15.3 × 0.07 mm) Collapsed Resistance		
k_z	5.3	W/(m • K)
Substrate (33 × 33 × 1.2 mm)		
k_x	13.5	W/(m • K)
k_y	13.5	
k_z	5.3	
C5 Solder layer (33 × 33 × 0.4 mm)		
k_x	0.034	W/(m • K)
k_y	0.034	
k_z	9.6	

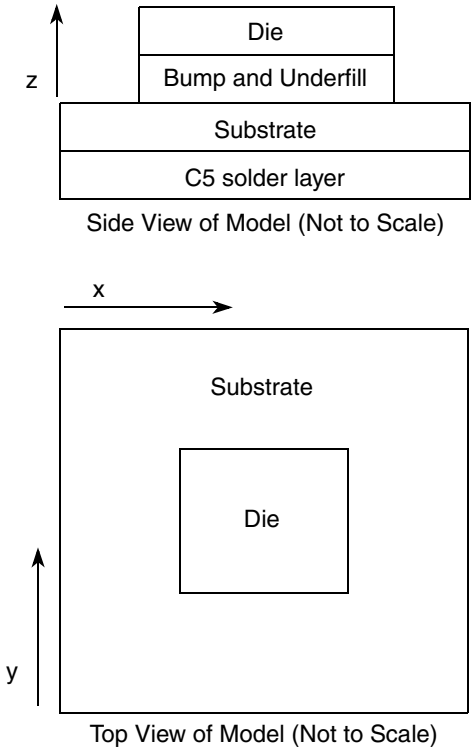


Figure 62. Recommended Thermal Model of MPC8641

19.2.4 Temperature Diode

The MPC8641 has a temperature diode on the microprocessor that can be used in conjunction with other system temperature monitoring devices (such as Analog Devices, ADT7461™). These devices use the negative temperature coefficient of a diode operated at a constant current to determine the temperature of the microprocessor and its environment. It is recommended that each device be individually calibrated.

The following are the specifications of the MPC8641 on-board temperature diode:

$V_f > 0.40$ V

$V_f < 0.90$ V

An approximate value of the ideality may be obtained by calibrating the device near the expected operating temperature.

Ideality factor is defined as the deviation from the ideal diode equation:

$$I_{fw} = I_s \left[e^{\frac{qV_f}{nKT}} - 1 \right]$$

20 System Design Information

This section provides electrical and thermal design recommendations for successful application of the MPC8641.

20.1 System Clocking

This device includes six PLLs, as follows:

1. The platform PLL generates the platform clock from the externally supplied SYSCLK input. The frequency ratio between the platform and SYSCLK is selected using the platform PLL ratio configuration bits as described in Section 18.2, "MPX to SYSCLK PLL Ratio."
2. The dual e600 Core PLLs generate the e600 clock from the externally supplied input.
3. The local bus PLL generates the clock for the local bus.
4. There are two internal PLLs for the SerDes block.

20.2 Power Supply Design and Sequencing

20.2.1 PLL Power Supply Filtering

Each of the PLLs listed above is provided with power through independent power supply pins.

There are a number of ways to reliably provide power to the PLLs, but the recommended solution is to provide independent filter circuits per PLL power supply as illustrated in Figure 64, one to each of the AV_{DD} type pins. By providing independent filters to each PLL the opportunity to cause noise injection from one PLL to the other is reduced.

This circuit is intended to filter noise in the PLLs resonant frequency range from a 500 kHz to 10 MHz range. It should be built with surface mount capacitors with minimum Effective Series Inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

Each circuit should be placed as close as possible to the specific AV_{DD} type pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the AV_{DD} type pin, which is on the periphery of the footprint, without the inductance of vias.

Figure 63 and Figure 64 show the PLL power supply filter circuits for the platform and cores, respectively.

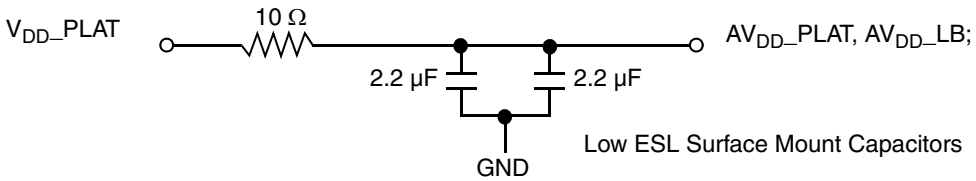
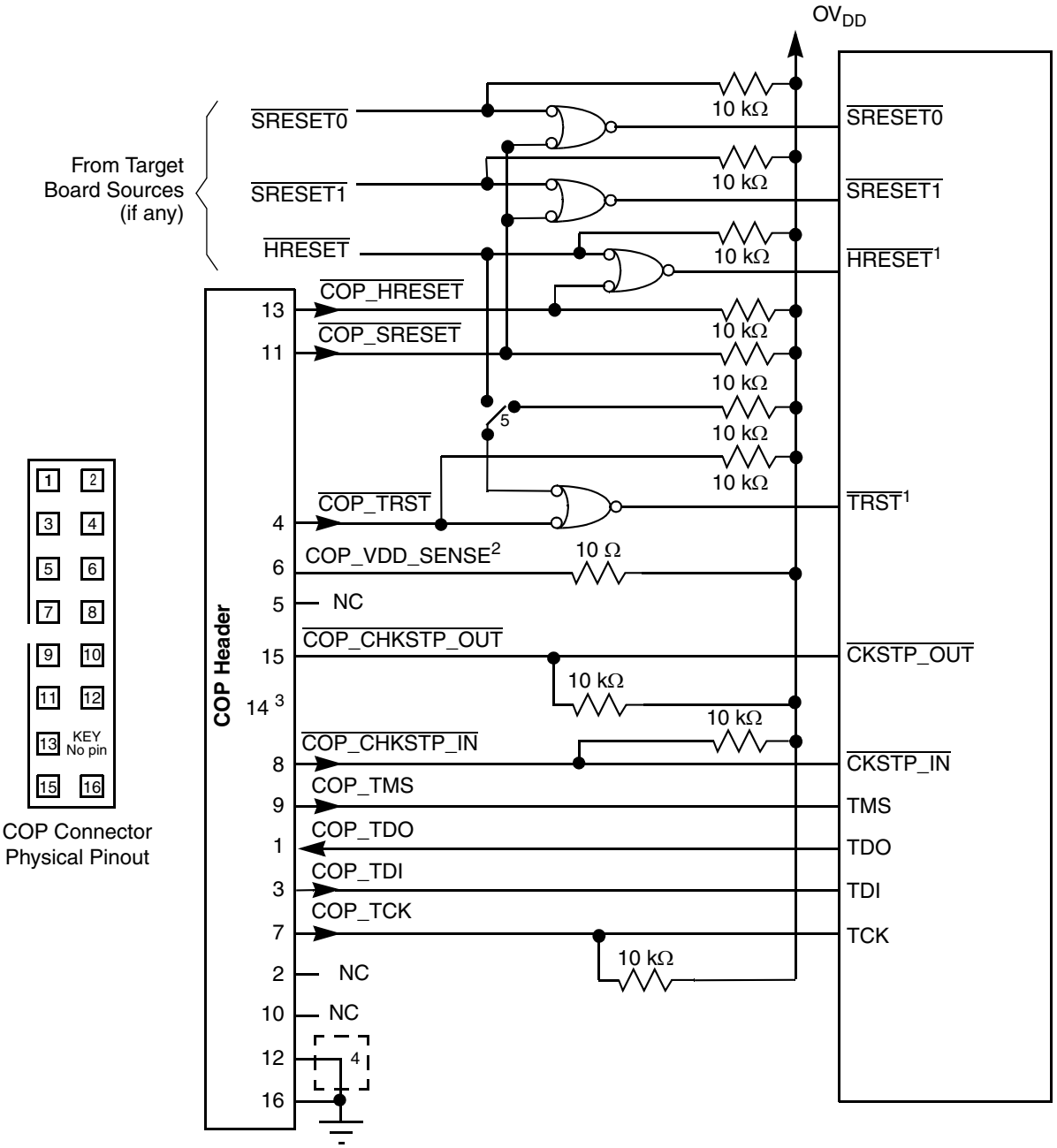


Figure 63. MPC8641 PLL Power Supply Filter Circuit (for platform and Local Bus)



Notes:

1. The COP port and target board should be able to independently assert $\overline{\text{HRESET}}$ and $\overline{\text{TRST}}$ to the processor in order to fully control the processor as shown here.
2. Populate this with a 10 Ω resistor for short-circuit/current-limiting protection.
3. The KEY location (pin 14) is not physically present on the COP header.
4. Although pin 12 is defined as a No-Connect, some debug tools may use pin 12 as an additional GND pin for improved signal integrity.
5. This switch is included as a precaution for BSDL testing. The switch should be open during BSDL testing to avoid accidentally asserting the $\overline{\text{TRST}}$ line. If BSDL testing is not being performed, this switch should be closed or removed.

Figure 68. JTAG/COP Interface Connection for one MPC8641 device