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Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e600
Number of Cores/Bus Width	2 Core, 32-Bit
Speed	1.5GHz
Co-Processors/DSP	-
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (4)
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	1023-BBGA, FCBGA
Supplier Device Package	1023-FCCBGA (33x33)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc8641dhx1500ke

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



Overview



Figure 1. MPC8641 and MPC8641D







Notes:

- 1. Dotted waveforms correspond to optional supply values for a specified power supply. See Table 2.
- 2. The recommended maximum ramp up time for power supplies is 20 milliseconds.
- 3. Refer to Section 5, "RESET Initialization" for additional information on PLL relock and reset signal assertion timing requirements.
- 4. Refer to Table 11 for additional information on reset configuration pin setup timing requirements. In addition see Figure 68 regarding HRESET and JTAG connection details including TRST.
- 5. e600 PLL relock time is 100 microseconds maximum plus 255 MPX_clk cycles.
- 6. Stable PLL configuration signals are required as stable SYSCLK is applied. All other POR configuration inputs are required 4 SYSCLK cycles before HRESET negation and are valid at least 2 SYSCLK cycles after HRESET has negated (hold requirement). See Section 5, "RESET Initialization" for more information on setup and hold time of reset configuration signals.
- V_{DD}_PLAT, AV_{DD}_PLAT must strictly reach 90% of their recommended voltage before the rail for Dn_GV_{DD}, and Dn_MV_{REF} reaches 10% of their recommended voltage.
- 8. SYSCLK must be driven only AFTER the power for the various power supplies is stable.
- In device sleep mode, the reset configuration signals for DRAM types (TSEC2_TXD[4],TSEC2_TX_ER) must be valid BEFORE HRESET is asserted.

Figure 3. MPC8641 Power-Up and Reset Sequence



2

2

2

4

5

0.08

0.70

0.66

0.10

0.45

12.00

9.80

7.70

0.0125

The maximum power dissipation for individual power supplies of the MPC8641D is shown in Table 5.

Supply Voltage Power **Component Description** Notes (Volts) (Watts) Per Core voltage Supply V_{DD}_Core0/V_{DD}_Core1 = 1.1 V @ 1500 MHz 21.00 Per Core PLL voltage supply AV_{DD}_Core0/AV_{DD}_Core1 = 1.1 V @ 1500 MHz 0.0125 Per Core voltage Supply V_{DD}_Core0/V_{DD}_Core1 = 1.05 V @ 1333 MHz 17.00 AV_{DD}_Core0/AV_{DD}_Core1 = 1.05 V @ 1333 MHz Per Core PLL voltage supply 0.0125 Per Core voltage Supply V_{DD}_Core0/V_{DD}_Core1 = 0.95 V @ 1000 MHz 11.50 5 AV_{DD}_Core0/AV_{DD}_Core1 = 0.95 V @ 1000 MHz Per Core PLL voltage supply 0.0125 5 DDR Controller I/O voltage supply Dn_GV_{DD} = 2.5 V @ 400 MHz 0.80 2 Dn_GV_{DD} = 1.8 V @ 533 MHz 2 0.68 Dn_GV_{DD} = 1.8 V @ 600 MHz 0.77 2 $L/TV_{DD} = 3.3 V$ 16-bit FIFO @ 200 MHz 2, 3 0.11

 $L/TV_{DD} = 3.3 V$

 $SV_{DD} = 1.1 V$

 XV_{DD} SRDSn = 1.1 V

 AV_{DD} SRDS1/ AV_{DD} SRDS2 = 1.1 V

OV_{DD} = 3.3 V

V_{DD}_PLAT = 1.1 V @ 600 MHz

V_{DD}_PLAT = 1.05 Vn @ 500 MHz

V_{DD}_PLAT = 1.05 Vn @ 400 MHz

 AV_{DD} PLAT, AV_{DD} LB = 1.1 V

Table 5. MPC8641D Individual Supply Maximum Power Dissipation ¹

Platform source Supply Platform source Supply Platform, Local Bus PLL voltage Supply

eTsec 1&2/3&4 Voltage Supply non-FIFO eTsec*n* Voltage Supply

x8 SerDes transceiver Supply

x8 SerDes I/O Supply

SerDes PLL voltage supply Port 1 or 2

Platform I/O Supply

Platform source Supply

Notes:

1. This is a maximum power supply number which is provided for power supply and board design information. The numbers are based on 100% bus utilization for each component. The components listed are not expected to have 100% bus usage simultaneously for all components. Actual numbers may vary based on activity.

2. Number is based on a per port/interface value.

3. This is based on one eTSEC port used. Since 16-bit FIFO mode involves two ports, the number will need to be multiplied by two for the total. The other eTSEC protocols dissipate less than this number per port. Note that the power needs to be multiplied by the number of ports used for the protocol for the total eTSEC port power dissipation.

4. This includes Local Bus, DUART, I²C, DMA, Multiprocessor Interrupts, System Control & Clocking, Debug, Test, Power management, JTAG and Miscellaneous I/O voltage.

5. These power numbers are for Part Number MC8641xxx1000NX only. V_{DD} _Coren = 0.95 V and V_{DD} _PLAT = 1.05 V.



4 Input Clocks

Table 7 provides the system clock (SYSCLK) DC specifications for the MPC8641.

Table 7. SYSCLK DC Electrical Characteristics (OVDD = 3.3 V ± 165 mV)

Parameter	Symbol	Min	Мах	Unit
High-level input voltage	V _{IH}	2	OV _{DD} + 0.3	V
Low-level input voltage	V _{IL}	-0.3	0.8	V
Input current $(V_{IN}^{1} = 0 V \text{ or } V_{IN} = V_{DD})$	I _{IN}		±5	μA

Note:

1. Note that the symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

4.1 System Clock Timing

Table 8 provides the system clock (SYSCLK) AC timing specifications for the MPC8641.

Table 8. SYSCLK AC Timing Specifications

At recommended operating conditions (see Table 2) with $OV_{DD} = 3.3 \text{ V} \pm 165 \text{ mV}$.

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
SYSCLK frequency	fsysclk	66	—	166.66	MHz	1
SYSCLK cycle time	t _{SYSCLK}	6	—	_	ns	_
SYSCLK rise and fall time	t _{KH} , t _{KL}	0.6	1.0	1.2	ns	2
SYSCLK duty cycle	t _{KHK} /t _{SYSCLK}	40	—	60	%	3
SYSCLK jitter	_			150	ps	4, 5

Notes:

- Caution: The MPX clock to SYSCLK ratio and e600 core to MPX clock ratio settings must be chosen such that the resulting SYSCLK frequency, e600 (core) frequency, and MPX clock frequency do not exceed their respective maximum or minimum operating frequencies. See Section 18.2, "MPX to SYSCLK PLL Ratio," and Section 18.3, "e600 to MPX clock PLL Ratio," for ratio settings.
- 2. Rise and fall times for SYSCLK are measured at 0.4 V and 2.7 V.
- 3. Timing is guaranteed by design and characterization.
- 4. This represents the short term jitter only and is guaranteed by design.
- 5. The SYSCLK driver's closed loop jitter bandwidth should be <500 kHz at -20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track SYSCLK drivers with the specified jitter. Note that the frequency modulation for SYSCLK reduces significantly for the spread spectrum source case. This is to guarantee what is supported based on design.

4.1.1 SYSCLK and Spread Spectrum Sources

Spread spectrum clock sources are an increasingly popular way to control electromagnetic interference emissions (EMI) by spreading the emitted noise to a wider spectrum and reducing the peak noise magnitude in order to meet industry and government requirements. These clock sources intentionally add long-term jitter in order to diffuse the EMI spectral content. The jitter specification given in Table 8 considers short-term (cycle-to-cycle) jitter only and the clock generator's cycle-to-cycle output jitter



Input Clocks

should meet the MPC8641 input cycle-to-cycle jitter requirement. Frequency modulation and spread are separate concerns, and the MPC8641 is compatible with spread spectrum sources if the recommendations listed in Table 9 are observed.

Table 9. Spread Spectrum Clock Source Recommendations

At recommended operating conditions. See Table 2.

Parameter	Min	Мах	Unit	Notes
Frequency modulation	—	50	kHz	1
Frequency spread		1.0	%	1, 2

Notes:

1. Guaranteed by design.

2. SYSCLK frequencies resulting from frequency spreading, and the resulting core and VCO frequencies, must meet the minimum and maximum specifications given in Table 8.

It is imperative to note that the processor's minimum and maximum SYSCLK, core, and VCO frequencies must not be exceeded regardless of the type of clock source. Therefore, systems in which the processor is operated at its maximum rated e600 core frequency should avoid violating the stated limits by using down-spreading only.

 SDn_REF_CLK and $\overline{SDn_REF_CLK}$ was designed to work with a spread spectrum clock (+0 to 0.5% spreading at 30–33kHz rate is allowed), assuming both ends have same reference clock. For better results use a source without significant unintended modulation.

4.2 Real Time Clock Timing

The RTC input is sampled by the platform clock (MPX clock). The output of the sampling latch is then used as an input to the counters of the PIC. There is no jitter specification. The minimum pulse width of the RTC signal should be greater than 2x the period of the MPX clock. That is, minimum clock high time is $2 \times t_{MPX}$, and minimum clock low time is $2 \times t_{MPX}$. There is no minimum RTC frequency; RTC may be grounded if not needed.

4.3 eTSEC Gigabit Reference Clock Timing

Table 10 provides the eTSEC gigabit reference clocks (EC1_GTX_CLK125 and EC2_GTX_CLK125) AC timing specifications for the MPC8641.

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
ECn_GTX_CLK125 frequency	f _{G125}	—	125 ±100 ppm	_	MHz	3
ECn_GTX_CLK125 cycle time	t _{G125}	—	8	_	ns	—
ECn_GTX_CLK125 peak-to-peak jitter	t _{G125J}	—		250	ps	1

Table 10. ECn_GTX_CLK125 AC Timing Specifications

DDR and DDR2 SDRAM

Table 15 provides the recommended operating conditions for the DDR SDRAM component(s) when $Dn_GV_{DD}(typ) = 2.5 \text{ V}.$

Parameter/Condition	Symbol	Min	Мах	Unit	Notes
I/O supply voltage	D <i>n_</i> GV _{DD}	2.375	2.625	V	1
I/O reference voltage	Dn_MV _{REF}	$0.49 \times Dn_GV_{DD}$	$0.51 \times Dn_GV_{DD}$	V	2
I/O termination voltage	V _{TT}	D <i>n</i> _MV _{REF} – 0.04	- 0.04 D <i>n</i> _MV _{REF} + 0.04		3
Input high voltage	V _{IH}	D <i>n</i> _MV _{REF} + 0.15	D <i>n</i> _GV _{DD} + 0.3	V	—
Input low voltage	V _{IL}	-0.3	D <i>n</i> _MV _{REF} - 0.15	V	—
Output leakage current	I _{OZ}	-50	50	μA	4
Output high current (V _{OUT} = 1.95 V)	I _{ОН}	-16.2	—	mA	—
Output low current (V _{OUT} = 0.35 V)	I _{OL}	16.2	_	mA	—

Table	15 DDR	SDRAM DC	Electrical	Characteristics	for Dn	GV	(tvn)	- 251	/
lable	15. DDn	SURAW DC	Electrical	Characteristics			(LYP)	= 2.5	

Notes:

1. Dn_GV_{DD} is expected to be within 50 mV of the DRAM Dn_GV_{DD} at all times.

2. MV_{REF} is expected to be equal to $0.5 \times Dn_{GV_{DD}}$, and to track $Dn_{GV_{DD}}$ DC variations as measured at the receiver. Peak-to-peak noise on $Dn_{MV_{REF}}$ may not exceed ±2% of the DC value.

3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to Dn_MV_{REF}. This rail should track variations in the DC level of Dn_MV_{REF}.

4. Output leakage is measured with all outputs disabled, 0 V \leq V_{OUT} \leq D*n*_GV_{DD}.

Table 16 provides the DDR capacitance when $Dn \text{ }_{\text{DD}}(\text{typ})=2.5 \text{ V}$.

Table 16. DDR SDRAM Capacitance for Dn_GV_{DD} (typ) = 2.5 V

Parameter/Condition	Symbol	Min	Мах	Unit	Notes
Input/output capacitance: DQ, DQS	C _{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS	C _{DIO}	—	0.5	pF	1

Note:

1. This parameter is sampled. $Dn_GV_{DD} = 2.5 V \pm 0.125 V$, f = 1 MHz, $T_A = 25^{\circ}C$, $V_{OUT} = Dn_GVDD/2$, V_{OUT} (peak-to-peak) = 0.2 V.

Table 17 provides the current draw characteristics for MV_{REF} .

Table 17. Current Draw Characteristics for MV_{REF}

Parameter / Condition	Symbol	Min	Max	Unit	Note
Current draw for MV _{REF}	I _{MVREF}	—	500	μA	1

1. The voltage regulator for MV_{REF} must be able to supply up to 500 μA current.



DDR and DDR2 SDRAM

Figure 4 shows the DDR SDRAM input timing for the MDQS to MDQ skew measurement (tDISKEW).



Figure 4. DDR Input Timing Diagram for tDISKEW

6.2.2 DDR SDRAM Output AC Timing Specifications

Table 21. DDR SDRAM Output AC Timing Specifications

At recommended operating conditions.

Parameter	Symbol ¹	Min	Мах	Unit	Notes
MCK[n] cycle time, MCK[n]/MCK[n] crossing	t _{MCK}	3	10	ns	2
MCK duty cycle 600 MHz 533 MHz 400 MHz	^t мскн/t _М ск	47.5 47 47	52.5 53 53	%	8 9 9
ADDR/CMD output setup with respect to MCK	t _{DDKHAS}			ns	3
600 MHz		1.10	—		7
533 MHz		1.48	—		7
400 MHz		1.95	—		
ADDR/CMD output hold with respect to MCK	t _{DDKHAX}			ns	3
600 MHz		1.10	—		7
533 MHz		1.48	—		7
400 MHz		1.95	—		
MCS[n] output setup with respect to MCK	t _{DDKHCS}			ns	3
600 MHz		1.10	—		7
533 MHz		1.48	—		7
400 MHz		1.95	—		



Table 28. GMII Transmit AC Timing Specifications (continued)

At recommended operating conditions with L/TV_{DD} of 3.3 V \pm 5% and 2.5 V \pm 5%.

Parameter/Condition	Symbol ¹	Min	Тур	Max	Unit
GTX_CLK data clock fall time (80%-20%)	t _{GTXF} 2	_		1.0	ns

Notes:

1. The symbols used for timing specifications herein follow the pattern t_{(first two letters of functional block)(signal)(state) (reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{GTKHDV} symbolizes GMII transmit timing (GT) with respect to the t_{GTX} clock reference (K) going to the high state (H) relative to the time date input signals (D) reaching the valid state (V) to state or setup time. Also, t_{GTKHDX} symbolizes GMII transmit timing (GT) with respect to the high state (H) relative to the time date input signals (D) going invalid (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{GTX} represents the GMII(G) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).}}

2. Guaranteed by design.

Figure 10 shows the GMII transmit AC timing diagram.



Figure 10. GMII Transmit AC Timing Diagram

8.2.2.2 GMII Receive AC Timing Specifications

Table 29 provides the GMII receive AC timing specifications.

Table 29. GMII Receive AC Timing Specifications

At recommended operating conditions with L/TV_{DD} of 3.3 V \pm 5% and 2.5 V \pm 5%.

Parameter/Condition	Symbol ¹	Min	Тур	Мах	Unit
RX_CLK clock period	t _{GRX} 3		8.0	—	ns
RX_CLK duty cycle	t _{GRXH} /t _{GRX}	40	—	60	ns
RXD[7:0], RX_DV, RX_ER setup time to RX_CLK	t _{GRDVKH}	2.0	—	—	ns
RXD[7:0], RX_DV, RX_ER hold time to RX_CLK	t _{GRDXKH}	0.5	—	—	ns
RX_CLK clock rise time (20%-80%)	t _{GRXR} 2		_	1.0	ns



Ethernet: Enhanced Three-Speed Ethernet (eTSEC), MII Management

8.2.3.2 MII Receive AC Timing Specifications

Table 31 provides the MII receive AC timing specifications.

Table 31. MII Receive AC Timing Specifications

At recommended operating conditions with L/TV_{DD} of 3.3 V \pm 5%.

Parameter/Condition	Symbol ¹	Min	Тур	Мах	Unit
RX_CLK clock period 10 Mbps	t _{MRX} 2,3	—	400	—	ns
RX_CLK clock period 100 Mbps	t _{MRX} ³	—	40	—	ns
RX_CLK duty cycle	t _{MRXH} /t _{MRX}	35	—	65	%
RXD[3:0], RX_DV, RX_ER setup time to RX_CLK	t _{MRDVKH}	10.0	—	—	ns
RXD[3:0], RX_DV, RX_ER hold time to RX_CLK	t _{MRDXKH}	10.0	—	—	ns
RX_CLK clock rise time (20%-80%)	t _{MRXR} 2	1.0	—	4.0	ns
RX_CLK clock fall time (80%-20%)	t _{MRXF} 2	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of t_{(first two letters of functional block)(signal)(state) (reference)(state)} for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

2. Guaranteed by design.

3. ±100 ppm tolerance on RX_CLK frequency

Figure 14 provides the AC test load for eTSEC.



Figure 14. eTSEC AC Test Load

Figure 15 shows the MII receive AC timing diagram.



Figure 15. MII Receive AC Timing Diagram



8.2.4 TBI AC Timing Specifications

This section describes the TBI transmit and receive AC timing specifications.

8.2.4.1 TBI Transmit AC Timing Specifications

Table 32 provides the TBI transmit AC timing specifications.

Table 32. TBI Transmit AC Timing Specifications

At recommended operating conditions with L/TV_{DD} of 3.3 V \pm 5% and 2.5 V \pm 5%.

Parameter/Condition	Symbol ¹	Min	Тур	Мах	Unit
TCG[9:0] setup time GTX_CLK going high	t _{TTKHDV}	2.0	—	—	ns
TCG[9:0] hold time from GTX_CLK going high	t _{TTKHDX}	1.0	—	—	ns
GTX_CLK rise time (20%-80%)	t _{TTXR} ²	—	—	1.0	ns
GTX_CLK fall time (80%–20%)	t _{TTXF} 2	—	—	1.0	ns

Notes:

1. The symbols used for timing specifications herein follow the pattern of t_{(first two letters of functional block)(signal)(state)(reference)(state)} for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{TTKHDV} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the valid state (V) or setup time. Also, t_{TTKHDX} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the valid state (V) or setup time. Also, t_{TTKHDX} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the invalid state (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{TTX} represents the TBI (T) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

2. Guaranteed by design.

Figure 16 shows the TBI transmit AC timing diagram.



Figure 16. TBI Transmit AC Timing Diagram



8.2.7 RMII AC Timing Specifications

This section describes the RMII transmit and receive AC timing specifications.

8.2.7.1 RMII Transmit AC Timing Specifications

The RMII transmit AC timing specifications are in Table 36.

Table 36. RMII Transmit AC Timing Specifications

At recommended operating conditions with L/TV_{DD} of 3.3 V \pm 5%.

Parameter/Condition	Symbol ¹	Min	Тур	Мах	Unit
REF_CLK clock period	t _{RMT}	—	20.0	—	ns
REF_CLK duty cycle	t _{RMTH} /t _{RMT}	35	50	65	%
REF_CLK peak-to-peak jitter	t _{RMTJ}	—	_	250	ps
Rise time REF_CLK (20%-80%)	t _{RMTR}	1.0	_	2.0	ns
Fall time REF_CLK (80%–20%)	t _{RMTF}	1.0	_	2.0	ns
REF_CLK to RMII data TXD[1:0], TX_EN delay	t _{RMTDX}	1.0	_	10.0	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of t_{(first two letters of functional block)(signal)(state) (reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).}

Figure 20 shows the RMII transmit AC timing diagram.



Figure 20. RMII Transmit AC Timing Diagram



Figure 26 to Figure 31 show the local bus signals.



Figure 26. Local Bus Signals (PLL Enabled)

NOTE

PLL bypass mode is recommended when LBIU frequency is at or below 83 MHz. When LBIU operates above 83 MHz, LBIU PLL is recommended to be enabled.

Table 42 describes the general timing parameters of the local bus interface at $OV_{DD} = 3.3$ V with PLL bypassed.

Table 42. Local Bus	Timing Parameters—F	LL Bypassed
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Parameter	Symbol ¹	Min	Мах	Unit	Notes
Local bus cycle time	t _{LBK}	12	_	ns	2
Local bus duty cycle	t _{LBKH/} t _{LBK}	45	55	%	—
Internal launch/capture clock to LCLK delay	t _{LBKHKT}	2.3	3.9	ns	8
Input setup to local bus clock (except LGTA/LUPWAIT)	t _{LBIVKH1}	5.7	_	ns	4, 5
LGTA/LUPWAIT input setup to local bus clock	t _{LBIVKL2}	5.6	_	ns	4, 5
Input hold from local bus clock (except LGTA/LUPWAIT)	t _{LBIXKH1}	-1.8	_	ns	4, 5



Local Bus



Figure 27. Local Bus Signals (PLL Bypass Mode)

NOTE

In PLL bypass mode, LCLK[n] is the inverted version of the internal clock with the delay of t_{LBKHKT} . In this mode, signals are launched at the rising edge of the internal clock and are captured at falling edge of the internal clock, with the exception of the LGTA/LUPWAIT signal, which is captured at the rising edge of the internal clock.



Figure 43 shows the SerDes reference clock connection reference circuits for HCSL type clock driver. It assumes that the DC levels of the clock driver chip is compatible with MPC8641D SerDes reference clock input's DC requirement.



Figure 43. DC-Coupled Differential Connection with HCSL Clock Driver (Reference Only)

Figure 44 shows the SerDes reference clock connection reference circuits for LVDS type clock driver. Since LVDS clock driver's common mode voltage is higher than the MPC8641D SerDes reference clock input's allowed range (100 to 400 mV), AC-coupled connection scheme must be used. It assumes the LVDS output driver features $50-\Omega$ termination resistor. It also assumes that the LVDS transmitter establishes its own common mode level without relying on the receiver or other external component.



Figure 44. AC-Coupled Differential Connection with LVDS Clock Driver (Reference Only)

Figure 45 shows the SerDes reference clock connection reference circuits for LVPECL type clock driver. Since LVPECL driver's DC levels (both common mode voltages and output swing) are incompatible with



High-Speed Serial Interfaces (HSSI)

13.2.4 AC Requirements for SerDes Reference Clocks

The clock driver selected should provide a high quality reference clock with low phase noise and cycle-to-cycle jitter. Phase noise less than 100 kHz can be tracked by the PLL and data recovery loops and is less of a problem. Phase noise above 15 MHz is filtered by the PLL. The most problematic phase noise occurs in the 1–15 MHz range. The source impedance of the clock driver should be 50 Ω to match the transmission line and reduce reflections which are a source of noise to the system.

Table 47 describes some AC parameters common to PCI Express and Serial RapidIO protocols.

Table 47. SerDes Reference Clock Common AC Parameters

At recommended operating conditions with XV_{DD} _SRDS1 or XV_{DD} _SRDS2 = 1.1V ± 5% and 1.05V ± 5%.

Parameter	Symbol	Min	Max	Unit	Notes
Rising Edge Rate	Rise Edge Rate	1.0	4.0	V/ns	2, 3
Falling Edge Rate	Fall Edge Rate	1.0	4.0	V/ns	2, 3
Differential Input High Voltage	V _{IH}	+200		mV	2
Differential Input Low Voltage	V _{IL}	_	-200	mV	2
Rising edge rate (SD <i>n</i> _REF_CLK) to falling edge rate (SD <i>n</i> _REF_CLK) matching	Rise-Fall Matching	_	20	%	1, 4

Notes:

1. Measurement taken from single ended waveform.

2. Measurement taken from differential waveform.

3. Measured from –200 mV to +200 mV on the differential waveform (derived from SD*n*_REF_CLK minus SD*n*_REF_CLK). The signal must be monotonic through the measurement region for rise and fall time. The 400 mV measurement window is centered on the differential zero crossing. See Figure 47.

4. Matching applies to rising edge rate for SD*n*_REF_CLK and falling edge rate for SD<u>n_REF_CLK</u>. It is measured using a 200 mV window centered on the median cross point where SDn_REF_CLK rising meets SD*n*_REF_CLK falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The Rise Edge Rate of SD*n*_REF_CLK should be compared to the Fall Edge Rate of SD*n*_REF_CLK, the maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 48.



Figure 47. Differential Measurement Points for Rise and Fall Time



PCI Express

Table 49. Differential Transmitter	· (TX) Output S	Specifications	(continued)
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Symbol	Parameter	Min	Nom	Мах	Units	Comments
T _{TX-IDLE-SET-TO-IDLE}	Maximum time to transition to a valid Electrical idle after sending an Electrical Idle ordered set		_	20	UI	After sending an Electrical Idle ordered set, the Transmitter must meet all Electrical Idle Specifications within this time. This is considered a debounce time for the Transmitter to meet Electrical Idle after transitioning from L0.
T _{TX-IDLE-TO-DIFF-DATA}	Maximum time to transition to valid TX specifications after leaving an Electrical idle condition			20	UI	Maximum time to meet all TX specifications when transitioning from Electrical Idle to sending differential data. This is considered a debounce time for the TX to meet all TX specifications after leaving Electrical Idle
RL _{TX-DIFF}	Differential Return Loss	12	—	—	dB	Measured over 50 MHz to 1.25 GHz. See Note 4
RL _{TX-CM}	Common Mode Return Loss	6	—	—	dB	Measured over 50 MHz to 1.25 GHz. See Note 4
Z _{TX-DIFF-DC}	DC Differential TX Impedance	80	100	120	Ω	TX DC Differential mode Low Impedance
Z _{TX-DC}	Transmitter DC Impedance	40	—	—	Ω	Required TX D+ as well as D- DC Impedance during all states
L _{TX-SKEW}	Lane-to-Lane Output Skew	_	—	500 + 2 UI	ps	Static skew between any two Transmitter Lanes within a single Link
C _{TX}	AC Coupling Capacitor	75	—	—	nF	All Transmitters shall be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. See Note 8.
T _{crosslink}	Crosslink Random Timeout	0			ms	This random timeout helps resolve conflicts in crosslink configuration by eventually resulting in only one Downstream and one Upstream Port. See Note 7.

Notes:

1. No test load is necessarily associated with this value.

- 2. Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 52 and measured over any 250 consecutive TX UIs. (Also refer to the transmitter compliance eye diagram shown in Figure 50)
- 3. A T_{TX-EYE} = 0.70 UI provides for a total sum of deterministic and random jitter budget of T_{TX-JITTER-MAX} = 0.30 UI for the Transmitter collected over any 250 consecutive TX UIs. The T_{TX-EYE-MEDIAN-to-MAX-JITTER} median is less than half of the total TX jitter budget collected over any 250 consecutive TX UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.
- 4. The Transmitter input impedance shall result in a differential return loss greater than or equal to 12 dB and a common mode return loss greater than or equal to 6 dB over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements is 50 Ω to ground for both the D+ and D- line (that is, as measured by a Vector Network Analyzer with 50 ohm probes—see Figure 52). Note that the series capacitors C_{TX} is optional for the return loss measurement.
- 5. Measured between 20-80% at transmitter package pins into a test load as shown in Figure 52 for both V_{TX-D+} and V_{TX-D-} .
- 6. See Section 4.3.1.8 of the PCI Express Base Specifications Rev 1.0a
- 7. See Section 4.2.6.3 of the PCI Express Base Specifications Rev 1.0a
- 8. MPC8641D SerDes transmitter does not have C_{TX} built-in. An external AC Coupling capacitor is required.



Symbol	Parameter	Min	Nom	Max	Units	Comments
T _{RX-IDLE-DET-DIFF-} ENTERTIME	Unexpected Electrical Idle Enter Detect Threshold Integration Time			10	ms	An unexpected Electrical Idle ($V_{RX-DIFFp-p} < V_{RX-IDLE-DET-DIFFp-p}$) must be recognized no longer than $T_{RX-IDLE-DET-DIFF-ENTERING}$ to signal an unexpected idle condition.
L _{TX-SKEW}	Total Skew			20	ns	Skew across all lanes on a Link. This includes variation in the length of SKP ordered set (for example, COM and one to five Symbols) at the RX as well as any delay differences arising from the interconnect itself.

Notes:

- 1. No test load is necessarily associated with this value.
- 2. Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 52 should be used as the RX device when taking measurements (also refer to the Receiver compliance eye diagram shown in Figure 51). If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.
- 3. A T_{RX-EYE} = 0.40 UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the Transmitter and interconnect collected any 250 consecutive UIs. The T_{RX-EYE-MEDIAN-to-MAX-JITTER} specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total. UI jitter budget collected over any 250 consecutive TX UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as the reference for the eye diagram.
- 4. The Receiver input impedance shall result in a differential return loss greater than or equal to 15 dB with the D+ line biased to 300 mV and the D- line biased to -300 mV and a common mode return loss greater than or equal to 6 dB (no bias required) over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements for is 50 Ω to ground for both the D+ and D- line (that is, as measured by a Vector Network Analyzer with 50 ohm probes see Figure 52). Note: that the series capacitors C_{TX} is optional for the return loss measurement.
- 5. Impedance during all LTSSM states. When transitioning from a Fundamental Reset to Detect (the initial state of the LTSSM) there is a 5 ms transition time before Receiver termination values must be met on all un-configured Lanes of a Port.
- 6. The RX DC Common Mode Impedance that exists when no power is present or Fundamental Reset is asserted. This helps ensure that the Receiver Detect circuit will not falsely assume a Receiver is powered on when it is not. This term must be measured at 300 mV above the RX ground.
- 7. It is recommended that the recovered TX UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function. Least squares and median deviation fits have worked well with experimental and simulated data.

14.5 Receiver Compliance Eye Diagrams

The RX eye diagram in Figure 51 is specified using the passive compliance/test measurement load (see Figure 52) in place of any real PCI Express RX component.

Note: In general, the minimum Receiver eye diagram measured with the compliance/test measurement load (see Figure 52) will be larger than the minimum Receiver eye diagram measured over a range of systems at the input Receiver of any real PCI Express component. The degraded eye diagram at the input Receiver is due to traces internal to the package as well as silicon parasitic characteristics which cause the real PCI Express component to vary in impedance from the compliance/test measurement load. The input Receiver eye diagram is implementation specific and is not specified. RX component designer should





Figure 52. Compliance Test/Measurement Load

15 Serial RapidIO

This section describes the DC and AC electrical specifications for the RapidIO interface of the MPC8641, for the LP-Serial physical layer. The electrical specifications cover both single and multiple-lane links. Two transmitter types (short run and long run) on a single receiver are specified for each of three baud rates, 1.25, 2.50, and 3.125 GBaud.

Two transmitter specifications allow for solutions ranging from simple board-to-board interconnect to driving two connectors across a backplane. A single receiver specification is given that will accept signals from both the short run and long run transmitter specifications.

The short run transmitter specifications should be used mainly for chip-to-chip connections on either the same printed circuit board or across a single connector. This covers the case where connections are made to a mezzanine (daughter) card. The minimum swings of the short run specification reduce the overall power used by the transceivers.

The long run transmitter specifications use larger voltage swings that are capable of driving signals across backplanes. This allows a user to drive signals across two connectors and a backplane. The specifications allow a distance of at least 50 cm at all baud rates.

All unit intervals are specified with a tolerance of +/-100 ppm. The worst case frequency difference between any transmit and receive clock will be 200 ppm.

To ensure interoperability between drivers and receivers of different vendors and technologies, AC coupling at the receiver input must be used.

15.1 DC Requirements for Serial RapidIO SD*n*_REF_CLK and SD*n*_REF_CLK

For more information, see Section 13.2, "SerDes Reference Clocks."

15.2 AC Requirements for Serial RapidIO SD*n*_REF_CLK and SD*n*_REF_CLK

Table 51 lists AC requirements.



Serial RapidIO

Characteristic	Symbol	Ra	nge	Unit	Notes
Characteristic	Symbol	Min	Мах	Onit	Notes
Output Voltage,	Vo	-0.40	2.30	Volts	Voltage relative to COMMON of either signal comprising a differential pair
Differential Output Voltage	V _{DIFFPP}	500	1000	mV p-p	_
Deterministic Jitter	J _D	—	0.17	UI p-p	—
Total Jitter	J _T	—	0.35	UI p-p	—
Multiple output skew	S _{MO}	_	1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	800	800	ps	+/– 100 ppm

Table 52. Short Run Transmitter AC Timing Specifications—1.25 GBaud

Table 53. Short Run Transmitter AC Timing Specifications—2.5 GBaud

Characteristic	Symbol	Ra	nge	Unit	Notoo	
Characteristic	Symbol	Min	Мах	Onic	Notes	
Output Voltage,	Vo	-0.40	2.30	Volts	Voltage relative to COMMON of either signal comprising a differential pair	
Differential Output Voltage	V _{DIFFPP}	500	1000	mV p-p	_	
Deterministic Jitter	J _D	—	0.17	UI p-p	—	
Total Jitter	J _T	—	0.35	UI p-p	—	
Multiple Output skew	S _{MO}	—	1000	ps	Skew at the transmitter output between lanes of a multilane link	
Unit Interval	UI	400	400	ps	+/– 100 ppm	

Table 54. Short Run Transmitter AC Timing Specifications—3.125 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max	Onic	notes
Output Voltage,	Vo	-0.40	2.30	Volts	Voltage relative to COMMON of either signal comprising a differential pair
Differential Output Voltage	V _{DIFFPP}	500	1000	mV p-p	_
Deterministic Jitter	J _D	—	0.17	UI p-p	—
Total Jitter	J _T	—	0.35	UI p-p	—



System Design Information



Notes:

- 1. The COP port and target board should be able to independently assert HRESET and TRST to the processor in order to fully control the processor as shown here.
- 2. Populate this with a 10 Ω resistor for short-circuit/current-limiting protection.
- 3. The KEY location (pin 14) is not physically present on the COP header.
- 4. Although pin 12 is defined as a No-Connect, some debug tools may use pin 12 as an additional GND pin for improved signal integrity.
- This switch is included as a precaution for BSDL testing. The switch should be open during BSDL testing to avoid accidentally asserting the TRST line. If BSDL testing is not being performed, this switch should be closed or removed.

Figure 68. JTAG/COP Interface Connection for one MPC8641 device