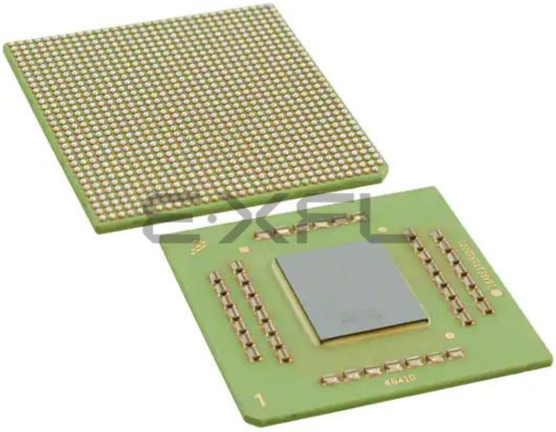

Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e600
Number of Cores/Bus Width	2 Core, 32-Bit
Speed	1.25GHz
Co-Processors/DSP	-
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (4)
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	-
Package / Case	1023-BBGA, FCBGA
Supplier Device Package	1023-FCCBGA (33x33)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc8641dthx1250he

  - Support for PCI-Express message-shared interrupts (MSIs)
- Local bus controller (LBC)
  - Multiplexed 32-bit address and data operating at up to 133 MHz
  - Eight chip selects support eight external slaves
- Integrated DMA controller
  - Four-channel controller
  - All channels accessible by both the local and the remote masters
  - Supports transfers to or from any local memory or I/O port
  - Ability to start and flow control each DMA channel from external 3-pin interface
- Device performance monitor
  - Supports eight 32-bit counters that count the occurrence of selected events
  - Ability to count up to 512 counter-specific events
  - Supports 64 reference events that can be counted on any of the 8 counters
  - Supports duration and quantity threshold counting
  - Burstiness feature that permits counting of burst events with a programmable time between bursts
  - Triggering and chaining capability
  - Ability to generate an interrupt on overflow
- Dual I^2C controllers
  - Two-wire interface
  - Multiple master support
  - Master or slave I^2C mode support
  - On-chip digital filtering rejects spikes on the bus
- Boot sequencer
  - Optionally loads configuration data from serial ROM at reset via the I^2C interface
  - Can be used to initialize configuration registers and/or memory
  - Supports extended I^2C addressing mode
  - Data integrity checked with preamble signature and CRC
- DUART
  - Two 4-wire interfaces (SIN, SOUT, $\overline{\text{RTS}}$, $\overline{\text{CTS}}$)
  - Programming model compatible with the original 16450 UART and the PC16550D
- IEEE 1149.1-compatible, JTAG boundary scan
- Available as 1023 pin Hi-CTE flip chip ceramic ball grid array (FC-CBGA)

Table 10. EC*n*_GTX_CLK125 AC Timing Specifications (continued)

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
EC*n*_GTX_CLK125 duty cycle GMII, TBI 1000Base-T for RGMII, RTBI	t_{G125H}/t_{G125}	 45 47	—	 55 53	%	1, 2

Notes:
1. Timing is guaranteed by design and characterization.
2. EC*n*_GTX_CLK125 is used to generate the GTX clock for the eTSEC transmitter with 2% degradation. EC*n*_GTX_CLK125 duty cycle can be loosened from 47/53% as long as the PHY device can tolerate the duty cycle generated by the eTSEC GTX_CLK. See Section 8.2.6, "RGMII and RTBI AC Timing Specifications," for duty cycle for 10Base-T and 100Base-T reference clock.
3. ±100 ppm tolerance on EC*n*_GTX_CLK125 frequency

NOTE

The phase between the output clocks TSEC1_GTX_CLK and TSEC2_GTX_CLK (ports 1 and 2) is no more than 100 ps. The phase between the output clocks TSEC3_GTX_CLK and TSEC4_GTX_CLK (ports 3 and 4) is no more than 100 ps.

4.4 Platform Frequency Requirements for PCI-Express and Serial RapidIO

The MPX platform clock frequency must be considered for proper operation of the high-speed PCI Express and Serial RapidIO interfaces as described below.

For proper PCI Express operation, the MPX clock frequency must be greater than or equal to:

$$\frac{527\text{ MHz} \times (\text{PCI-Express link width})}{16 / (1 + \text{cfg\_plat\_freq})}$$

Note that at MPX = 400 MHz, cfg_plat_freq = 0 and at MPX > 400 MHz, cfg_plat_freq = 1. Therefore, when operating PCI Express in x8 link width, the MPX platform frequency must be 400 MHz with cfg_plat_freq = 0 or greater than or equal to 527 MHz with cfg_plat_freq = 1.

For proper Serial RapidIO operation, the MPX clock frequency must be greater than or equal to:

$$\frac{2 \times (0.8512) \times (\text{Serial RapidIO interface frequency}) \times (\text{Serial RapidIO link width})}{64}$$

4.5 Other Input Clocks

For information on the input clocks of other functional blocks of the platform such as SerDes, and eTSEC, see the specific section of this document.

5 RESET Initialization

This section describes the AC electrical specifications for the RESET initialization timing requirements of the MPC8641. Table 11 provides the RESET initialization AC timing specifications.

Table 11. RESET Initialization Timing Specifications

Parameter/Condition	Min	Max	Unit	Notes
Required assertion time of $\overline{\text{HRESET}}$	100	—	µs	—
Minimum assertion time for $\overline{\text{SRESET\_0}}$ & $\overline{\text{SRESET\_1}}$	3	—	SYSCLKs	1
Platform PLL input setup time with stable SYSCLK before $\overline{\text{HRESET}}$ negation	100	—	µs	2
Input setup time for POR configs (other than PLL config) with respect to negation of $\overline{\text{HRESET}}$	4	—	SYSCLKs	1
Input hold time for all POR configs (including PLL config) with respect to negation of $\overline{\text{HRESET}}$	2	—	SYSCLKs	1
Maximum valid-to-high impedance time for actively driven POR configs with respect to negation of $\overline{\text{HRESET}}$	—	5	SYSCLKs	1

Notes:

1. SYSCLK is the primary clock input for the MPC8641.

2 This is related to $\overline{\text{HRESET}}$ assertion time. Stable PLL configuration inputs are required when a stable SYSCLK is applied. See the *MPC8641D Integrated Host Processor Reference Manual* for more details on the power-on reset sequence.

Table 12 provides the PLL lock times.

Table 12. PLL Lock Times

Parameter/Condition	Min	Max	Unit	Notes
(Platform and E600) PLL lock times	—	100	µs	1
Local bus PLL	—	50	µs	—

Note:

1.The PLL lock time for e600 PLLs require an additional 255 MPX_CLK cycles.

Table 15 provides the recommended operating conditions for the DDR SDRAM component(s) when D*n*_GV$_{\text{DD}}$(typ) = 2.5 V.

Table 15. DDR SDRAM DC Electrical Characteristics for D*n*_GV$_{\text{DD}}$ (typ) = 2.5 V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
I/O supply voltage	D*n*_GV$_{\text{DD}}$	2.375	2.625	V	1
I/O reference voltage	D*n*_MV$_{\text{REF}}$	0.49 × D*n*_GV$_{\text{DD}}$	0.51 × D*n*_GV$_{\text{DD}}$	V	2
I/O termination voltage	V$_{\text{TT}}$	D*n*_MV$_{\text{REF}}$ – 0.04	D*n*_MV$_{\text{REF}}$ + 0.04	V	3
Input high voltage	V$_{\text{IH}}$	D*n*_MV$_{\text{REF}}$ + 0.15	D*n*_GV$_{\text{DD}}$ + 0.3	V	—
Input low voltage	V$_{\text{IL}}$	–0.3	D*n*_MV$_{\text{REF}}$– 0.15	V	—
Output leakage current	I$_{\text{OZ}}$	–50	50	μA	4
Output high current (V$_{\text{OUT}}$ = 1.95 V)	I$_{\text{OH}}$	–16.2	—	mA	—
Output low current (V$_{\text{OUT}}$ = 0.35 V)	I$_{\text{OL}}$	16.2	—	mA	—

Notes:

1. D*n*_GV$_{\text{DD}}$ is expected to be within 50 mV of the DRAM D*n*_GV$_{\text{DD}}$ at all times.
2. MV$_{\text{REF}}$ is expected to be equal to 0.5 × D*n*_GV$_{\text{DD}}$, and to track D*n*_GV$_{\text{DD}}$ DC variations as measured at the receiver. Peak-to-peak noise on D*n*_MV$_{\text{REF}}$ may not exceed ±2% of the DC value.
3. V$_{\text{TT}}$ is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to D*n*_MV$_{\text{REF}}$ This rail should track variations in the DC level of D*n*_MV$_{\text{REF}}$
4. Output leakage is measured with all outputs disabled, 0 V ≤ V$_{\text{OUT}}$ ≤ D*n*_GV$_{\text{DD}}$.

Table 16 provides the DDR capacitance when D*n*_GV$_{\text{DD}}$ (typ)=2.5 V.

Table 16. DDR SDRAM Capacitance for D*n*_GV$_{\text{DD}}$ (typ) = 2.5 V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input/output capacitance: DQ, DQS	C$_{\text{IO}}$	6	8	pF	1
Delta input/output capacitance: DQ, DQS	C$_{\text{DIO}}$	—	0.5	pF	1

Note:

1. This parameter is sampled. D*n*_GV$_{\text{DD}}$ = 2.5 V ± 0.125 V, f = 1 MHz, T$_{\text{A}}$ = 25°C, V$_{\text{OUT}}$ = D*n*_GVDD/2, V$_{\text{OUT}}$ (peak-to-peak) = 0.2 V.

Table 17 provides the current draw characteristics for MV$_{\text{REF}}$.

Table 17. Current Draw Characteristics for MV$_{\text{REF}}$

Parameter / Condition	Symbol	Min	Max	Unit	Note
Current draw for MV$_{\text{REF}}$	I$_{\text{MVREF}}$	—	500	μA	1

1. The voltage regulator for MV$_{\text{REF}}$ must be able to supply up to 500 μA current.

Figure 4 shows the DDR SDRAM input timing for the MDQS to MDQ skew measurement (tDISKEW).

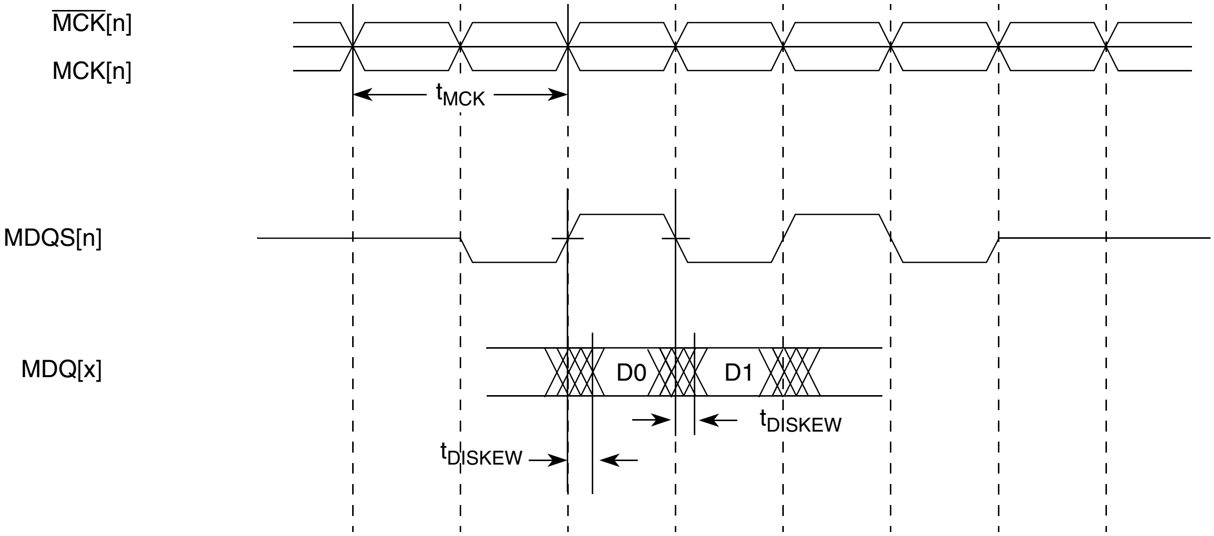

Figure 4. DDR Input Timing Diagram for tDISKEW

6.2.2 DDR SDRAM Output AC Timing Specifications

Table 21. DDR SDRAM Output AC Timing Specifications

At recommended operating conditions.

Parameter	Symbol [1]	Min	Max	Unit	Notes
MCK[n] cycle time, MCK[n]/$\overline{\text{MCK}}$[n] crossing	t_{MCK}	3	10	ns	2
MCK duty cycle	t_{MCKH}/t_{MCK}			%	
600 MHz		47.5	52.5		8
533 MHz		47	53		9
400 MHz		47	53		9
ADDR/CMD output setup with respect to MCK	t_{DDKHAS}			ns	3
600 MHz		1.10	—		7
533 MHz		1.48	—		7
400 MHz		1.95	—		
ADDR/CMD output hold with respect to MCK	t_{DDKHAX}			ns	3
600 MHz		1.10	—		7
533 MHz		1.48	—		7
400 MHz		1.95	—		
$\overline{\text{MCS}}$[n] output setup with respect to MCK	t_{DDKHCS}			ns	3
600 MHz		1.10	—		7
533 MHz		1.48	—		7
400 MHz		1.95	—		

Figure 7 provides the AC test load for the DDR bus.

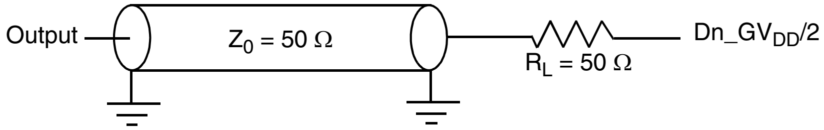

Figure 7. DDR AC Test Load

7 DUART

This section describes the DC and AC electrical specifications for the DUART interface of the MPC8641.

7.1 DUART DC Electrical Characteristics

Table 22 provides the DC electrical characteristics for the DUART interface.

Table 22. DUART DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	–0.3	0.8	V
Input current (V_{IN} [1] = 0 V or V_{IN} = V_{DD})	I_{IN}	—	±5	μA
High-level output voltage (OV_{DD} = min, I_{OH} = –100 μA)	V_{OH}	OV_{DD} – 0.2	—	V
Low-level output voltage (OV_{DD} = min, I_{OL} = 100 μA)	V_{OL}	—	0.2	V

Note:

1. Note that the symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

7.2 DUART AC Electrical Specifications

Table 23 provides the AC timing parameters for the DUART interface.

Table 23. DUART AC Timing Specifications

Parameter	Value	Unit	Notes
Minimum baud rate	MPX clock/1,048,576	baud	1,2
Maximum baud rate	MPX clock/16	baud	1,3
Oversample rate	16	—	1,4

Notes:

1. Guaranteed by design.
2. MPX clock refers to the platform clock.
3. Actual attainable baud rate will be limited by the latency of interrupt processing.
4. The middle of a start bit is detected as the 8th sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16th sample.

8.2.4.2 TBI Receive AC Timing Specifications

Table 33 provides the TBI receive AC timing specifications.

Table 33. TBI Receive AC Timing Specifications

At recommended operating conditions with L/TV_{DD} of 3.3 V ± 5% and 2.5 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
PMA_RX_CLK[0:1] clock period	t_{TRX}[3]	—	16.0	—	ns
PMA_RX_CLK[0:1] skew	t_{SKTRX}	7.5	—	8.5	ns
PMA_RX_CLK[0:1] duty cycle	t_{TRXH}/t_{TRX}	40	—	60	%
RCG[9:0] setup time to rising PMA_RX_CLK	t_{TRDVKH}	2.5	—	—	ns
RCG[9:0] hold time to rising PMA_RX_CLK	t_{TRDXKH}	1.5	—	—	ns
PMA_RX_CLK[0:1] clock rise time (20%-80%)	t_{TRXR}[2]	0.7	—	2.4	ns
PMA_RX_CLK[0:1] clock fall time (80%-20%)	t_{TRXF}[2]	0.7	—	2.4	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{TRDVKH} symbolizes TBI receive timing (TR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{TRX} clock reference (K) going to the high (H) state or setup time. Also, t_{TRDXKH} symbolizes TBI receive timing (TR) with respect to the time data input signals (D) went invalid (X) relative to the t_{TRX} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{TRX} represents the TBI (T) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall). For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (TRX).
2. Guaranteed by design.
3. ±100 ppm tolerance on PMA_RX_CLK[0:1] frequency

Figure 17 shows the TBI receive AC timing diagram.

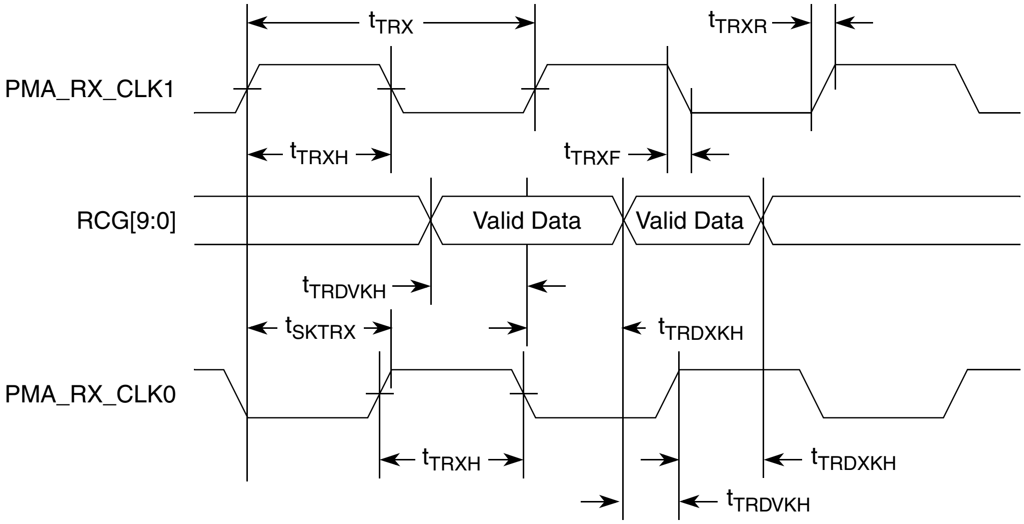

Figure 17. TBI Receive AC Timing Diagram

8.2.5 TBI Single-Clock Mode AC Specifications

When the eTSEC is configured for TBI modes, all clocks are supplied from external sources to the relevant eTSEC interface. In single-clock TBI mode, when TBICON[CLKSEL] = 1 a 125-MHz TBI receive clock is supplied on TSEC*n*_RX_CLK pin (no receive clock is used on TSEC*n*_TX_CLK in this mode, whereas for the dual-clock mode this is the PMA1 receive clock). The 125-MHz transmit clock is applied on the TSEC_GTX_CLK125 pin in all TBI modes.

A summary of the single-clock TBI mode AC specifications for receive appears in Table 34.

Table 34. TBI single-clock Mode Receive AC Timing Specification

At recommended operating conditions with L/TV$_{DD}$ of 3.3 V ± 5% and 2.5 V ± 5%.

Parameter/Condition	Symbol	Min	Typ	Max	Unit
RX_CLK clock period	t_{TRR}[1]	7.5	8.0	8.5	ns
RX_CLK duty cycle	t_{TRRH}/t_{TRR}	40	50	60	%
RX_CLK peak-to-peak jitter	t_{TRRJ}	—	—	250	ps
Rise time RX_CLK (20%–80%)	t_{TRRR}	—	—	1.0	ns
Fall time RX_CLK (80%–20%)	t_{TRRF}	—	—	1.0	ns
RCG[9:0] setup time to RX_CLK rising edge	$t_{TRRDVKH}$	2.0	—	—	ns
RCG[9:0] hold time to RX_CLK rising edge	$t_{TRRDXKH}$	1.0	—	—	ns

[1] ±100 ppm tolerance on RX_CLK frequency

A timing diagram for TBI receive appears in Figure 18.

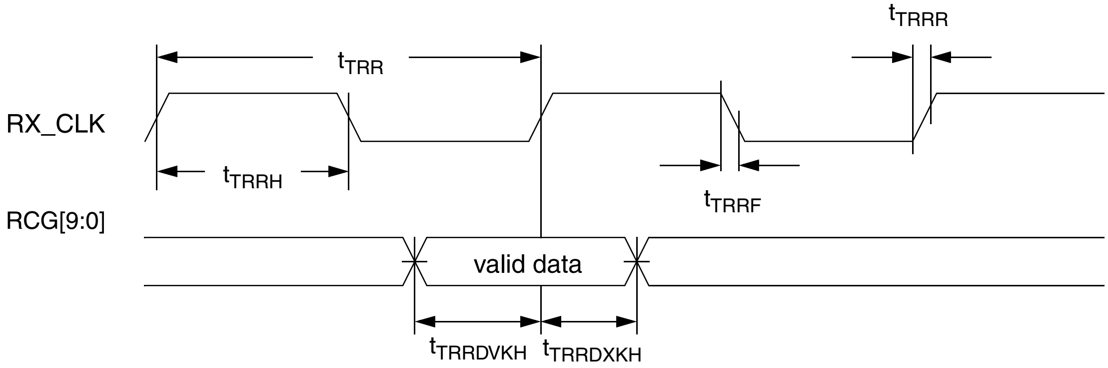

Figure 18. TBI Single-Clock Mode Receive AC Timing Diagram

8.2.6 RGMII and RTBI AC Timing Specifications

Table 35 presents the RGMII and RTBI AC timing specifications.

Table 35. RGMII and RTBI AC Timing Specifications

At recommended operating conditions with L/TV$_{DD}$ of 2.5 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
Data to clock output skew (at transmitter)	t_{SKRGT}[5]	–500	0	500	ps
Data to clock input skew (at receiver) [2]	t_{SKRGT}	1.0	—	2.8	ns

Table 39. MII Management AC Timing Specifications (continued)

At recommended operating conditions with OV_{DD} is 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit	Notes
MDIO to MDC hold time	t_{MDDXKH}	0	—	—	ns	—
MDC rise time	t_{MDCR}	—	—	10	ns	4
MDC fall time	t_{MDHF}	—	—	10	ns	4

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. This parameter is dependent on the system clock speed. (The maximum frequency is the maximum platform frequency divided by 64.)
3. This parameter is dependent on the system clock speed. (That is, for a system clock of 267 MHz, the maximum frequency is 8.3 MHz and the minimum frequency is 1.2 MHz; for a system clock of 375 MHz, the maximum frequency is 11.7 MHz and the minimum frequency is 1.7 MHz.)
4. Guaranteed by design.
5. t_{MPXCLK} is the platform (MPX) clock

Figure 23 provides the AC test load for eTSEC.

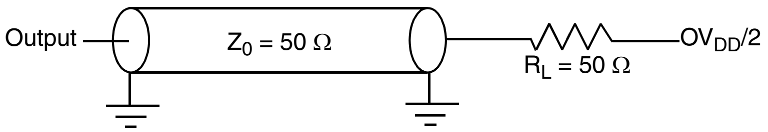

Figure 23. eTSEC AC Test Load

NOTE

Output will see a 50-Ω load since what it sees is the transmission line.

Figure 24 shows the MII management AC timing diagram.

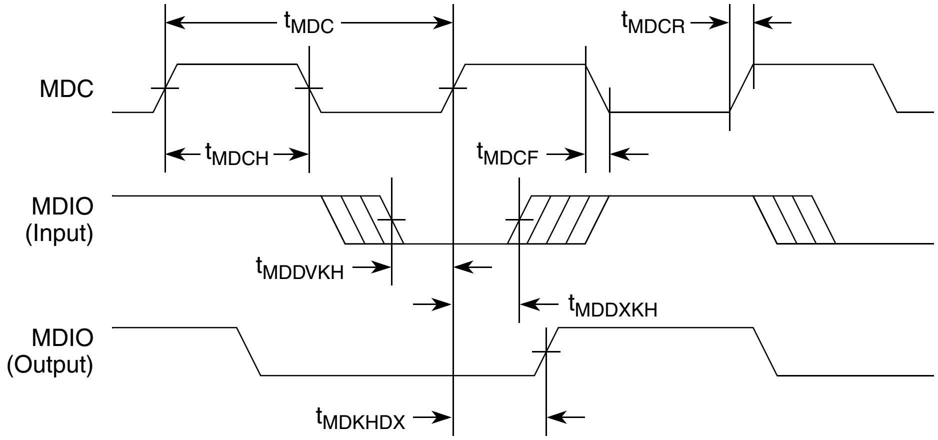

Figure 24. MII Management Interface Timing Diagram

Table 44. JTAG AC Timing Specifications (Independent of SYSCLK) [1] (continued)

At recommended operating conditions (see Table 3).

Parameter	Symbol [2]	Min	Max	Unit	Notes
Output hold times:				ns	
Boundary-scan data	t_{JTKLDX}	30	—		5, 6
TDO	t_{JTKLOX}	30	—		
JTAG external clock to output high impedance:				ns	
Boundary-scan data	t_{JTKLDZ}	3	19		5, 6
TDO	t_{JTKLOZ}	3	9		

Notes:

1. All outputs are measured from the midpoint voltage of the falling/rising edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 32). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
3. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
4. Non-JTAG signal input timing with respect to t_{TCLK}.
5. Non-JTAG signal output timing with respect to t_{TCLK}.
6. Guaranteed by design.

Figure 32 provides the AC test load for TDO and the boundary-scan outputs.

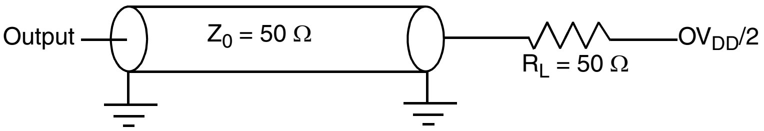

Figure 32. AC Test Load for the JTAG Interface

Figure 33 provides the JTAG clock input timing diagram.

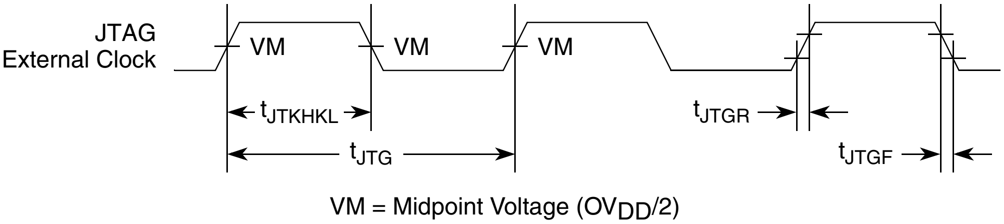

Figure 33. JTAG Clock Input Timing Diagram

13.2.3 Interfacing With Other Differential Signaling Levels

With on-chip termination to SGND, the differential reference clocks inputs are HCSL (High-Speed Current Steering Logic) compatible DC-coupled.

Many other low voltage differential type outputs like LVDS (Low Voltage Differential Signaling) can be used but may need to be AC-coupled due to the limited common mode input range allowed (100 to 400 mV) for DC-coupled connection.

LVPECL outputs can produce signal with too large amplitude and may need to be DC-biased at clock driver output first, then followed with series attenuation resistor to reduce the amplitude, in addition to AC-coupling.

NOTE

Figure 43 to Figure 46 below are for conceptual reference only. Due to the fact that clock driver chip's internal structure, output impedance and termination requirements are different between various clock driver chip manufacturers, it is very possible that the clock circuit reference designs provided by clock driver chip vendor are different from what is shown below. They might also vary from one vendor to the other. Therefore, Freescale Semiconductor can neither provide the optimal clock driver reference circuits, nor guarantee the correctness of the following clock driver connection reference circuits. The system designer is recommended to contact the selected clock driver chip vendor for the optimal reference circuits with the MPC8641D SerDes reference clock receiver requirement provided in this document.

MPC8641D SerDes reference clock input's DC requirement, AC-coupling has to be used. Figure 45 assumes that the LVPECL clock driver's output impedance is 50 Ω. R1 is used to DC-bias the LVPECL outputs prior to AC-coupling. Its value could be ranged from 140 Ω to 240 Ω depending on clock driver vendor's requirement. R2 is used together with the SerDes reference clock receiver's 50-Ω termination resistor to attenuate the LVPECL output's differential peak level such that it meets the MPC8641D SerDes reference clock's differential input amplitude requirement (between 200 mV and 800 mV differential peak). For example, if the LVPECL output's differential peak is 900 mV and the desired SerDes reference clock input amplitude is selected as 600mV, the attenuation factor is 0.67, which requires R2 = 25 Ω. Please consult clock driver chip manufacturer to verify whether this connection scheme is compatible with a particular clock driver chip.

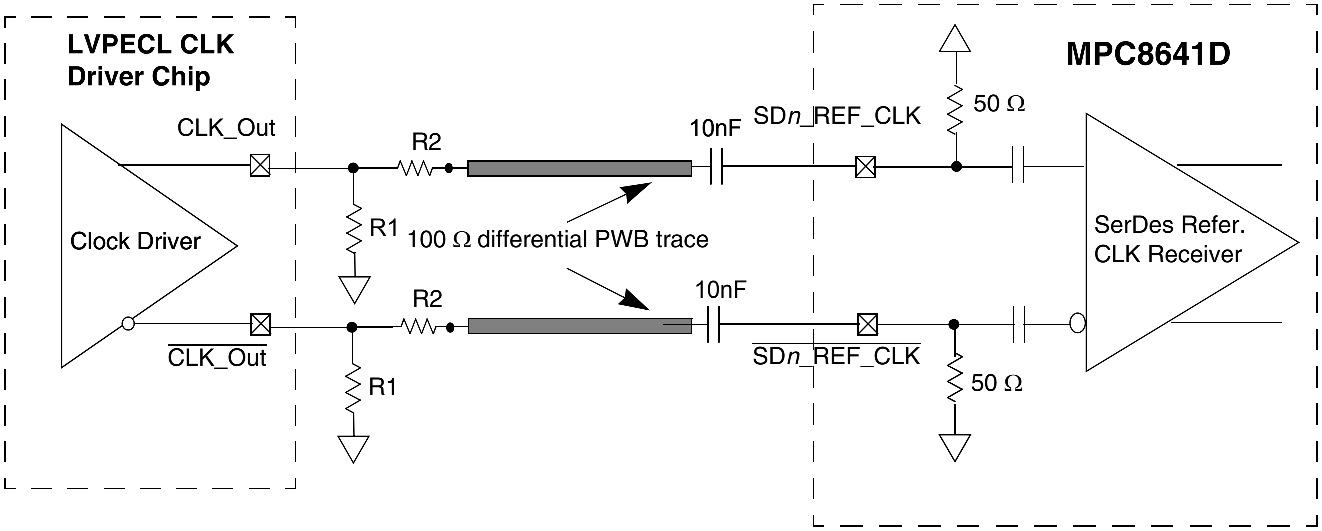

Figure 45. AC-Coupled Differential Connection with LVPECL Clock Driver (Reference Only)

14.4.2 Transmitter Compliance Eye Diagrams

The TX eye diagram in Figure 50 is specified using the passive compliance/test measurement load (see Figure 52) in place of any real PCI Express interconnect + RX component.

There are two eye diagrams that must be met for the transmitter. Both eye diagrams must be aligned in time using the jitter median to locate the center of the eye diagram. The different eye diagrams will differ in voltage depending whether it is a transition bit or a de-emphasized bit. The exact reduced voltage level of the de-emphasized bit will always be relative to the transition bit.

The eye diagram must be valid for any 250 consecutive UIs.

A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.

NOTE

It is recommended that the recovered TX UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function (that is, least squares and median deviation fits).

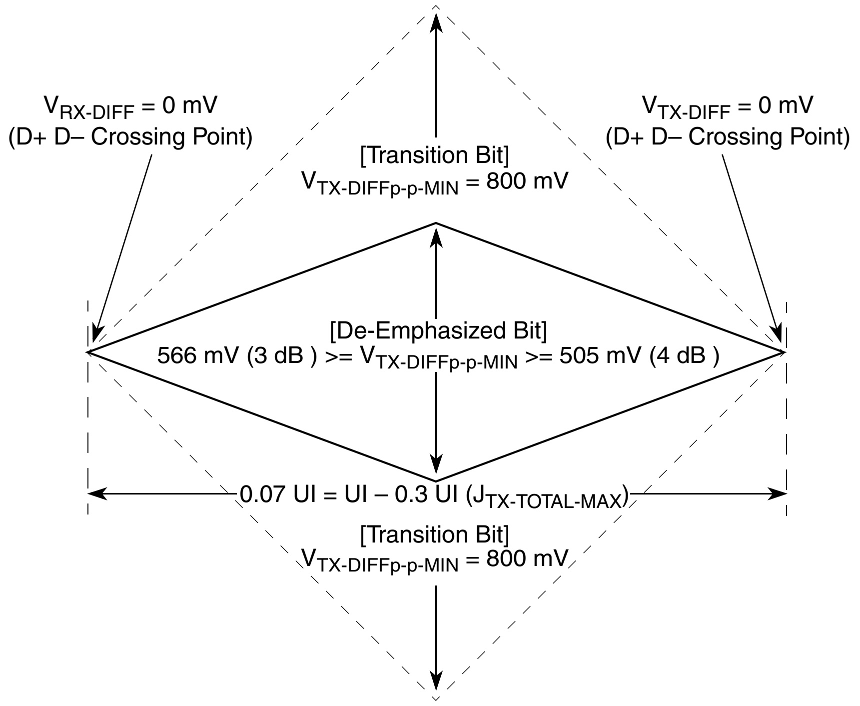

Figure 50. Minimum Transmitter Timing and Voltage Output Compliance Specifications

14.4.3 Differential Receiver (RX) Input Specifications

Table 50 defines the specifications for the differential input at all receivers (RXs). The parameters are specified at the component pins.

Table 50. Differential Receiver (RX) Input Specifications

Symbol	Parameter	Min	Nom	Max	Units	Comments
UI	Unit Interval	399.88	400	400.12	ps	Each UI is 400 ps ± 300 ppm. UI does not account for Spread Spectrum Clock dictated variations. See Note 1.
$V_{\text{RX-DIFFp-p}}$	Differential Peak-to-Peak Output Voltage	0.175	—	—	V	$V_{\text{RX-DIFFp-p}} = 2^{*}\lvert V_{\text{RX-D+}} - V_{\text{RX-D-}}\rvert$ See Note 2.
$T_{\text{RX-EYE}}$	Minimum Receiver Eye Width	0.4	—	—	UI	The maximum interconnect media and Transmitter jitter that can be tolerated by the Receiver can be derived as $T_{\text{RX-MAX-JITTER}} = 1 - T_{\text{RX-EYE}} = 0.6$ UI. See Notes 2 and 3.
$T_{\text{RX-EYE-MEDIAN-to-MAX-JITTER}}$	Maximum time between the jitter median and maximum deviation from the median.	—	—	0.3	UI	Jitter is defined as the measurement variation of the crossing points ($V_{\text{RX-DIFFp-p}} = 0$ V) in relation to a recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI. See Notes 2, 3 and 7.
$V_{\text{RX-CM-ACp}}$	AC Peak Common Mode Input Voltage	—	—	150	mV	$V_{\text{RX-CM-ACp}} = \lvert V_{\text{RXD+}} - V_{\text{RXD-}}\rvert/2 - V_{\text{RX-CM-DC}}$ $V_{\text{RX-CM-DC}} = DC_{(avg)}$ of $\lvert V_{\text{RX-D+}} - V_{\text{RX-D-}}\rvert/2$ See Note 2
$RL_{\text{RX-DIFF}}$	Differential Return Loss	15	—	—	dB	Measured over 50 MHz to 1.25 GHz with the D+ and D– lines biased at +300 mV and –300 mV, respectively. See Note 4
$RL_{\text{RX-CM}}$	Common Mode Return Loss	6	—	—	dB	Measured over 50 MHz to 1.25 GHz with the D+ and D– lines biased at 0 V. See Note 4
$Z_{\text{RX-DIFF-DC}}$	DC Differential Input Impedance	80	100	120	Ω	RX DC Differential mode impedance. See Note 5
$Z_{\text{RX-DC}}$	DC Input Impedance	40	50	60	Ω	Required RX D+ as well as D– DC Impedance (50 ± 20% tolerance). See Notes 2 and 5.
$Z_{\text{RX-HIGH-IMP-DC}}$	Powered Down DC Input Impedance	200 k	—	—	Ω	Required RX D+ as well as D– DC Impedance when the Receiver terminations do not have power. See Note 6.
$V_{\text{RX-IDLE-DET-DIFFp-p}}$	Electrical Idle Detect Threshold	65	—	—	mV	$V_{\text{RX-IDLE-DET-DIFFp-p}} = 2^{*}\lvert V_{\text{RX-D+}} - V_{\text{RX-D-}}\rvert$ Measured at the package pins of the Receiver

provide additional margin to adequately compensate for the degraded minimum Receiver eye diagram (shown in Figure 51) expected at the input Receiver based on some adequate combination of system simulations and the Return Loss measured looking into the RX package and silicon. The RX eye diagram must be aligned in time using the jitter median to locate the center of the eye diagram.

The eye diagram must be valid for any 250 consecutive UIs.

A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.

NOTE

The reference impedance for return loss measurements is 50Ω to ground for both the D+ and D- line (that is, as measured by a Vector Network Analyzer with 50Ω probes—see Figure 52). Note that the series capacitors, C_{TX}, are optional for the return loss measurement.

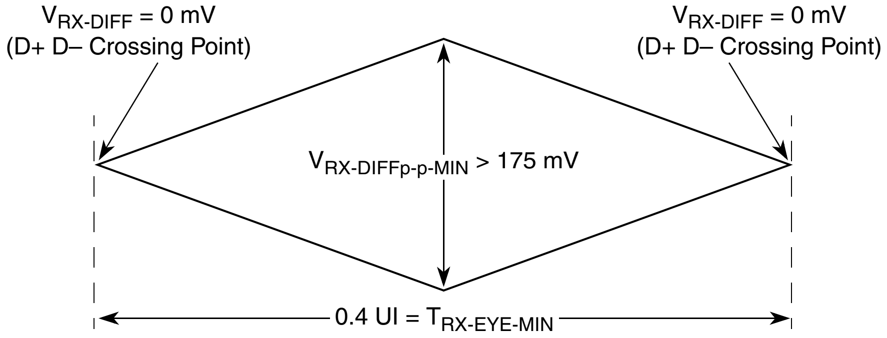

Figure 51. Minimum Receiver Eye Timing and Voltage Compliance Specification

14.5.1 Compliance Test and Measurement Load

The AC timing and voltage parameters must be verified at the measurement point, as specified within 0.2 inches of the package pins, into a test/measurement load shown in Figure 52.

NOTE

The allowance of the measurement point to be within 0.2 inches of the package pins is meant to acknowledge that package/board routing may benefit from D+ and D– not being exactly matched in length at the package pin boundary.

17 Signal Listings

Table 63 provides the pin assignments for the signals. Notes for the signal changes on the single core device (MPC8641) are italicized and prefixed by *“S”*.

Table 63. MPC8641 Signal Reference by Functional Block

Name[1]	Package Pin Number	Pin Type	Power Supply	Notes
DDR Memory Interface 1 Signals[2,3]				
D1_MDQ[0:63]	D15, A14, B12, D12, A15, B15, B13, C13, C11, D11, D9, A8, A12, A11, A9, B9, F11, G12, K11, K12, E10, E9, J11, J10, G8, H10, L9, L7, F10, G9, K9, K8, AC6, AC7, AG8, AH9, AB6, AB8, AE9, AF9, AL8, AM8, AM10, AK11, AH8, AK8, AJ10, AK10, AL12, AJ12, AL14, AM14, AL11, AM11, AM13, AK14, AM15, AJ16, AK18, AL18, AJ15, AL15, AL17, AM17	I/O	D1_GV$_{DD}$	—
D1_MECC[0:7]	M8, M7, R8, T10, L11, L10, P9, R10	I/O	D1_GV$_{DD}$	—
D1_MDM[0:8]	C14, A10, G11, H9, AD7, AJ9, AM12, AK16, N10	O	D1_GV$_{DD}$	—
D1_MDQS[0:8]	A13, C10, H12, J7, AE8, AM9, AK13, AK17, N9	I/O	D1_GV$_{DD}$	—
$\overline{\text{D1\_MDQS}}$[0:8]	D14, B10, H13, J8, AD8, AL9, AJ13, AM16, P10	I/O	D1_GV$_{DD}$	—
D1_MBA[0:2]	AA8, AA10, T9	O	D1_GV$_{DD}$	—
D1_MA[0:15]	Y10, W8, W9, V7, V8, U6, V10, U9, U7, U10, Y9, T6, T8, AE12, R7, P6	O	D1_GV$_{DD}$	—
$\overline{\text{D1\_MWE}}$	AB11	O	D1_GV$_{DD}$	—
$\overline{\text{D1\_MRAS}}$	AB12	O	D1_GV$_{DD}$	—
$\overline{\text{D1\_MCAS}}$	AC10	O	D1_GV$_{DD}$	—
$\overline{\text{D1\_MCS}}$[0:3]	AB9, AD10, AC12, AD11	O	D1_GV$_{DD}$	—
D1_MCKE[0:3]	P7, M10, N8, M11	O	D1_GV$_{DD}$	23
D1_MCK[0:5]	W6, E13, AH11, Y7, F14, AG10	O	D1_GV$_{DD}$	—
$\overline{\text{D1\_MCK}}$[0:5]	Y6, E12, AH12, AA7, F13, AG11	O	D1_GV$_{DD}$	—
D1_MODT[0:3]	AC9, AF12, AE11, AF10	O	D1_GV$_{DD}$	—
D1_MDIC[0:1]	E15, G14	IO	D1_GV$_{DD}$	27
D1_MV$_{REF}$	AM18	DDR Port 1 reference voltage	D1_GV$_{DD}$ /2	3
DDR Memory Interface 2 Signals[2,3]				

Table 63. MPC8641 Signal Reference by Functional Block (continued)

Name[1]	Package Pin Number	Pin Type	Power Supply	Notes
D1_MDVAL/LB_DVAL	J16	O	OV_{DD}	10
D2_MDVAL	D19	O	OV_{DD}	—
Power Management Signals[5]				
ASLEEP	C19	O	OV_{DD}	—
System Clocking Signals[5]				
SYSCLK	G16	I	OV_{DD}	—
RTC	K17	I	OV_{DD}	32
CLK_OUT	B16	O	OV_{DD}	23
Test Signals[5]				
$\overline{\text{LSSD\_MODE}}$	C18	I	OV_{DD}	26
TEST_MODE[0:3]	C16, E17, D18, D16	I	OV_{DD}	26
JTAG Signals[5]				
TCK	H18	I	OV_{DD}	—
TDI	J18	I	OV_{DD}	24
TDO	G18	O	OV_{DD}	23
TMS	F18	I	OV_{DD}	24
$\overline{\text{TRST}}$	A17	I	OV_{DD}	24
Miscellaneous[5]				
Spare	J17	—	—	13
GPOUT[0:7]/ TSEC1_TXD[0:7]	AF25, AC23, AG24, AG23, AE24, AE23, AE22, AD22	O	OV_{DD}	6, 10
GPIN[0:7]/ TSEC1_RXD[0:7]	AL25, AL24, AK26, AK25, AM26, AF26, AH24, AG25	I	OV_{DD}	10
GPOUT[8:15]/ TSEC2_TXD[0:7]	AB20, AJ23, AJ22, AD19, AH23, AH21, AG22, AG21	O	OV_{DD}	10
GPIN[8:15]/ TSEC2_RXD[0:7]	AL22, AK22, AM21, AH20, AG20, AF20, AF23, AF22	I	OV_{DD}	10
Additional Analog Signals				
TEMP_ANODE	AA11	Thermal	—	—
TEMP_CATHODE	Y11	Thermal	—	—
Sense, Power and GND Signals				
$SENSEV_{DD}$_Core0	M14	V_{DD}_Core0 sensing pin	—	31
$SENSEV_{DD}$_Core1	U20	V_{DD}_Core1 sensing pin	—	12,31, *S1*

Table 63. MPC8641 Signal Reference by Functional Block (continued)

Name[1]	Package Pin Number	Pin Type	Power Supply	Notes
SENSEV$_{SS}$_Core0	P14	Core0 GND sensing pin	—	31
SENSEV$_{SS}$_Core1	V20	Core1 GND sensing pin	—	12, 31, *S3*
SENSEV$_{DD}$_PLAT	N18	V$_{DD}$_PLAT sensing pin	—	28
SENSEV$_{SS}$_PLAT	P18	Platform GND sensing pin	—	29
D1_GV$_{DD}$	B11, B14, D10, D13, F9, F12, H8, H11, H14, K10, K13, L8, P8, R6, U8, V6, W10, Y8, AA6, AB10, AC8, AD12, AE10, AF8, AG12, AH10, AJ8, AJ14, AK12, AL10, AL16	SDRAM 1 I/O supply	D1_GV$_{DD}$ 2.5 - DDR 1.8 DDR2	—
D2_GV$_{DD}$	B2, B5, B8, D4, D7, E2, F6, G4, H2, J6, K4, L2, M6, N4, P2, T4, U2, W4, Y2, AB4, AC2, AD6, AE4, AF2, AG6, AH4, AJ2, AK6, AL4, AM2	SDRAM 2 I/O supply	D2_GV$_{DD}$ 2.5 V - DDR 1.8 V - DDR2	—
OV$_{DD}$	B22, B25, B28, D17, D24, D27, F19, F22, F26, F29, G17, H21, H24, K19, K23, M21, AM30	DUART, Local Bus, DMA, Multiprocessor Interrupts, System Control & Clocking, Debug, Test, JTAG, Power management, I^{2}C, JTAG and Miscellaneous I/O voltage	OV$_{DD}$ 3.3 V	—
LV$_{DD}$	AC20, AD23, AH22	TSEC1 and TSEC2 I/O voltage	LV$_{DD}$ 2.5/3.3 V	—
TV$_{DD}$	AC17, AG18, AK20	TSEC3 and TSEC4 I/O voltage	TV$_{DD}$ 2.5/3.3 V	—
SV$_{DD}$	H31, J29, K28, K32, L30, M28, M31, N29, R30, T31, U29, V32, W30, Y31, AA29, AB32, AC30, AD31, AE29, AG30, AH31, AJ29, AK32, AL30, AM31	Transceiver Power Supply SerDes	SV$_{DD}$ 1.05/1.1 V	—
XV$_{DD}$_SRDS1	K26, L24, M27, N25, P26, R24, R28, T27, U25, V26	Serial I/O Power Supply for SerDes Port 1	XV$_{DD}$_SRDS1 1.05/1.1 V	—

The Bergquist Company 800-347-4572
18930 West 78th St.
Chanhassen, MN 55317
Internet: www.bergquistcompany.com

Chomerics, Inc. 781-935-4850
77 Dragon Ct.
Woburn, MA 01801
Internet: www.chomerics.com

Dow-Corning Corporation 800-248-2481
Corporate Center
PO Box 994
Midland, MI 48686-0994
Internet: www.dowcorning.com

Shin-Etsu MicroSi, Inc. 888-642-7674
10028 S. 51st St.
Phoenix, AZ 85044
Internet: www.microsi.com

Thermagon Inc. 888-246-9050
4707 Detroit Ave.
Cleveland, OH 44102
Internet: www.thermagon.com

The following section provides a heat sink selection example using one of the commercially available heat sinks.

19.2.3 Heat Sink Selection Example

For preliminary heat sink sizing, the die-junction temperature can be expressed as follows:

$$T_j = T_i + T_r + (R_{\theta JC} + R_{\theta int} + R_{\theta sa}) \times P_d$$

where:

T_j is the die-junction temperature
T_i is the inlet cabinet ambient temperature
T_r is the air temperature rise within the computer cabinet
$R_{\theta JC}$ is the junction-to-case thermal resistance
$R_{\theta int}$ is the adhesive or interface material thermal resistance
$R_{\theta sa}$ is the heat sink base-to-ambient thermal resistance
P_d is the power dissipated by the device

During operation, the die-junction temperatures (T_j) should be maintained less than the value specified in Table 2. The temperature of air cooling the component greatly depends on the ambient inlet air temperature and the air temperature rise within the electronic cabinet. An electronic cabinet inlet-air temperature (T_i) may range from 30° to 40°C. The air temperature rise within a cabinet (T_r) may be in the range of 5° to 10°C. The thermal resistance of the thermal interface material ($R_{\theta int}$) is typically about 0.2°C/W. For

Another useful equation is:

$$V_H - V_L = n\frac{KT}{q}\left[ln\frac{I_H}{I_L}\right]$$

Where:

I_{fw} = Forward current
I_s = Saturation current
V_d = Voltage at diode
V_f = Voltage forward biased
V_H = Diode voltage while I_H is flowing
V_L = Diode voltage while I_L is flowing
I_H = Larger diode bias current
I_L = Smaller diode bias current
q = Charge of electron (1.6×10^{-19} C)
n = Ideality factor (normally 1.0)
K = Boltzman’s constant (1.38×10^{-23} Joules/K)
T = Temperature (Kelvins)

The ratio of I_H to I_L is usually selected to be 10:1. The above simplifies to the following:

$$V_H - V_L = 1.986 \times 10^{-4} \times nT$$

Solving for T, the equation becomes:

$$nT = \frac{V_H - V_L}{1.986 \times 10^{-4}}$$