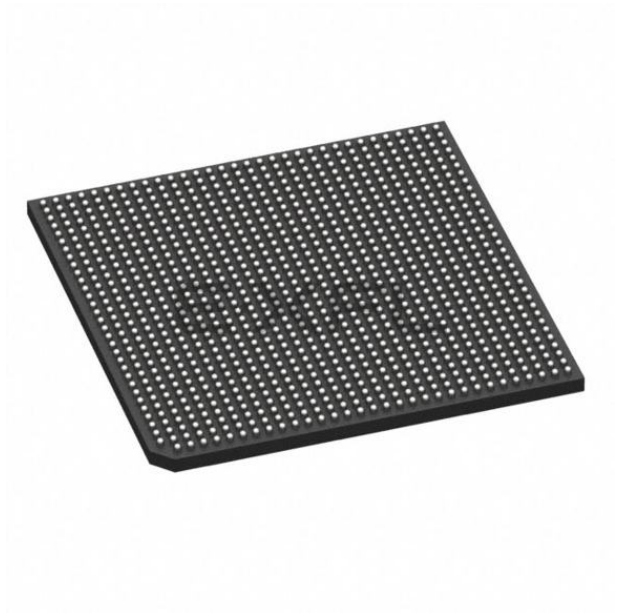

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e600
Number of Cores/Bus Width	2 Core, 32-Bit
Speed	1.333GHz
Co-Processors/DSP	-
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (4)
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	-
Package / Case	1023-BCBGA, FCCBGA
Supplier Device Package	1023-FCCBGA (33x33)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc8641dtvj1333je

2 Electrical Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC8641. The MPC8641 is currently targeted to these specifications.

2.1 Overall DC Electrical Characteristics

This section covers the ratings, conditions, and other characteristics.

2.1.1 Absolute Maximum Ratings

Table 1 provides the absolute maximum ratings.

Table 1. Absolute Maximum Ratings[1]

Characteristic	Symbol	Absolute Maximum Value	Unit	Notes
Cores supply voltages	V_{DD}_Core0, V_{DD}_Core1	–0.3 to 1.21 V	V	2
Cores PLL supply	AV_{DD}_Core0, AV_{DD}_Core1	–0.3 to 1.21 V	V	—
SerDes Transceiver Supply (Ports 1 and 2)	SV_{DD}	–0.3 to 1.21 V	V	—
SerDes Serial I/O Supply Port 1	XV_{DD}_SRDS1	–0.3 to 1.21V	V	—
SerDes Serial I/O Supply Port 2	XV_{DD}_SRDS2	–0.3 to 1.21 V	V	—
SerDes DLL and PLL supply voltage for Port 1 and Port 2	AV_{DD}_SRDS1, AV_{DD}_SRDS2	–0.3 to 1.21V	V	—
Platform Supply voltage	V_{DD}_PLAT	–0.3 to 1.21V	V	—
Local Bus and Platform PLL supply voltage	AV_{DD}_LB, AV_{DD}_PLAT	–0.3 to 1.21V	V	—
DDR and DDR2 SDRAM I/O supply voltages	D1_GV_{DD}, D2_GV_{DD}	–0.3 to 2.75 V	V	3
		–0.3 to 1.98 V	V	3
eTSEC 1 and 2 I/O supply voltage	LV_{DD}	–0.3 to 3.63 V	V	4
		–0.3 to 2.75 V	V	4
eTSEC 3 and 4 I/O supply voltage	TV_{DD}	–0.3 to 3.63 V	V	4
		–0.3 to 2.75 V	V	4
Local Bus, DUART, DMA, Multiprocessor Interrupts, System Control & Clocking, Debug, Test, Power management, I^2C, JTAG and Miscellaneous I/O voltage	OV_{DD}	–0.3 to 3.63 V	V	—

2.1.3 Output Driver Characteristics

Table 3 provides information on the characteristics of the output driver strengths. The values are preliminary estimates.

Table 3. Output Drive Capability

Driver Type	Programmable Output Impedance (Ω)	Supply Voltage	Notes
DDR1 signal	18 36 (half strength mode)	D*n*_GV_{DD} = 2.5 V	4, 9
DDR2 signal	18 36 (half strength mode)	D*n*_GV_{DD} = 1.8 V	1, 5, 9
Local Bus signals	45 25	OV_{DD} = 3.3 V	2, 6
eTSEC/10/100 signals	45	T/LV_{DD} = 3.3 V	6
	30	T/LV_{DD} = 2.5 V	6
DUART, DMA, Multiprocessor Interrupts, System Control & Clocking, Debug, Test, Power management, JTAG and Miscellaneous I/O voltage	45	OV_{DD} = 3.3 V	6
I^2C	150	OV_{DD} = 3.3 V	7
SRIO, PCI Express	100	SV_{DD} = 1.1/1.05 V	3, 8

Notes:
1. See the DDR Control Driver registers in the MPC8641D reference manual for more information.
2. Only the following local bus signals have programmable drive strengths: LALE, LAD[0:31], LDP[0:3], LA[27:31], LCKE, LCS[1:2], LWE[0:3], LGPL1, LGPL2, LGPL3, LGPL4, LGPL5, LCLK[0:2]. The other local bus signals have a fixed drive strength of 45 Ω. See the POR Impedance Control register in the MPC8641D reference manual for more information about local bus signals and their drive strength programmability.
3. See Section 17, "Signal Listings," for details on resistor requirements for the calibration of SD*n*_IMP_CAL_TX and SD*n*_IMP_CAL_RX transmit and receive signals.
4. Stub Series Terminated Logic (SSTL-25) type pins.
5. Stub Series Terminated Logic (SSTL-18) type pins.
6. Low Voltage Transistor-Transistor Logic (LVTTL) type pins.
7. Open Drain type pins.
8. Low Voltage Differential Signaling (LVDS) type pins.
9. The drive strength of the DDR interface in half strength mode is at T_j = 105C and at D*n*_GV_{DD} (min).

2.2 Power Up/Down Sequence

The MPC8641 requires its power rails to be applied in a specific sequence in order to ensure proper device operation.

NOTE

The recommended maximum ramp up time for power supplies is 20 milliseconds.

The chronological order of power up is as follows:

1. All power rails other than DDR I/O (D*n*_GV_{DD}, and D*n*_MV_{REF}).

NOTE

There is no required order sequence between the individual rails for this item (# 1). However, V_{DD}_PLAT, AV_{DD}_PLAT rails must reach 90% of their recommended value before the rail for Dn_GV_{DD}, and Dn_MV_{REF} (in next step) reaches 10% of their recommended value. AV_{DD} type supplies must be delayed with respect to their source supplies by the RC time constant of the PLL filter circuit described in Section 20.2.1, "PLL Power Supply Filtering."

2. D*n*_GV_{DD}, D*n*_MV_{REF}

NOTE

It is possible to leave the related power supply (D*n*_GV_{DD}, D*n*_MV_{REF}) turned off at reset for a DDR port that will not be used. Note that these power supplies can only be powered up again at reset for functionality to occur on the DDR port.

3. SYSCLK

The recommended order of power down is as follows:

1. D*n*_GV_{DD}, D*n*_MV_{REF}
2. All power rails other than DDR I/O (D*n*_GV_{DD}, D*n*_MV_{REF}).

NOTE

SYSCLK may be powered down simultaneous to either of item # 1 or # 2 in the power down sequence. Beyond this, the power supplies may power down simultaneously if the preservation of DDR*n* memory is not a concern.

See Figure 3 for more details on the Power and Reset Sequencing details.

The maximum power dissipation for individual power supplies of the MPC8641D is shown in Table 5.

Table 5. MPC8641D Individual Supply Maximum Power Dissipation [1]

Component Description	Supply Voltage (Volts)	Power (Watts)	Notes
Per Core voltage Supply	V_{DD}_Core0/V_{DD}_Core1 = 1.1 V @ 1500 MHz	21.00	
Per Core PLL voltage supply	AV_{DD}_Core0/AV_{DD}_Core1 = 1.1 V @ 1500 MHz	0.0125	
Per Core voltage Supply	V_{DD}_Core0/V_{DD}_Core1 = 1.05 V @ 1333 MHz	17.00	
Per Core PLL voltage supply	AV_{DD}_Core0/AV_{DD}_Core1 = 1.05 V @ 1333 MHz	0.0125	
Per Core voltage Supply	V_{DD}_Core0/V_{DD}_Core1 = 0.95 V @ 1000 MHz	11.50	5
Per Core PLL voltage supply	AV_{DD}_Core0/AV_{DD}_Core1 = 0.95 V @ 1000 MHz	0.0125	5
DDR Controller I/O voltage supply	D*n*_GV_{DD} = 2.5 V @ 400 MHz	0.80	2
	D*n*_GV_{DD} = 1.8 V @ 533 MHz	0.68	2
	D*n*_GV_{DD} = 1.8 V @ 600 MHz	0.77	2
16-bit FIFO @ 200 MHz eTsec 1&2/3&4 Voltage Supply	L/TV_{DD} = 3.3 V	0.11	2, 3
non-FIFO eTsec*n* Voltage Supply	L/TV_{DD} = 3.3 V	0.08	2
x8 SerDes transceiver Supply	SV_{DD} = 1.1 V	0.70	2
x8 SerDes I/O Supply	XV_{DD}_SRDS*n* = 1.1 V	0.66	2
SerDes PLL voltage supply Port 1 or 2	AV_{DD}_SRDS1/AV_{DD}_SRDS2 = 1.1 V	0.10	
Platform I/O Supply	OV_{DD} = 3.3 V	0.45	4
Platform source Supply	V_{DD}_PLAT = 1.1 V @ 600 MHz	12.00	
Platform source Supply	V_{DD}_PLAT = 1.05 Vn @ 500 MHz	9.80	5
Platform source Supply	V_{DD}_PLAT = 1.05 Vn @ 400 MHz	7.70	
Platform, Local Bus PLL voltage Supply	AV_{DD}_PLAT, AV_{DD}_LB = 1.1 V	0.0125	

Notes:

1. This is a maximum power supply number which is provided for power supply and board design information. The numbers are based on 100% bus utilization for each component. The components listed are not expected to have 100% bus usage simultaneously for all components. Actual numbers may vary based on activity.
2. Number is based on a per port/interface value.
3. This is based on one eTSEC port used. Since 16-bit FIFO mode involves two ports, the number will need to be multiplied by two for the total. The other eTSEC protocols dissipate less than this number per port. Note that the power needs to be multiplied by the number of ports used for the protocol for the total eTSEC port power dissipation.
4. This includes Local Bus, DUART, I^2C, DMA, Multiprocessor Interrupts, System Control & Clocking, Debug, Test, Power management, JTAG and Miscellaneous I/O voltage.
5. These power numbers are for Part Number MC8641xxx1000NX only. V_{DD}_Core*n* = 0.95 V and V_{DD}_PLAT = 1.05 V.

Table 10. EC*n*_GTX_CLK125 AC Timing Specifications (continued)

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
EC*n*_GTX_CLK125 duty cycle GMII, TBI 1000Base-T for RGMII, RTBI	t_{G125H}/t_{G125}	 45 47	—	 55 53	%	1, 2

Notes:
1. Timing is guaranteed by design and characterization.
2. EC*n*_GTX_CLK125 is used to generate the GTX clock for the eTSEC transmitter with 2% degradation. EC*n*_GTX_CLK125 duty cycle can be loosened from 47/53% as long as the PHY device can tolerate the duty cycle generated by the eTSEC GTX_CLK. See Section 8.2.6, "RGMII and RTBI AC Timing Specifications," for duty cycle for 10Base-T and 100Base-T reference clock.
3. ±100 ppm tolerance on EC*n*_GTX_CLK125 frequency

NOTE

The phase between the output clocks TSEC1_GTX_CLK and TSEC2_GTX_CLK (ports 1 and 2) is no more than 100 ps. The phase between the output clocks TSEC3_GTX_CLK and TSEC4_GTX_CLK (ports 3 and 4) is no more than 100 ps.

4.4 Platform Frequency Requirements for PCI-Express and Serial RapidIO

The MPX platform clock frequency must be considered for proper operation of the high-speed PCI Express and Serial RapidIO interfaces as described below.

For proper PCI Express operation, the MPX clock frequency must be greater than or equal to:

$$\frac{527\ \text{MHz} \times (\text{PCI-Express link width})}{16 / (1 + \text{cfg\_plat\_freq})}$$

Note that at MPX = 400 MHz, cfg_plat_freq = 0 and at MPX > 400 MHz, cfg_plat_freq = 1. Therefore, when operating PCI Express in x8 link width, the MPX platform frequency must be 400 MHz with cfg_plat_freq = 0 or greater than or equal to 527 MHz with cfg_plat_freq = 1.

For proper Serial RapidIO operation, the MPX clock frequency must be greater than or equal to:

$$\frac{2 \times (0.8512) \times (\text{Serial RapidIO interface frequency}) \times (\text{Serial RapidIO link width})}{64}$$

4.5 Other Input Clocks

For information on the input clocks of other functional blocks of the platform such as SerDes, and eTSEC, see the specific section of this document.

6 DDR and DDR2 SDRAM

This section describes the DC and AC electrical specifications for the DDR SDRAM interface of the MPC8641. Note that DDR SDRAM is D*n*_GV_{DD}(typ) = 2.5 V and DDR2 SDRAM is D*n*_GV_{DD}(typ) = 1.8 V.

6.1 DDR SDRAM DC Electrical Characteristics

Table 13 provides the recommended operating conditions for the DDR2 SDRAM component(s) of the MPC8641 when D*n*_GV_{DD}(typ) = 1.8 V.

Table 13. DDR2 SDRAM DC Electrical Characteristics for D*n*_GV_{DD}(typ) = 1.8 V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
I/O supply voltage	D*n*_GV_{DD}	1.71	1.89	V	1
I/O reference voltage	D*n*_MV_{REF}	0.49 × D*n*_GV_{DD}	0.51 × D*n*_GV_{DD}	V	2
I/O termination voltage	V_{TT}	D*n*_MV_{REF} – 0.04	D*n*_MV_{REF} + 0.04	V	3
Input high voltage	V_{IH}	D*n*_MV_{REF}+ 0.125	D*n*_GV_{DD} + 0.3	V	—
Input low voltage	V_{IL}	–0.3	D*n*_MV_{REF} – 0.125	V	—
Output leakage current	I_{OZ}	–50	50	μA	4
Output high current (V_{OUT} = 1.420 V)	I_{OH}	–13.4	—	mA	—
Output low current (V_{OUT} = 0.280 V)	I_{OL}	13.4	—	mA	—

Notes:
1. D*n*_GV_{DD} is expected to be within 50 mV of the DRAM D*n*_GV_{DD} at all times.
2. D*n*_MV_{REF} is expected to be equal to 0.5 × D*n*_GV_{DD}, and to track D*n*_GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on D*n*_MV_{REF} may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to D*n*_MV_{REF}. This rail should track variations in the DC level of D*n*_MV_{REF}.
4. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ D*n*_GV_{DD}.

Table 14 provides the DDR2 capacitance when D*n*_GV_{DD}(typ) = 1.8 V.

Table 14. DDR2 SDRAM Capacitance for D*n*_GV_{DD}(typ)=1.8 V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input/output capacitance: DQ, DQS, $\overline{\text{DQS}}$	C_{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS, $\overline{\text{DQS}}$	C_{DIO}	—	0.5	pF	1

Note:
1. This parameter is sampled. D*n*_GV_{DD} = 1.8 V ± 0.090 V, f = 1 MHz, T_A = 25°C, V_{OUT} = D*n*_GV_{DD}/2, V_{OUT} (peak-to-peak) = 0.2 V.

Table 24. GMII, MII, RMII, TBI and FIFO DC Electrical Characteristics (continued)

Parameter	Symbol	Min	Max	Unit	Notes
Input low current (V_{IN} = GND)	I_{IL}	–600	—	μA	3

Notes:

1 LV_{DD} supports eTSECs 1 and 2.
2 TV_{DD} supports eTSECs 3 and 4.
3 The symbol V_{IN}, in this case, represents the LV_{IN} and TV_{IN} symbols referenced in Table 1 and Table 2.

Table 25. GMII, RGMII, RTBI, TBI and FIFO DC Electrical Characteristics

Parameters	Symbol	Min	Max	Unit	Notes
Supply voltage 2.5 V	LV_{DD}/TV_{DD}	2.375	2.625	V	1,2
Output high voltage (LV_{DD}/TV_{DD} = Min, I_{OH} = –1.0 mA)	V_{OH}	2.00	—	V	—
Output low voltage (LV_{DD}/TV_{DD} = Min, I_{OL} = 1.0 mA)	V_{OL}	—	0.40	V	—
Input high voltage	V_{IH}	1.70	—	V	—
Input low voltage	V_{IL}	—	0.90	V	—
Input high current (V_{IN} = LV_{DD}, V_{IN} = TV_{DD})	I_{IH}	—	10	μA	1, 2,3
Input low current (V_{IN} = GND)	I_{IL}	–15	—	μA	3

Note:

1 LV_{DD} supports eTSECs 1 and 2.
2 TV_{DD} supports eTSECs 3 and 4.
3 Note that the symbol V_{IN}, in this case, represents the LV_{IN} and TV_{IN} symbols referenced in Table 1 and Table 2.

8.2 FIFO, GMII, MII, TBI, RGMII, RMII, and RTBI AC Timing Specifications

The AC timing specifications for FIFO, GMII, MII, TBI, RGMII, RMII and RTBI are presented in this section.

8.2.1 FIFO AC Specifications

The basis for the AC specifications for the eTSEC's FIFO modes is the double data rate RGMII and RTBI specifications, since they have similar performance and are described in a source-synchronous fashion like FIFO modes. However, the FIFO interface provides deliberate skew between the transmitted data and source clock in GMII fashion.

When the eTSEC is configured for FIFO modes, all clocks are supplied from external sources to the relevant eTSEC interface. That is, the transmit clock must be applied to the eTSEC*n*'s TSEC*n*_TX_CLK, while the receive clock must be applied to pin TSEC*n*_RX_CLK. The eTSEC internally uses the transmit

Figure 26 to Figure 31 show the local bus signals.

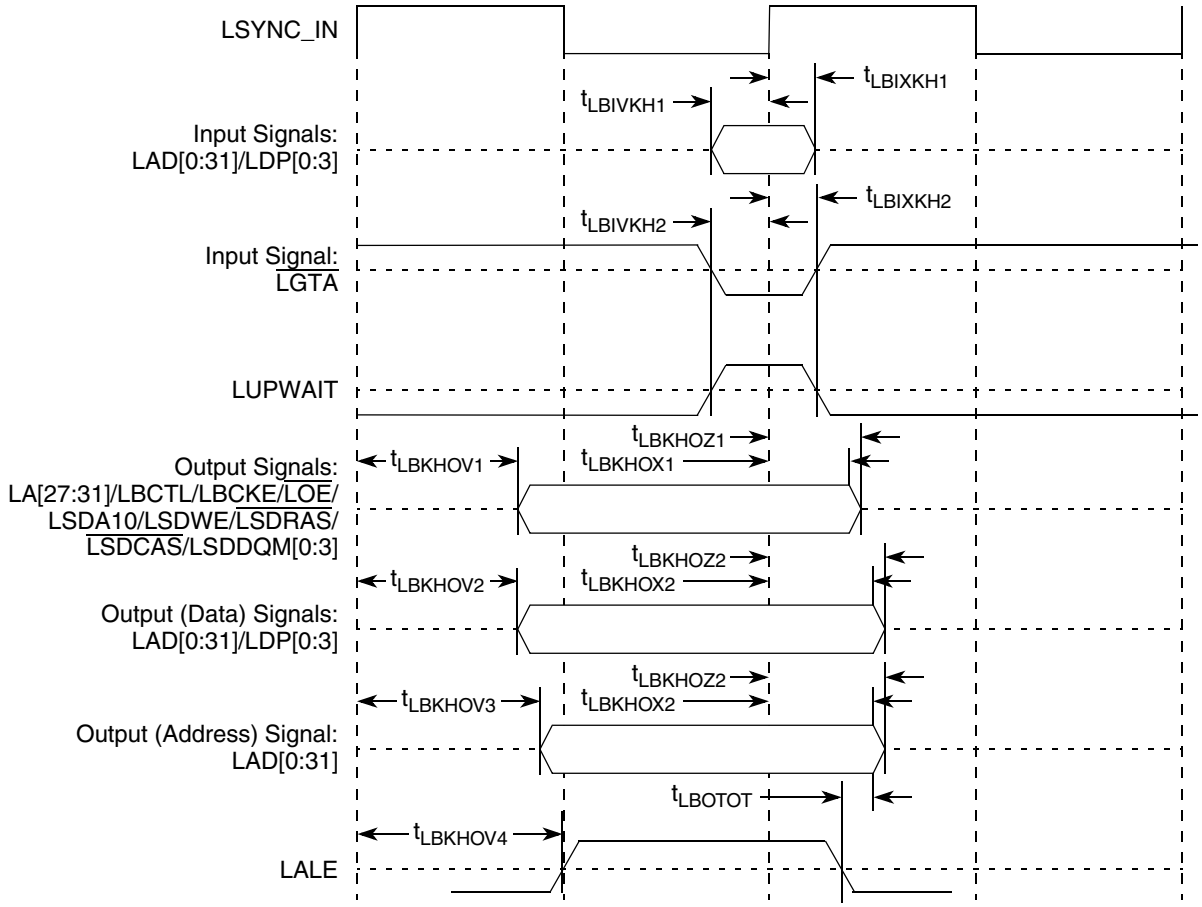


Figure 26. Local Bus Signals (PLL Enabled)

NOTE

PLL bypass mode is recommended when LBIU frequency is at or below 83 MHz. When LBIU operates above 83 MHz, LBIU PLL is recommended to be enabled.

Table 42 describes the general timing parameters of the local bus interface at OV_{DD} = 3.3 V with PLL bypassed.

Table 42. Local Bus Timing Parameters—PLL Bypassed

Parameter	Symbol [1]	Min	Max	Unit	Notes
Local bus cycle time	t_{LBK}	12	—	ns	2
Local bus duty cycle	t_{LBKH}/t_{LBK}	45	55	%	—
Internal launch/capture clock to LCLK delay	t_{LBKHKT}	2.3	3.9	ns	8
Input setup to local bus clock (except $\overline{\text{LGTA}}$/LUPWAIT)	$t_{LBIVKH1}$	5.7	—	ns	4, 5
$\overline{\text{LGTA}}$/LUPWAIT input setup to local bus clock	$t_{LBIVKL2}$	5.6	—	ns	4, 5
Input hold from local bus clock (except $\overline{\text{LGTA}}$/LUPWAIT)	$t_{LBIXKH1}$	–1.8	—	ns	4, 5

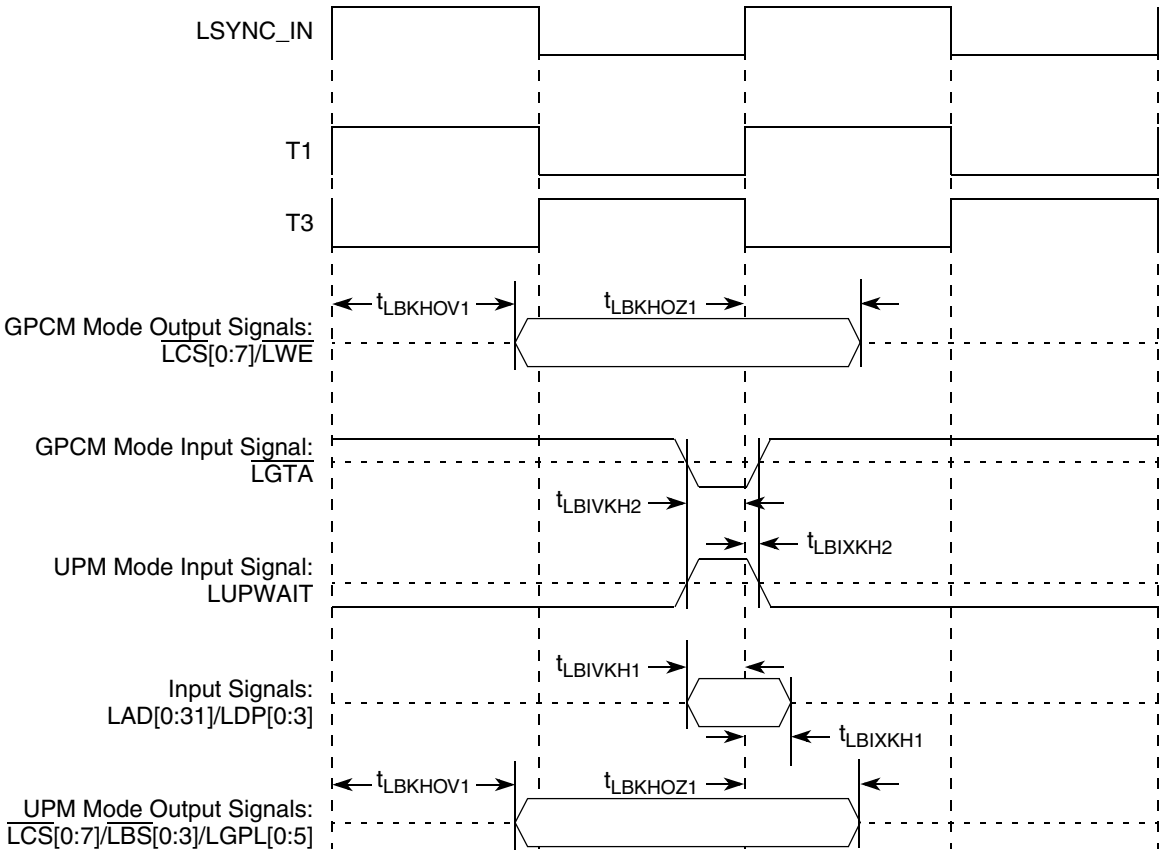


Figure 28. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 2 (clock ratio of 4) (PLL Enabled)

Table 44. JTAG AC Timing Specifications (Independent of SYSCLK) [1] (continued)

At recommended operating conditions (see Table 3).

Parameter	Symbol [2]	Min	Max	Unit	Notes
Output hold times: Boundary-scan data TDO	 t_{JTKLDX} t_{JTKLOX}	 30 30	 — —	ns	5, 6
JTAG external clock to output high impedance: Boundary-scan data TDO	 t_{JTKLDZ} t_{JTKLOZ}	 3 3	 19 9	ns	5, 6

Notes:

1. All outputs are measured from the midpoint voltage of the falling/rising edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 32). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
3. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
4. Non-JTAG signal input timing with respect to t_{TCLK}.
5. Non-JTAG signal output timing with respect to t_{TCLK}.
6. Guaranteed by design.

Figure 32 provides the AC test load for TDO and the boundary-scan outputs.

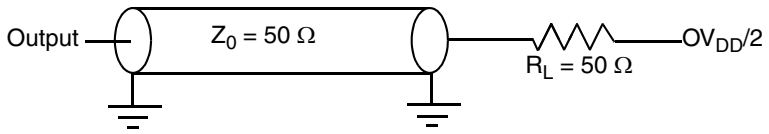


Figure 32. AC Test Load for the JTAG Interface

Figure 33 provides the JTAG clock input timing diagram.

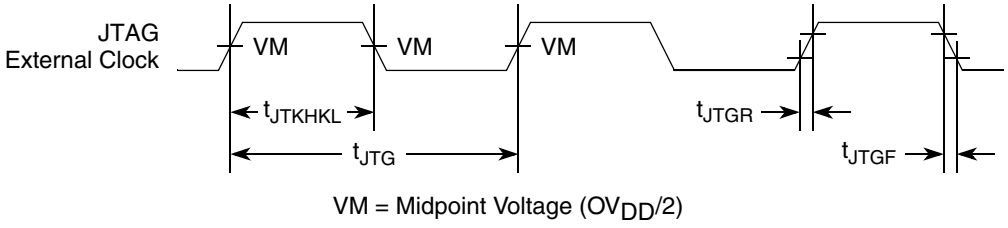


Figure 33. JTAG Clock Input Timing Diagram

Table 49. Differential Transmitter (TX) Output Specifications (continued)

Symbol	Parameter	Min	Nom	Max	Units	Comments
T_{TX-EYE}	Minimum TX Eye Width	0.70	—	—	UI	The maximum Transmitter jitter can be derived as $T_{TX-MAX-JITTER}$ = 1 – T_{TX-EYE}= 0.3 UI. See Notes 2 and 3.
$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time between the jitter median and maximum deviation from the median.	—	—	0.15	UI	Jitter is defined as the measurement variation of the crossing points ($V_{TX-DIFFp-p}$ = 0 V) in relation to a recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI. See Notes 2 and 3.
$T_{TX-RISE}$, $T_{TX-FALL}$	D+/D– TX Output Rise/Fall Time	0.125	—	—	UI	See Notes 2 and 5
$V_{TX-CM-ACp}$	RMS AC Peak Common Mode Output Voltage	—	—	20	mV	$V_{TX-CM-ACp}$ = RMS(|V_{TXD+} + V_{TXD-}|/2 – $V_{TX-CM-DC}$) $V_{TX-CM-DC}$ = $DC_{(avg)}$ of |V_{TX-D+} + V_{TX-D-}|/2 See Note 2
$V_{TX-CM-DC-ACTIVE-IDLE-DELTA}$	Absolute Delta of DC Common Mode Voltage During L0 and Electrical Idle	0	—	100	mV	|$V_{TX-CM-DC\ (during\ L0)}$ – $V_{TX-CM-Idle-DC\ (During\ Electrical\ Idle)}$|<=100 mV $V_{TX-CM-DC}$ = $DC_{(avg)}$ of |V_{TX-D+} + V_{TX-D-}|/2 [L0] $V_{TX-CM-Idle-DC}$ = $DC_{(avg)}$ of |V_{TX-D+} + V_{TX-D-}|/2 [Electrical Idle] See Note 2.
$V_{TX-CM-DC-LINE-DELTA}$	Absolute Delta of DC Common Mode between D+ and D–	0	—	25	mV	|$V_{TX-CM-DC-D+}$ – $V_{TX-CM-DC-D-}$| <= 25 mV $V_{TX-CM-DC-D+}$ = $DC_{(avg)}$ of |V_{TX-D+}| $V_{TX-CM-DC-D-}$ = $DC_{(avg)}$ of |V_{TX-D-}| See Note 2.
$V_{TX-IDLE-DIFFp}$	Electrical Idle differential Peak Output Voltage	0	—	20	mV	$V_{TX-IDLE-DIFFp}$ = |$V_{TX-IDLE-D+}$ –$V_{TX-IDLE-D-}$| <= 20 mV See Note 2.
$V_{TX-RCV-DETECT}$	The amount of voltage change allowed during Receiver Detection	—	—	600	mV	The total amount of voltage change that a transmitter can apply to sense whether a low impedance Receiver is present. See Note 6.
$V_{TX-DC-CM}$	The TX DC Common Mode Voltage	0	—	3.6	V	The allowed DC Common Mode voltage under any conditions. See Note 6.
$I_{TX-SHORT}$	TX Short Circuit Current Limit	—	—	90	mA	The total current the Transmitter can provide when shorted to its ground
$T_{TX-IDLE-MIN}$	Minimum time spent in Electrical Idle	50	—	—	UI	Minimum time a Transmitter must be in Electrical Idle Utilized by the Receiver to start looking for an Electrical Idle Exit after successfully receiving an Electrical Idle ordered set

14.4.3 Differential Receiver (RX) Input Specifications

Table 50 defines the specifications for the differential input at all receivers (RXs). The parameters are specified at the component pins.

Table 50. Differential Receiver (RX) Input Specifications

Symbol	Parameter	Min	Nom	Max	Units	Comments
UI	Unit Interval	399.88	400	400.12	ps	Each UI is 400 ps ± 300 ppm. UI does not account for Spread Spectrum Clock dictated variations. See Note 1.
$V_{RX-DIFFp-p}$	Differential Peak-to-Peak Output Voltage	0.175	—	—	V	$V_{RX-DIFFp-p} = 2*\|V_{RX-D+} - V_{RX-D-}\|$ See Note 2.
T_{RX-EYE}	Minimum Receiver Eye Width	0.4	—	—	UI	The maximum interconnect media and Transmitter jitter that can be tolerated by the Receiver can be derived as $T_{RX-MAX-JITTER} = 1 - T_{RX-EYE} = 0.6$ UI. See Notes 2 and 3.
$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time between the jitter median and maximum deviation from the median.	—	—	0.3	UI	Jitter is defined as the measurement variation of the crossing points ($V_{RX-DIFFp-p}$ = 0 V) in relation to a recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI. See Notes 2, 3 and 7.
$V_{RX-CM-ACp}$	AC Peak Common Mode Input Voltage	—	—	150	mV	$V_{RX-CM-ACp} = \|V_{RXD+} - V_{RXD-}\|/2 - V_{RX-CM-DC}$ $V_{RX-CM-DC} = DC_{(avg)}$ of $\|V_{RX-D+} - V_{RX-D-}\|/2$ See Note 2
$RL_{RX-DIFF}$	Differential Return Loss	15	—	—	dB	Measured over 50 MHz to 1.25 GHz with the D+ and D– lines biased at +300 mV and –300 mV, respectively. See Note 4
RL_{RX-CM}	Common Mode Return Loss	6	—	—	dB	Measured over 50 MHz to 1.25 GHz with the D+ and D– lines biased at 0 V. See Note 4
$Z_{RX-DIFF-DC}$	DC Differential Input Impedance	80	100	120	Ω	RX DC Differential mode impedance. See Note 5
Z_{RX-DC}	DC Input Impedance	40	50	60	Ω	Required RX D+ as well as D– DC Impedance (50 ± 20% tolerance). See Notes 2 and 5.
$Z_{RX-HIGH-IMP-DC}$	Powered Down DC Input Impedance	200 k	—	—	Ω	Required RX D+ as well as D– DC Impedance when the Receiver terminations do not have power. See Note 6.
$V_{RX-IDLE-DET-DIFFp-p}$	Electrical Idle Detect Threshold	65	—	—	mV	$V_{RX-IDLE-DET-DIFFp-p} = 2*\|V_{RX-D+} - V_{RX-D-}\|$ Measured at the package pins of the Receiver

Table 63. MPC8641 Signal Reference by Functional Block (continued)

Name[1]	Package Pin Number	Pin Type	Power Supply	Notes
D1_MDVAL/LB_DVAL	J16	O	OV_{DD}	10
D2_MDVAL	D19	O	OV_{DD}	—
Power Management Signals[5]				
ASLEEP	C19	O	OV_{DD}	—
System Clocking Signals[5]				
SYSCLK	G16	I	OV_{DD}	—
RTC	K17	I	OV_{DD}	32
CLK_OUT	B16	O	OV_{DD}	23
Test Signals[5]				
$\overline{\text{LSSD\_MODE}}$	C18	I	OV_{DD}	26
TEST_MODE[0:3]	C16, E17, D18, D16	I	OV_{DD}	26
JTAG Signals[5]				
TCK	H18	I	OV_{DD}	—
TDI	J18	I	OV_{DD}	24
TDO	G18	O	OV_{DD}	23
TMS	F18	I	OV_{DD}	24
$\overline{\text{TRST}}$	A17	I	OV_{DD}	24
Miscellaneous[5]				
Spare	J17	—	—	13
GPOUT[0:7]/ TSEC1_TXD[0:7]	AF25, AC23, AG24, AG23, AE24, AE23, AE22, AD22	O	OV_{DD}	6, 10
GPIN[0:7]/ TSEC1_RXD[0:7]	AL25, AL24, AK26, AK25, AM26, AF26, AH24, AG25	I	OV_{DD}	10
GPOUT[8:15]/ TSEC2_TXD[0:7]	AB20, AJ23, AJ22, AD19, AH23, AH21, AG22, AG21	O	OV_{DD}	10
GPIN[8:15]/ TSEC2_RXD[0:7]	AL22, AK22, AM21, AH20, AG20, AF20, AF23, AF22	I	OV_{DD}	10
Additional Analog Signals				
TEMP_ANODE	AA11	Thermal	—	—
TEMP_CATHODE	Y11	Thermal	—	—
Sense, Power and GND Signals				
$SENSEV_{DD}$_Core0	M14	V_{DD}_Core0 sensing pin	—	31
$SENSEV_{DD}$_Core1	U20	V_{DD}_Core1 sensing pin	—	12,31, *S1*

Table 63. MPC8641 Signal Reference by Functional Block (continued)

Name[1]	Package Pin Number	Pin Type	Power Supply	Notes
$SENSEV_{SS}$_Core0	P14	Core0 GND sensing pin	—	31
$SENSEV_{SS}$_Core1	V20	Core1 GND sensing pin	—	12, 31, *S3*
$SENSEV_{DD}$_PLAT	N18	V_{DD}_PLAT sensing pin	—	28
$SENSEV_{SS}$_PLAT	P18	Platform GND sensing pin	—	29
$D1\_GV_{DD}$	B11, B14, D10, D13, F9, F12, H8, H11, H14, K10, K13, L8, P8, R6, U8, V6, W10, Y8, AA6, AB10, AC8, AD12, AE10, AF8, AG12, AH10, AJ8, AJ14, AK12, AL10, AL16	SDRAM 1 I/O supply	$D1\_GV_{DD}$ 2.5 - DDR 1.8 DDR2	—
$D2\_GV_{DD}$	B2, B5, B8, D4, D7, E2, F6, G4, H2, J6, K4, L2, M6, N4, P2, T4, U2, W4, Y2, AB4, AC2, AD6, AE4, AF2, AG6, AH4, AJ2, AK6, AL4, AM2	SDRAM 2 I/O supply	$D2\_GV_{DD}$ 2.5 V - DDR 1.8 V - DDR2	—
OV_{DD}	B22, B25, B28, D17, D24, D27, F19, F22, F26, F29, G17, H21, H24, K19, K23, M21, AM30	DUART, Local Bus, DMA, Multiprocessor Interrupts, System Control & Clocking, Debug, Test, JTAG, Power management, I^2C, JTAG and Miscellaneous I/O voltage	OV_{DD} 3.3 V	—
LV_{DD}	AC20, AD23, AH22	TSEC1 and TSEC2 I/O voltage	LV_{DD} 2.5/3.3 V	—
TV_{DD}	AC17, AG18, AK20	TSEC3 and TSEC4 I/O voltage	TV_{DD} 2.5/3.3 V	—
SV_{DD}	H31, J29, K28, K32, L30, M28, M31, N29, R30, T31, U29, V32, W30, Y31, AA29, AB32, AC30, AD31, AE29, AG30, AH31, AJ29, AK32, AL30, AM31	Transceiver Power Supply SerDes	SV_{DD} 1.05/1.1 V	—
XV_{DD}_SRDS1	K26, L24, M27, N25, P26, R24, R28, T27, U25, V26	Serial I/O Power Supply for SerDes Port 1	XV_{DD}_SRDS1 1.05/1.1 V	—

Table 63. MPC8641 Signal Reference by Functional Block (continued)

Name[1]	Package Pin Number	Pin Type	Power Supply	Notes
TSEC3_TXD[6:7]/ cfg_tsec3_prtcl[0:1]	AL20, AL19	—	LV_{DD}	—
TSEC4_TXD[0:3]/ cfg_io_ports[0:3]	AC18, AC16, AD18, AD17	—	LV_{DD}	—
TSEC4_TXD[5]/ cfg_tsec4_reduce	AB18	—	LV_{DD}	—
TSEC4_TXD[6:7]/ cfg_tsec4_prtcl[0:1]	AB17, AB16	—	LV_{DD}	—
LAD[0:31]/ cfg_gpporcr[0:31]	A30, E29, C29, D28, D29, H25, B29, A29, C28, L22, M22, A28, C27, H26, G26, B27, B26, A27, E27, G25, D26, E26, G24, F27, A26, A25, C25, H23, K22, D25, F25, H22	—	OV_{DD}	—
$\overline{\text{LWE[0]}}$/ cfg_cpu_boot	E21	—	OV_{DD}	—
$\overline{\text{LWE[1]}}$/ cfg_rio_sys_size	F21	—	OV_{DD}	—
$\overline{\text{LWE[2:3]}}$/ cfg_host_agt[0:1]	D22, E20	—	OV_{DD}	—
LDP[0:3], LA[27] / cfg_core_pll[0:4]	A24, E24, C24, B24, J21	—	OV_{DD}	22
LA[28:31]/ cfg_sys_pll[0:3]	K21, G22, F24, G21	—	OV_{DD}	22
LGPL[3], LGPL[5]/ cfg_boot_seq[0:1]	K20, J19	—	OV_{DD}	—
D1_MSRCID[0]/ cfg_mem_debug	F15	—	OV_{DD}	—
D1_MSRCID[1]/ cfg_ddr_debug	K15	—	OV_{DD}	—

Table 65. Memory Bus Clocking Specifications

Characteristic	Maximum Processor Core Frequency		Unit	Notes
	1000, 1250, 1333, 1500MHz			
	Min	Max		
Memory bus clock frequency	200	300	MHz	1, 2

Notes:
1. **Caution:** The MPX clock to SYSCLK ratio and e600 core to MPX clock ratio settings must be chosen such that the resulting SYSCLK frequency, e600 (core) frequency, and MPX clock frequency do not exceed their respective maximum or minimum operating frequencies. Refer to Section 18.2, "MPX to SYSCLK PLL Ratio," and Section 18.3, "e600 to MPX clock PLL Ratio," for ratio settings.
2. The memory bus clock speed is half the DDR/DDR2 data rate, hence, half the MPX clock frequency.

Table 66. Platform/MPX bus Clocking Specifications

Characteristic	Maximum Processor Core Frequency		Unit	Notes
	1000, 1250, 1333, 1500MHz			
	Min	Max		
Platform/MPX bus clock frequency	400	500-600	MHz	1, 2

Notes:
1. **Caution:** The MPX clock to SYSCLK ratio and e600 core to MPX clock ratio settings must be chosen such that the resulting SYSCLK frequency, e600 (core) frequency, and MPX clock frequency do not exceed their respective maximum or minimum operating frequencies. Refer to Section 18.2, "MPX to SYSCLK PLL Ratio," and Section 18.3, "e600 to MPX clock PLL Ratio," for ratio settings.
2. Platform/MPX frequencies between 400 and 500 MHz are not supported.

Table 67. Local Bus Clocking Specifications

Characteristic	Maximum Processor Core Frequency		Unit	Notes
	1000, 1250, 1333, 1500MHz			
	Min	Max		
Local bus clock speed (for Local Bus Controller)	25	133	MHz	1

Notes:
1. The Local bus clock speed on LCLK[0:2] is determined by MPX clock divided by the Local Bus PLL ratio programmed in LCRR[CLKDIV]. See the reference manual for the MPC8641D for more information on this.

18.2 MPX to SYSCLK PLL Ratio

The MPX clock is the clock that drives the MPX bus, and is also called the platform clock. The frequency of the MPX is set using the following reset signals, as shown in Table 68:

- SYSCLK input signal

example, assuming a T_i of 30°C, a T_r of 5°C, a package $R_{\theta JC}$ = 0.1, and a typical power consumption (P_d) of 43.4 W, the following expression for T_j is obtained:

Die-junction temperature: $T_j = 30°C + 5°C + (0.1°C/W + 0.2°C/W + \theta_{sa}) \times 43.4\ W$

For this example, a $R_{\theta sa}$ value of 1.32 °C/W or less is required to maintain the die junction temperature below the maximum value of Table 2.

Though the die junction-to-ambient and the heat sink-to-ambient thermal resistances are a common figure-of-merit used for comparing the thermal performance of various microelectronic packaging technologies, one should exercise caution when only using this metric in determining thermal management because no single parameter can adequately describe three-dimensional heat flow. The final die-junction operating temperature is not only a function of the component-level thermal resistance, but the system-level design and its operating conditions. In addition to the component's power consumption, a number of factors affect the final operating die-junction temperature—airflow, board population (local heat flux of adjacent components), heat sink efficiency, heat sink placement, next-level interconnect technology, system air temperature rise, altitude, and so on.

Due to the complexity and variety of system-level boundary conditions for today's microelectronic equipment, the combined effects of the heat transfer mechanisms (radiation, convection, and conduction) may vary widely. For these reasons, we recommend using conjugate heat transfer models for the board as well as system-level designs.

For system thermal modeling, the MPC8641 thermal model is shown in Figure 62. Four cuboids are used to represent this device. The die is modeled as 12.4x15.3 mm at a thickness of 0.86 mm. See Section 3, "Power Characteristics" for power dissipation details. The substrate is modeled as a single block 33x33x1.2 mm with orthotropic conductivity: 13.5 W/(m • K) in the xy-plane and 5.3 W/(m • K) in the z-direction. The die is centered on the substrate. The bump/underfill layer is modeled as a collapsed thermal resistance between the die and substrate with a conductivity of 5.3 W/(m • K) in the thickness dimension of 0.07 mm. Because the bump/underfill is modeled with zero physical dimension (collapsed height), the die thickness was slightly enlarged to provide the correct height. The C5 solder layer is modeled as a cuboid with dimensions 33x33x0.4 mm and orthotropic thermal conductivity of 0.034 W/(m • K) in the xy-plane and 9.6 W/(m • K) in the z-direction. An LGA solder layer would be modeled as a collapsed thermal resistance with thermal conductivity of 9.6W/(m • K) and an effective height of 0.1 mm. The thermal model uses approximate dimensions to reduce grid. Please refer to the case outline for actual dimensions.

For other pin pull-up or pull-down recommendations of signals, please see Section 17, "Signal Listings."

20.7 Output Buffer DC Impedance

The MPC8641 drivers are characterized over process, voltage, and temperature. For all buses, the driver is a push-pull single-ended driver type (open drain for I^2C).

To measure Z_0 for the single-ended drivers, an external resistor is connected from the chip pad to OV_{DD} or GND. Then, the value of each resistor is varied until the pad voltage is $OV_{DD}/2$ (see Figure 66). The output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held high, SW1 is closed (SW2 is open) and R_P is trimmed until the voltage at the pad equals $OV_{DD}/2$. R_P then becomes the resistance of the pull-up devices. R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N)/2$.

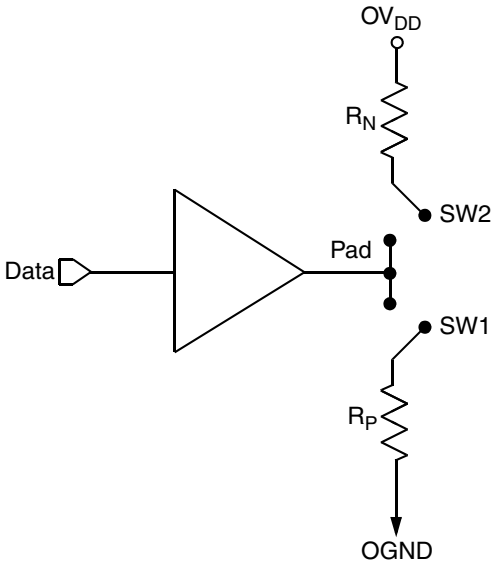


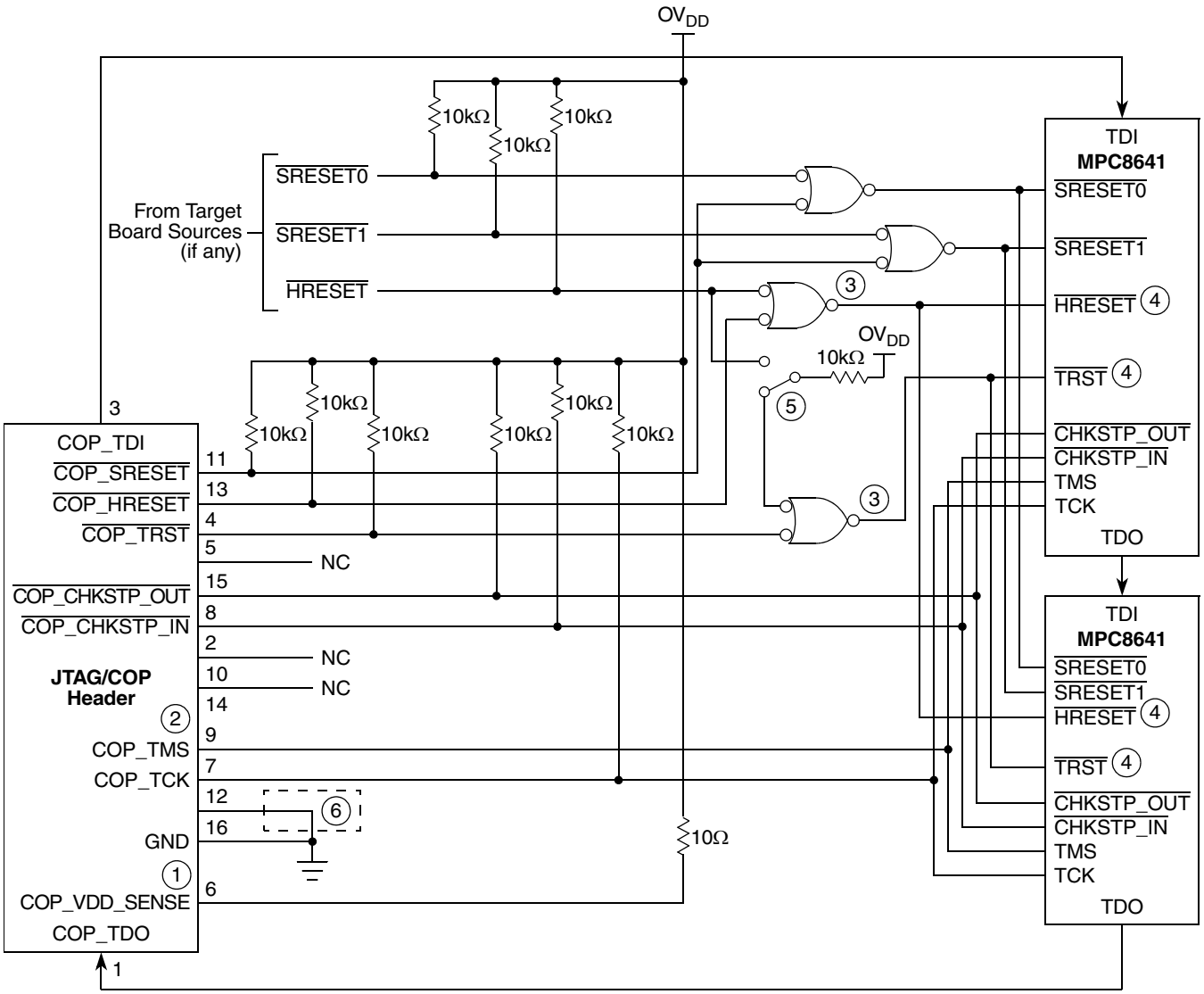
Figure 66. Driver Impedance Measurement

Table 73 summarizes the signal impedance targets. The driver impedances are targeted at minimum V_{DD}, nominal OV_{DD}, 105°C.

Table 73. Impedance Characteristics

Impedance	DUART, Control, Configuration, Power Management	PCI Express	DDR DRAM	Symbol	Unit
R_N	43 Target	25 Target	20 Target	Z_0	W
R_P	43 Target	25 Target	20 Target	Z_0	W

Note: Nominal supply voltages. See Table 1, T_j = 105°C.



Notes:

1. Populate this with a 10Ω resistor for short circuit/current-limiting protection.
2. KEY location; pin 14 is not physically present on the COP header.
3. Use a AND gate with sufficient drive strength to drive two inputs.
4. The COP port and target board should be able to independently assert $\overline{\text{HRESET}}$ and $\overline{\text{TRST}}$ to the processor in order to fully control the processor as shown above.
5. This switch is included as a precaution for BSDL testing. The switch should be open during BSDL testing to avoid accidentally asserting the $\overline{\text{TRST}}$ line. If BSDL testing is not being performed, this switch should be closed or removed.
6. Although pin 12 is defined as a No-Connect, some debug tools may use pin 12 as an additional GND pin for improved signal integrity.

Figure 69. JTAG/COP Interface Connection for Multiple MPC8641 Devices in Daisy Chain Configuration

Table 75 shows the parts that are available for ordering and their operating conditions.

Table 75. Part Offerings and Operating Conditions

Part Offerings[1]	Operating Conditions
MC8641Dxx1500KX	Dual core Max CPU speed = 1500 MHz, Max DDR = 600 MHz Core Voltage = 1.1 volts
MC8641Dxx1333JX	Dual core Max CPU speed = 1333 MHz, Max DDR = 533 MHz Core Voltage = 1.05 volts
MC8641Dxx1250HX	Dual core Max CPU speed = 1250 MHz, Max DDR = 500 MHz Core Voltage = 1.05 volts
MC8641Dxx1000GX	Dual core Max CPU speed = 1000 MHz, Max DDR = 400 MHz Core Voltage = 1.05 volts
MC8641Dxx1000NX	Dual core MAX CPU speed = 1000 MHz, MAX DDR = 500 MHz Core Voltage = 0.95 volts
MC8641xx1500KX	Single core Max CPU speed = 1500 MHz, Max DDR = 600 MHz Core Voltage = 1.1 volts
MC8641xx1333JX	Single core Max CPU speed = 1333 MHz, Max DDR = 533 MHz Core Voltage = 1.05 volts
MC8641xx1250HX	Single core Max CPU speed = 1250 MHz, Max DDR = 500 MHz Core Voltage = 1.05 volts
MC8641xx1000HX	Single core Max CPU speed = 1000 MHz, Max DDR = 400 MHz Core Voltage = 1.05 volts
MC8641xx1000NX	Single core Max CPU speed = 1000 MHz, Max DDR = 500 MHz Core Voltage = 0.95 volts

[1] Note that the “xx” in the part marking represents the package option. The upper case “X” represents the revision letter. For more information see Table 74.