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### Understanding [Embedded - Microprocessors](#)

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

### Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

#### Details

Product Status	Obsolete
Core Processor	PowerPC e600
Number of Cores/Bus Width	2 Core, 32-Bit
Speed	1.0GHz
Co-Processors/DSP	-
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (4)
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	-
Package / Case	1023-BCBGA, FCCBGA
Supplier Device Package	1023-FCCBGA (33x33)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/nxp-semiconductors/mc8641dtvu1000gc">https://www.e-xfl.com/product-detail/nxp-semiconductors/mc8641dtvu1000gc</a>

## 1.1 Key Features

The following lists an overview of the MPC8641 key feature set:

- Major features of the e600 core are as follows:
  - High-performance, 32-bit superscalar microprocessor that implements the PowerPC ISA
  - Eleven independent execution units and three register files
    - Branch processing unit (BPU)
    - Four integer units (IUs) that share 32 GPRs for integer operands
    - 64-bit floating-point unit (FPU)
    - Four vector units and a 32-entry vector register file (VRs)
    - Three-stage load/store unit (LSU)
  - Three issue queues, FIQ, VIQ, and GIQ, can accept as many as one, two, and three instructions, respectively, in a cycle.
  - Rename buffers
  - Dispatch unit
  - Completion unit
  - Two separate 32-Kbyte instruction and data level 1 (L1) caches
  - Integrated 1-Mbyte, eight-way set-associative unified instruction and data level 2 (L2) cache with ECC
  - 36-bit real addressing
  - Separate memory management units (MMUs) for instructions and data
  - Multiprocessing support features
  - Power and thermal management
  - Performance monitor
  - In-system testability and debugging features
  - Reliability and serviceability
- MPX coherency module (MCM)
  - Ten local address windows plus two default windows
  - Optional low memory offset mode for core 1 to allow for address disambiguation
- Address translation and mapping units (ATMUs)
  - Eight local access windows define mapping within local 36-bit address space
  - Inbound and outbound ATMUs map to larger external address spaces
  - Three inbound windows plus a configuration window on PCI Express
  - Four inbound windows plus a default window on serial RapidIO
  - Four outbound windows plus default translation for PCI Express
  - Eight outbound windows plus default translation for serial RapidIO with segmentation and sub-segmentation support

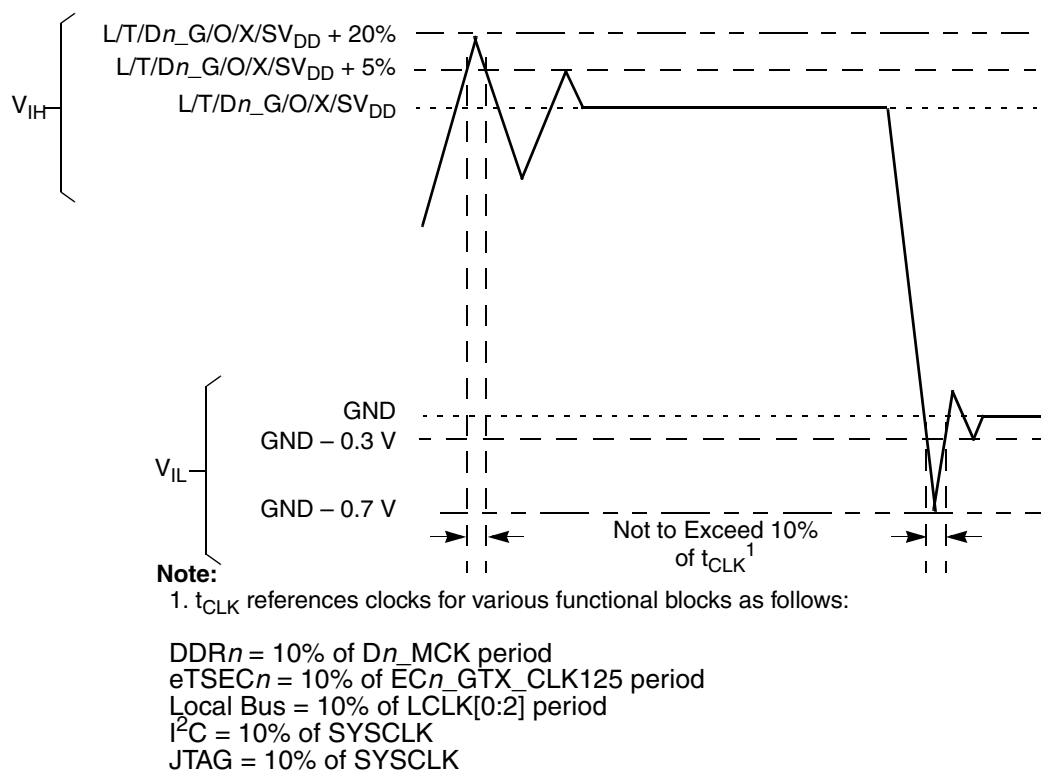
Table 2. Recommended Operating Conditions (continued)

Characteristic	Symbol	Recommended Value	Unit	Notes
Junction temperature range	$T_J$	0 to 105	°C	—

**Notes:**

- Core 1 characteristics apply only to MPC8641D
- If two separate power supplies are used for  $V_{DD\_Core0}$  and  $V_{DD\_Core1}$ , they must be at the same nominal voltage and the individual power supplies must be tracked and kept within 100 mV of each other during normal run time.
- Caution:**  $Dn\_MV_{IN}$  must meet the overshoot/undershoot requirements for  $Dn\_GV_{DD}$  as shown in [Figure 2](#).
- Caution:**  $L/TV_{IN}$  must meet the overshoot/undershoot requirements for  $L/TV_{DD}$  as shown in [Figure 2](#) during regular run time.
- Caution:**  $OV_{IN}$  must meet the overshoot/undershoot requirements for  $OV_{DD}$  as shown in [Figure 2](#) during regular run time.
- Timing limitations for  $M,L,T,O)V_{IN}$  and  $Dn\_MV_{REF}$  during regular run time is provided in [Figure 2](#)
- Applies to devices marked with a core frequency of 1333 MHz and below. Refer to [Table 74](#) Part Numbering Nomenclature to determine if the device has been marked for a core frequency of 1333 MHz and below.
- Applies to devices marked with a core frequency above 1333 MHz. Refer to [Table 74](#) Part Numbering Nomenclature to determine if the device has been marked for a core frequency above 1333 MHz.
- The 2.5 V  $\pm$  125 mV range is for DDR and 1.8 V  $\pm$  90 mV range is for DDR2.
- See [Section 8.2, “FIFO, GMII, MII, TBI, RGMII, RMII, and RTBI AC Timing Specifications,”](#) for details on the recommended operating conditions per protocol.
- The PCI Express interface of the device is expected to receive signals from 0.175 to 1.2 V. For more information refer to [Section 14.4.3, “Differential Receiver \(RX\) Input Specifications.”](#)
- Applies to Part Number MC8641xxx1000NX only.  $V_{DD\_Coren} = 0.95$  V and  $V_{DD\_PLAT} = 1.05$  V devices. Refer to [Table 74](#) Part Numbering Nomenclature to determine if the device has been marked for  $V_{DD\_Coren} = 0.95$  V.
- This voltage is the input to the filter discussed in [Section 20.2, “Power Supply Design and Sequencing,”](#) and not necessarily the voltage at the  $AV_{DD\_Coren}$  pin, which may be reduced from  $V_{DD\_Coren}$  by the filter.

Figure 2 shows the undershoot and overshoot voltages at the interfaces of the MPC8641.



**Figure 2. Overshoot/Undershoot Voltage for  $Dn\_M/O/L/TV_{IN}$**

The MPC8641 core voltage must always be provided at nominal  $V_{DD\_Coren}$  (See Table 2 for actual recommended core voltage). Voltage to the processor interface I/Os are provided through separate sets of supply pins and must be provided at the voltages shown in Table 2. The input voltage threshold scales with respect to the associated I/O supply voltage.  $OV_{DD}$  and  $L/TV_{DD}$  based receivers are simple CMOS I/O circuits and satisfy appropriate LVCMOS type specifications. The DDR SDRAM interface uses a single-ended differential receiver referenced to each externally supplied  $Dn\_MV_{REF}$  signal (nominally set to  $Dn\_GV_{DD}/2$ ) as is appropriate for the (SSTL-18 and SSTL-25) electrical signaling standards.

should meet the MPC8641 input cycle-to-cycle jitter requirement. Frequency modulation and spread are separate concerns, and the MPC8641 is compatible with spread spectrum sources if the recommendations listed in [Table 9](#) are observed.

**Table 9. Spread Spectrum Clock Source Recommendations**

At recommended operating conditions. See [Table 2](#).

Parameter	Min	Max	Unit	Notes
Frequency modulation	—	50	kHz	1
Frequency spread	—	1.0	%	1, 2

**Notes:**

1. Guaranteed by design.
2. SYSCLK frequencies resulting from frequency spreading, and the resulting core and VCO frequencies, must meet the minimum and maximum specifications given in [Table 8](#).

It is imperative to note that the processor's minimum and maximum SYSCLK, core, and VCO frequencies must not be exceeded regardless of the type of clock source. Therefore, systems in which the processor is operated at its maximum rated e600 core frequency should avoid violating the stated limits by using down-spreading only.

$SDn\_REF\_CLK$  and  $SDn\_REF\_CLK$  was designed to work with a spread spectrum clock (+0 to 0.5% spreading at 30–33kHz rate is allowed), assuming both ends have same reference clock. For better results use a source without significant unintended modulation.

## 4.2 Real Time Clock Timing

The RTC input is sampled by the platform clock (MPX clock). The output of the sampling latch is then used as an input to the counters of the PIC. There is no jitter specification. The minimum pulse width of the RTC signal should be greater than 2x the period of the MPX clock. That is, minimum clock high time is  $2 \times t_{MPX}$ , and minimum clock low time is  $2 \times t_{MPX}$ . There is no minimum RTC frequency; RTC may be grounded if not needed.

## 4.3 eTSEC Gigabit Reference Clock Timing

[Table 10](#) provides the eTSEC gigabit reference clocks (EC1\_GTX\_CLK125 and EC2\_GTX\_CLK125) AC timing specifications for the MPC8641.

**Table 10. ECn\_GTX\_CLK125 AC Timing Specifications**

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
ECn_GTX_CLK125 frequency	$f_{G125}$	—	125 ± 100 ppm	—	MHz	3
ECn_GTX_CLK125 cycle time	$t_{G125}$	—	8	—	ns	—
ECn_GTX_CLK125 peak-to-peak jitter	$t_{G125J}$	—	—	250	ps	1

## 8 Ethernet: Enhanced Three-Speed Ethernet (eTSEC), MII Management

This section provides the AC and DC electrical characteristics for enhanced three-speed and MII management.

### 8.1 Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1Gb Mbps)—GMII/MII/TBI/RGMII/RTBI/RMII Electrical Characteristics

The electrical characteristics specified here apply to all gigabit media independent interface (GMII), media independent interface (MII), ten-bit interface (TBI), reduced gigabit media independent interface (RGMII), reduced ten-bit interface (RTBI), and reduced media independent interface (RMII) signals except management data input/output (MDIO) and management data clock (MDC). The RGMII and RTBI interfaces are defined for 2.5 V, while the GMII and TBI interfaces can be operated at 3.3 or 2.5 V. Whether the GMII or TBI interface is operated at 3.3 or 2.5 V, the timing is compatible with IEEE 802.3. The RGMII and RTBI interfaces follow the Reduced Gigabit Media-Independent Interface (RGMII) Specification Version 1.3 (12/10/2000). The RMII interface follows the RMII Consortium RMII Specification Version 1.2 (3/20/1998). The electrical characteristics for MDIO and MDC are specified in [Section 9, “Ethernet Management Interface Electrical Characteristics.”](#)

#### 8.1.1 eTSEC DC Electrical Characteristics

All GMII, MII, TBI, RGMII, RMII and RTBI drivers and receivers comply with the DC parametric attributes specified in [Table 24](#) and [Table 25](#). The potential applied to the input of a GMII, MII, TBI, RGMII, RMII or RTBI receiver may exceed the potential of the receiver’s power supply (that is, a GMII driver powered from a 3.6-V supply driving  $V_{OH}$  into a GMII receiver powered from a 2.5-V supply). Tolerance for dissimilar GMII driver and receiver supply potentials is implicit in these specifications. The RGMII and RTBI signals are based on a 2.5-V CMOS interface voltage as defined by JEDEC EIA/JESD8-5.

**Table 24. GMII, MII, RMII, TBI and FIFO DC Electrical Characteristics**

Parameter	Symbol	Min	Max	Unit	Notes
Supply voltage 3.3 V	$LV_{DD}$ $TV_{DD}$	3.135	3.465	V	1, 2
Output high voltage ( $LV_{DD}/TV_{DD} = \text{Min}$ , $I_{OH} = -4.0 \text{ mA}$ )	$V_{OH}$	2.40	—	V	—
Output low voltage ( $LV_{DD}/TV_{DD} = \text{Min}$ , $I_{OL} = 4.0 \text{ mA}$ )	$V_{OL}$	—	0.50	V	—
Input high voltage	$V_{IH}$	2.0	—	V	—
Input low voltage	$V_{IL}$	—	0.90	V	—
Input high current ( $V_{IN} = LV_{DD}$ , $V_{IN} = TV_{DD}$ )	$I_{IH}$	—	40	$\mu\text{A}$	1, 2,3

**Table 35. RGMII and RTBI AC Timing Specifications (continued)**

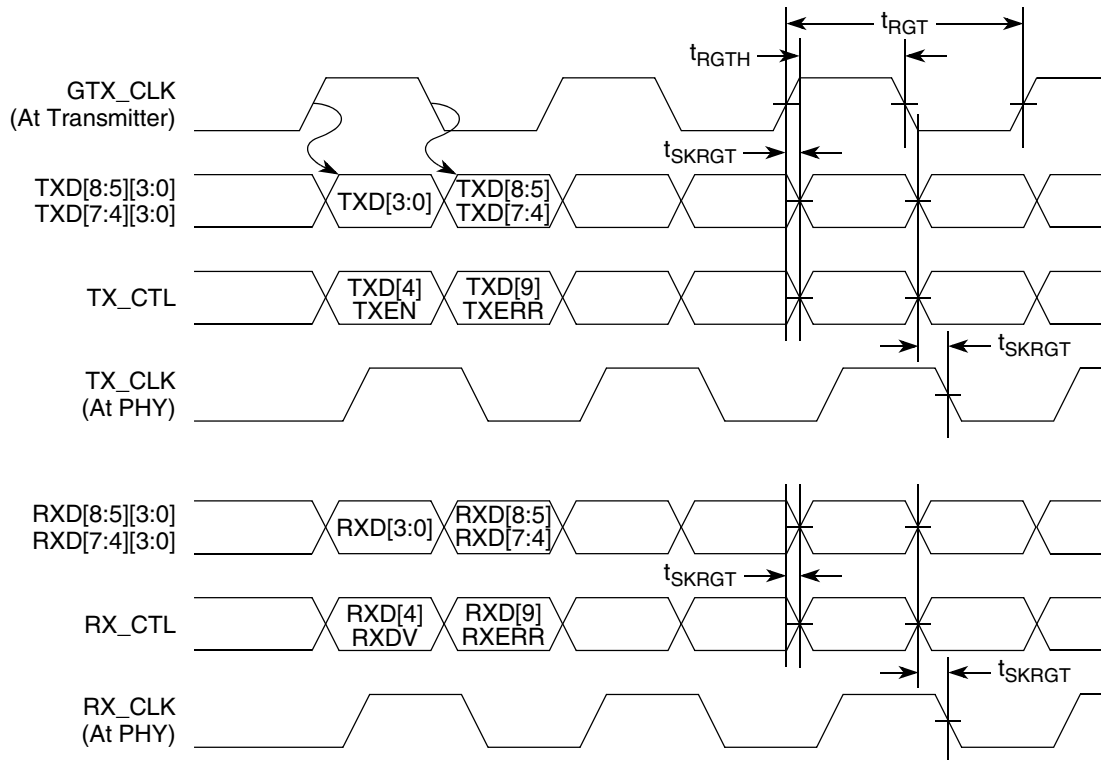
At recommended operating conditions with L/TV<sub>DD</sub> of 2.5 V ± 5%.

Parameter/Condition	Symbol <sup>1</sup>	Min	Typ	Max	Unit
Clock period duration <sup>3</sup>	$t_{RGT}^{5,6}$	7.2	8.0	8.8	ns
Duty cycle for 10BASE-T and 100BASE-TX <sup>3, 4</sup>	$t_{RGTH}/t_{RGT}^{5}$	40	50	60	%
Rise time (20%–80%)	$t_{RGTR}^{5}$	—	—	0.75	ns
Fall time (80%–20%)	$t_{RGTF}^{5}$	—	—	0.75	ns

**Notes:**

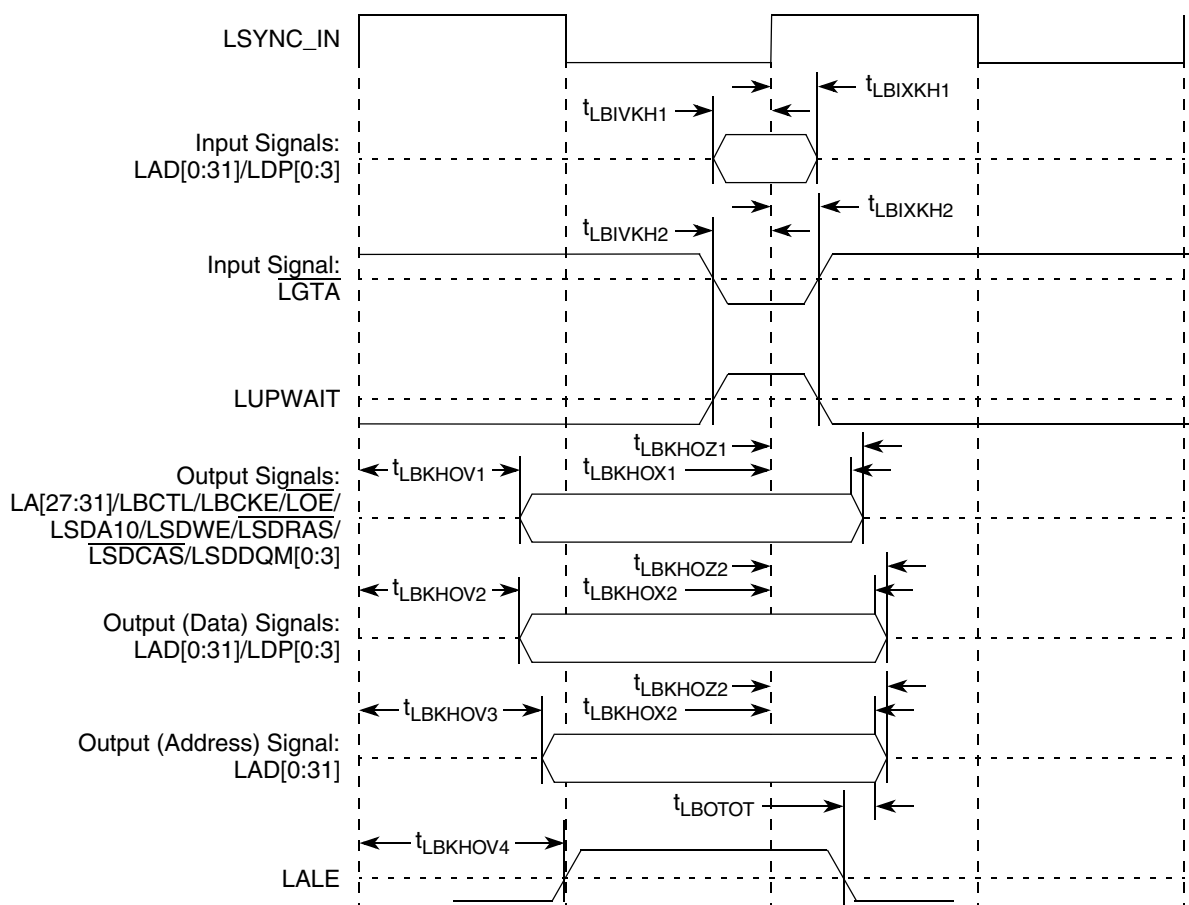
- Note that, in general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII and RTBI timing. For example, the subscript of  $t_{RGT}$  represents the TBI (T) receive (RX) clock. Note also that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).
- This implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 1.5 ns will be added to the associated clock signal.
- For 10 and 100 Mbps,  $t_{RGT}$  scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
- Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three  $t_{RGT}$  of the lowest speed transitioned between.
- Guaranteed by characterization
- ±100 ppm tolerance on RX\_CLK frequency

Figure 19 shows the RGMII and RTBI AC timing and multiplexing diagrams.



**Figure 19. RGMII and RTBI AC Timing and Multiplexing Diagrams**

Figure 26 to Figure 31 show the local bus signals.



**Figure 26. Local Bus Signals (PLL Enabled)**

#### NOTE

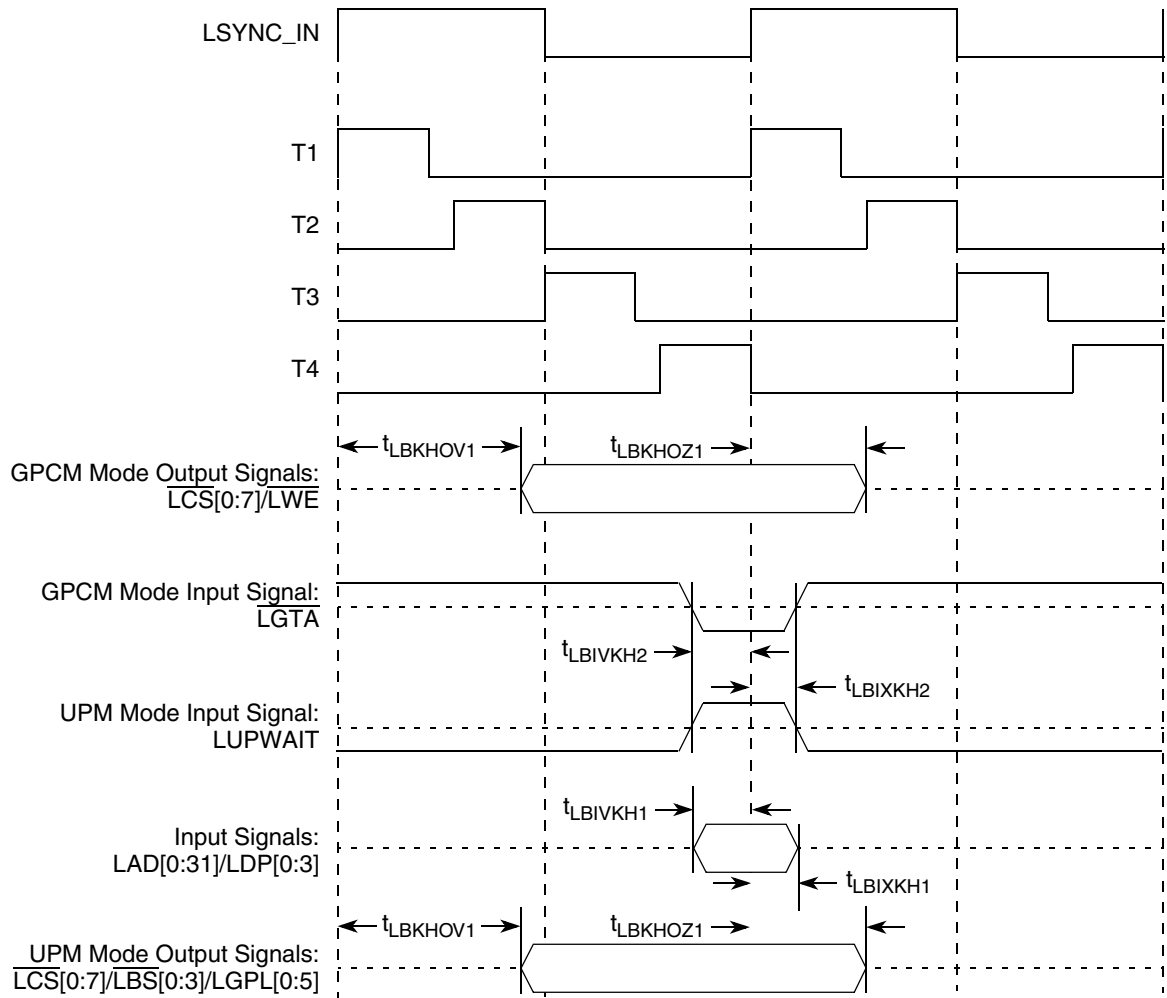
PLL bypass mode is recommended when LBIU frequency is at or below 83 MHz. When LBIU operates above 83 MHz, LBIU PLL is recommended to be enabled.

Table 42 describes the general timing parameters of the local bus interface at  $OV_{DD} = 3.3\text{ V}$  with PLL bypassed.

**Table 42. Local Bus Timing Parameters—PLL Bypassed**

Parameter	Symbol <sup>1</sup>	Min	Max	Unit	Notes
Local bus cycle time	$t_{LBK}$	12	—	ns	2
Local bus duty cycle	$t_{LBKH}/t_{LBK}$	45	55	%	—
Internal launch/capture clock to LCLK delay	$t_{LBKHK T}$	2.3	3.9	ns	8
Input setup to local bus clock (except $\overline{LGTA}/LUPWAIT$ )	$t_{LBIVKH1}$	5.7	—	ns	4, 5
$\overline{LGTA}/LUPWAIT$ input setup to local bus clock	$t_{LBIVKL2}$	5.6	—	ns	4, 5
Input hold from local bus clock (except $\overline{LGTA}/LUPWAIT$ )	$t_{LBIXKH1}$	−1.8	—	ns	4, 5





**Figure 30. Local Bus Signals, GPCM/UPM Signals for  $\text{LCRR}[\text{CLKDIV}] = 4$  or  $8$  (clock ratio of 8 or 16) (PLL Enabled)**

# 11 JTAG

This section describes the DC and AC electrical specifications for the IEEE 1149.1 (JTAG) interface of the MPC8641/D.

## 11.1 JTAG DC Electrical Characteristics

Table 43 provides the DC electrical characteristics for the JTAG interface.

**Table 43. JTAG DC Electrical Characteristics**

Parameter	Symbol	Min	Max	Unit
High-level input voltage	$V_{IH}$	2	$OV_{DD} + 0.3$	V
Low-level input voltage	$V_{IL}$	-0.3	0.8	V
Input current ( $V_{IN}^1 = 0$ V or $V_{IN} = V_{DD}$ )	$I_{IN}$	—	$\pm 5$	$\mu A$
High-level output voltage ( $OV_{DD} = \min$ , $I_{OH} = -100$ $\mu A$ )	$V_{OH}$	$OV_{DD} - 0.2$	—	V
Low-level output voltage ( $OV_{DD} = \min$ , $I_{OL} = 100$ $\mu A$ )	$V_{OL}$	—	0.2	V

**Note:**

1. Note that the symbol  $V_{IN}$ , in this case, represents the  $OV_{IN}$  symbol referenced in Table 1 and Table 2.

## 11.2 JTAG AC Electrical Specifications

Table 44 provides the JTAG AC timing specifications as defined in Figure 33 through Figure 35.

**Table 44. JTAG AC Timing Specifications (Independent of SYSCLK) <sup>1</sup>**

At recommended operating conditions (see Table 3).

Parameter	Symbol <sup>2</sup>	Min	Max	Unit	Notes
JTAG external clock frequency of operation	$f_{JTG}$	0	33.3	MHz	—
JTAG external clock cycle time	$t_{JTG}$	30	—	ns	—
JTAG external clock pulse width measured at 1.4 V	$t_{JTKHKL}$	15	—	ns	—
JTAG external clock rise and fall times	$t_{JTGR}$ & $t_{JTGF}$	0	2	ns	6
$\overline{TRST}$ assert time	$t_{TRST}$	25	—	ns	3
Input setup times:				ns	
Boundary-scan data TMS, TDI	$t_{JTDVKH}$ $t_{JTIVKH}$	4 0	— —		4
Input hold times:				ns	
Boundary-scan data TMS, TDI	$t_{JTDXKH}$ $t_{JTIXKH}$	20 25	— —		4
Valid times:				ns	
Boundary-scan data TDO	$t_{JTKLDV}$ $t_{JTKLOV}$	4 4	20 25		5

**Table 44. JTAG AC Timing Specifications (Independent of SYSCLK) <sup>1</sup> (continued)**

At recommended operating conditions (see Table 3).

Parameter	Symbol <sup>2</sup>	Min	Max	Unit	Notes
Output hold times:				ns	
Boundary-scan data	$t_{JTKLDX}$	30	—		5, 6
TDO	$t_{JKLOX}$	30	—		
JTAG external clock to output high impedance:				ns	
Boundary-scan data	$t_{JTKLDZ}$	3	19		5, 6
TDO	$t_{JKLOZ}$	3	9		

**Notes:**

1. All outputs are measured from the midpoint voltage of the falling/rising edge of  $t_{TCLK}$  to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50- $\Omega$  load (see Figure 32). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbols used for timing specifications herein follow the pattern of  $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)\ (reference)(state)}$  for inputs and  $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$  for outputs. For example,  $t_{JTDVXH}$  symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the  $t_{JTG}$  clock reference (K) going to the high (H) state or setup time. Also,  $t_{JTDVXH}$  symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the  $t_{JTG}$  clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
3.  $\overline{TRST}$  is an asynchronous level sensitive signal. The setup time is for test purposes only.
4. Non-JTAG signal input timing with respect to  $t_{TCLK}$ .
5. Non-JTAG signal output timing with respect to  $t_{TCLK}$ .
6. Guaranteed by design.

Figure 32 provides the AC test load for TDO and the boundary-scan outputs.

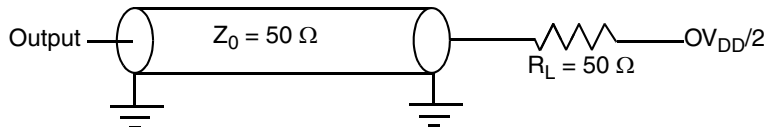
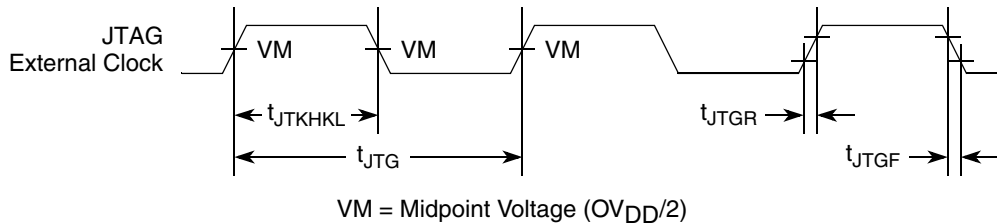

**Figure 32. AC Test Load for the JTAG Interface**

Figure 33 provides the JTAG clock input timing diagram.


**Figure 33. JTAG Clock Input Timing Diagram**

## 14.4.2 Transmitter Compliance Eye Diagrams

The TX eye diagram in Figure 50 is specified using the passive compliance/test measurement load (see Figure 52) in place of any real PCI Express interconnect + RX component.

There are two eye diagrams that must be met for the transmitter. Both eye diagrams must be aligned in time using the jitter median to locate the center of the eye diagram. The different eye diagrams will differ in voltage depending whether it is a transition bit or a de-emphasized bit. The exact reduced voltage level of the de-emphasized bit will always be relative to the transition bit.

The eye diagram must be valid for any 250 consecutive UIs.

A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.

### NOTE

It is recommended that the recovered TX UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function (that is, least squares and median deviation fits).

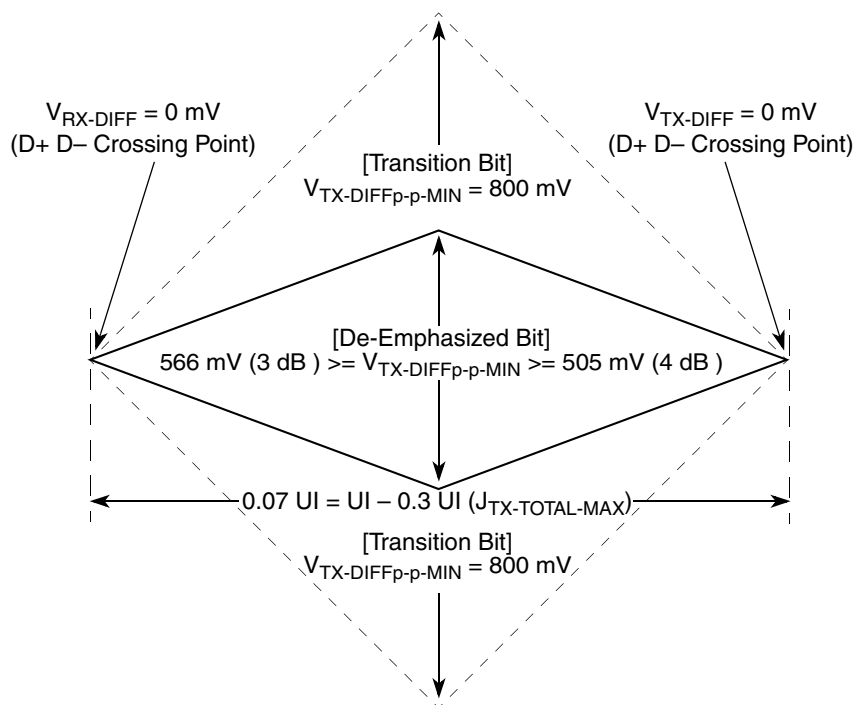


Figure 50. Minimum Transmitter Timing and Voltage Output Compliance Specifications

### 14.4.3 Differential Receiver (RX) Input Specifications

Table 50 defines the specifications for the differential input at all receivers (RXs). The parameters are specified at the component pins.

**Table 50. Differential Receiver (RX) Input Specifications**

Symbol	Parameter	Min	Nom	Max	Units	Comments
UI	Unit Interval	399.88	400	400.12	ps	Each UI is 400 ps $\pm$ 300 ppm. UI does not account for Spread Spectrum Clock dictated variations. See Note 1.
$V_{RX-DIFFp-p}$	Differential Peak-to-Peak Output Voltage	0.175	—	—	V	$V_{RX-DIFFp-p} = 2 \cdot  V_{RX-D+} - V_{RX-D-} $ See Note 2.
$T_{RX-EYE}$	Minimum Receiver Eye Width	0.4	—	—	UI	The maximum interconnect media and Transmitter jitter that can be tolerated by the Receiver can be derived as $T_{RX-MAX-JITTER} = 1 - T_{RX-EYE} = 0.6$ UI. See Notes 2 and 3.
$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time between the jitter median and maximum deviation from the median.	—	—	0.3	UI	Jitter is defined as the measurement variation of the crossing points ( $V_{RX-DIFFp-p} = 0$ V) in relation to a recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI. See Notes 2, 3 and 7.
$V_{RX-CM-ACp}$	AC Peak Common Mode Input Voltage	—	—	150	mV	$V_{RX-CM-ACp} =  V_{RXD+} - V_{RXD-} /2 - V_{RX-CM-DC}$ $V_{RX-CM-DC} = DC_{(avg)}$ of $ V_{RX-D+} - V_{RX-D-} /2$ See Note 2
$RL_{RX-DIFF}$	Differential Return Loss	15	—	—	dB	Measured over 50 MHz to 1.25 GHz with the D+ and D– lines biased at +300 mV and –300 mV, respectively. See Note 4
$RL_{RX-CM}$	Common Mode Return Loss	6	—	—	dB	Measured over 50 MHz to 1.25 GHz with the D+ and D– lines biased at 0 V. See Note 4
$Z_{RX-DIFF-DC}$	DC Differential Input Impedance	80	100	120	$\Omega$	RX DC Differential mode impedance. See Note 5
$Z_{RX-DC}$	DC Input Impedance	40	50	60	$\Omega$	Required RX D+ as well as D– DC Impedance ( $50 \pm 20\%$ tolerance). See Notes 2 and 5.
$Z_{RX-HIGH-IMP-DC}$	Powered Down DC Input Impedance	200 k	—	—	$\Omega$	Required RX D+ as well as D– DC Impedance when the Receiver terminations do not have power. See Note 6.
$V_{RX-IDLE-DET-DIFFp-p}$	Electrical Idle Detect Threshold	65	—	—	mV	$V_{RX-IDLE-DET-DIFFp-p} = 2 \cdot  V_{RX-D+} - V_{RX-D-} $ Measured at the package pins of the Receiver

Table 51. SDn\_REF\_CLK and  $\overline{\text{SDn\_REF\_CLK}}$  AC Requirements

Symbol	Parameter Description	Min	Typical	Max	Units	Comments
$t_{\text{REF}}$	REFCLK cycle time	—	10(8)	—	ns	8 ns applies only to serial RapidIO with 125-MHz reference clock
$t_{\text{REFCJ}}$	REFCLK cycle-to-cycle jitter. Difference in the period of any two adjacent REFCLK cycles	—	—	80	ps	—
$t_{\text{REFPJ}}$	Phase jitter. Deviation in edge location with respect to mean edge location	–40	—	40	ps	—

## 15.3 Signal Definitions

LP-Serial links use differential signaling. This section defines terms used in the description and specification of differential signals. Figure 53 shows how the signals are defined. The figures show waveforms for either a transmitter output (TD and  $\overline{\text{TD}}$ ) or a receiver input (RD and  $\overline{\text{RD}}$ ). Each signal swings between A Volts and B Volts where  $A > B$ . Using these waveforms, the definitions are as follows:

1. The transmitter output signals and the receiver input signals TD,  $\overline{\text{TD}}$ , RD and  $\overline{\text{RD}}$  each have a peak-to-peak swing of  $A - B$  Volts
2. The differential output signal of the transmitter,  $V_{\text{OD}}$ , is defined as  $V_{\text{TD}} - V_{\overline{\text{TD}}}$
3. The differential input signal of the receiver,  $V_{\text{ID}}$ , is defined as  $V_{\text{RD}} - V_{\overline{\text{RD}}}$
4. The differential output signal of the transmitter and the differential input signal of the receiver each range from  $A - B$  to  $-(A - B)$  Volts
5. The peak value of the differential transmitter output signal and the differential receiver input signal is  $A - B$  Volts
6. The peak-to-peak value of the differential transmitter output signal and the differential receiver input signal is  $2 * (A - B)$  Volts

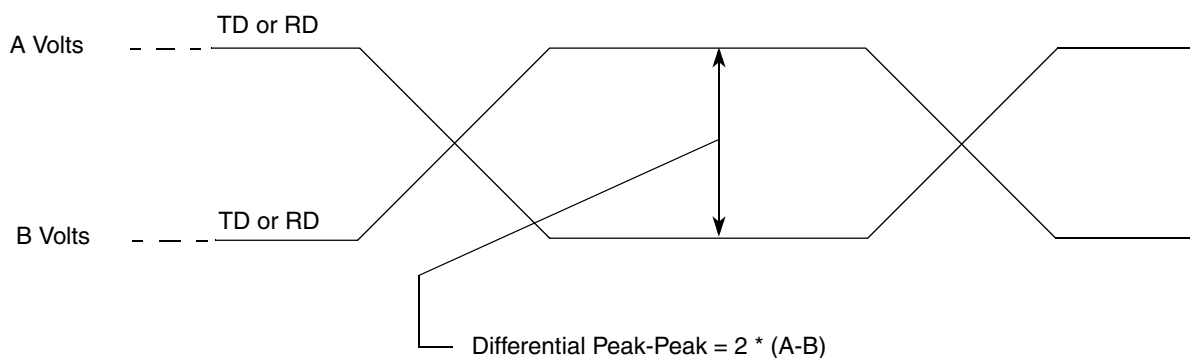


Figure 53. Differential Peak-Peak Voltage of Transmitter or Receiver

To illustrate these definitions using real values, consider the case of a CML (Current Mode Logic) transmitter that has a common mode voltage of 2.25 V and each of its outputs, TD and  $\overline{\text{TD}}$ , has a swing that goes between 2.5V and 2.0V. Using these values, the peak-to-peak voltage swing of the signals TD and  $\overline{\text{TD}}$  is 500 mV p-p. The differential output signal ranges between 500 mV and –500 mV. The peak differential voltage is 500 mV. The peak-to-peak differential voltage is 1000 mV p-p.

Continuous Jitter Test Pattern (CJPAT) defined in Annex 48A of IEEE 802.3ae. All lanes of the LP-Serial link shall be active in both the transmit and receive directions, and opposite ends of the links shall use asynchronous clocks. Four lane implementations shall use CJPAT as defined in Annex 48A. Single lane implementations shall use the CJPAT sequence specified in Annex 48A for transmission on lane 0. The amount of data represented in the eye shall be adequate to ensure that the bit error ratio is less than  $10^{-12}$ . The eye pattern shall be measured with AC coupling and the compliance template centered at 0 Volts differential. The left and right edges of the template shall be aligned with the mean zero crossing points of the measured data eye. The load for this test shall be 100  $\Omega$  resistive  $\pm 5\%$  differential to 2.5 GHz.

### 15.9.2 Jitter Test Measurements

For the purpose of jitter measurement, the effects of a single-pole high pass filter with a 3 dB point at (Baud Frequency)/1667 is applied to the jitter. The data pattern for jitter measurements is the Continuous Jitter Test Pattern (CJPAT) pattern defined in Annex 48A of IEEE 802.3ae. All lanes of the LP-Serial link shall be active in both the transmit and receive directions, and opposite ends of the links shall use asynchronous clocks. Four lane implementations shall use CJPAT as defined in Annex 48A. Single lane implementations shall use the CJPAT sequence specified in Annex 48A for transmission on lane 0. Jitter shall be measured with AC coupling and at 0 Volts differential. Jitter measurement for the transmitter (or for calibration of a jitter tolerance setup) shall be performed with a test procedure resulting in a BER curve such as that described in Annex 48B of IEEE 802.3ae.

### 15.9.3 Transmit Jitter

Transmit jitter is measured at the driver output when terminated into a load of 100  $\Omega$  resistive  $\pm 5\%$  differential to 2.5 GHz.

### 15.9.4 Jitter Tolerance

Jitter tolerance is measured at the receiver using a jitter tolerance test signal. This signal is obtained by first producing the sum of deterministic and random jitter defined in Section 8.6 and then adjusting the signal amplitude until the data eye contacts the 6 points of the minimum eye opening of the receive template shown in Figure 8-4 and Table 8-11. Note that for this to occur, the test signal must have vertical waveform symmetry about the average value and have horizontal symmetry (including jitter) about the mean zero crossing. Eye template measurement requirements are as defined above. Random jitter is calibrated using a high pass filter with a low frequency corner at 20 MHz and a 20 dB/decade roll-off below this. The required sinusoidal jitter specified in Section 8.6 is then added to the signal and the test load is replaced by the receiver being tested.

Table 63. MPC8641 Signal Reference by Functional Block (continued)

Name <sup>1</sup>	Package Pin Number	Pin Type	Power Supply	Notes
D1_MDVAL/LB_DVAL	J16	O	OV <sub>DD</sub>	10
D2_MDVAL	D19	O	OV <sub>DD</sub>	—
<b>Power Management Signals<sup>5</sup></b>				
ASLEEP	C19	O	OV <sub>DD</sub>	—
<b>System Clocking Signals<sup>5</sup></b>				
SYSCLK	G16	I	OV <sub>DD</sub>	—
RTC	K17	I	OV <sub>DD</sub>	32
CLK_OUT	B16	O	OV <sub>DD</sub>	23
<b>Test Signals<sup>5</sup></b>				
$\overline{\text{LSSD\_MODE}}$	C18	I	OV <sub>DD</sub>	26
TEST_MODE[0:3]	C16, E17, D18, D16	I	OV <sub>DD</sub>	26
<b>JTAG Signals<sup>5</sup></b>				
TCK	H18	I	OV <sub>DD</sub>	—
TDI	J18	I	OV <sub>DD</sub>	24
TDO	G18	O	OV <sub>DD</sub>	23
TMS	F18	I	OV <sub>DD</sub>	24
$\overline{\text{TRST}}$	A17	I	OV <sub>DD</sub>	24
<b>Miscellaneous<sup>5</sup></b>				
Spare	J17	—	—	13
GPOUT[0:7]/ TSEC1_TXD[0:7]	AF25, AC23, AG24, AG23, AE24, AE23, AE22, AD22	O	OV <sub>DD</sub>	6, 10
GPIN[0:7]/ TSEC1_RXD[0:7]	AL25, AL24, AK26, AK25, AM26, AF26, AH24, AG25	I	OV <sub>DD</sub>	10
GPOUT[8:15]/ TSEC2_TXD[0:7]	AB20, AJ23, AJ22, AD19, AH23, AH21, AG22, AG21	O	OV <sub>DD</sub>	10
GPIN[8:15]/ TSEC2_RXD[0:7]	AL22, AK22, AM21, AH20, AG20, AF20, AF23, AF22	I	OV <sub>DD</sub>	10
<b>Additional Analog Signals</b>				
TEMP_ANODE	AA11	Thermal	—	—
TEMP_CATHODE	Y11	Thermal	—	—
<b>Sense, Power and GND Signals</b>				
SENSEV <sub>DD</sub> _Core0	M14	V <sub>DD</sub> _Core0 sensing pin	—	31
SENSEV <sub>DD</sub> _Core1	U20	V <sub>DD</sub> _Core1 sensing pin	—	12,31, S1



Table 63. MPC8641 Signal Reference by Functional Block (continued)

Name <sup>1</sup>	Package Pin Number	Pin Type	Power Supply	Notes
AGND_SRDS1	P30	SerDes Port 1 Ground pin for AV <sub>DD</sub> _SRDS1	—	—
AGND_SRDS2	AF30	SerDes Port 2 Ground pin for AV <sub>DD</sub> _SRDS2	—	—
SGND	H28, H32, J30, K31, L28, L29, M32, N30, R29, T32, U30, V31, W29, Y32 AA30, AB31, AC29, AD32, AE30, AG29, AH32, AJ30, AK31, AL29, AM32	Ground pins for SV <sub>DD</sub>	—	—
XGND	K27, L25, M26, N24, P27, R25, T26, U24, V27, W25, Y28, AA24, AB27, AC25, AD28, AE26, AF27, AH28, AJ26, AK27, AL26, AM28	Ground pins for XV <sub>DD</sub> _SRDS <sub>n</sub>	—	—
<b>Reset Configuration Signals<sup>20</sup></b>				
TSEC1_TXD[0] / cfg_alt_boot_vec	AF25	—	LV <sub>DD</sub>	—
TSEC1_TXD[1] / cfg_platform_freq	AC23	—	LV <sub>DD</sub>	21
TSEC1_TXD[2:4] / cfg_device_id[5:7]	AG24, AG23, AE24	—	LV <sub>DD</sub>	—
TSEC1_TXD[5] / cfg_tsec1_reduce	AE23	—	LV <sub>DD</sub>	—
TSEC1_TXD[6:7] / cfg_tsec1_prtcl[0:1]	AE22, AD22	—	LV <sub>DD</sub>	—
TSEC2_TXD[0:3] / cfg_rom_loc[0:3]	AB20, AJ23, AJ22, AD19	—	LV <sub>DD</sub>	—
TSEC2_TXD[4], TSEC2_TX_ER / cfg_dram_type[0:1]	AH23, AB19	—	LV <sub>DD</sub>	38
TSEC2_TXD[5] / cfg_tsec2_reduce	AH21	—	LV <sub>DD</sub>	—
TSEC2_TXD[6:7] / cfg_tsec2_prtcl[0:1]	AG22, AG21	—	LV <sub>DD</sub>	—
TSEC3_TXD[0:1] / cfg_spare[0:1]	AL21, AJ21	O	TV <sub>DD</sub>	33
TSEC3_TXD[2] / cfg_core1_enable	AM20	O	TV <sub>DD</sub>	—
TSEC3_TXD[3] / cfg_core1_lm_offset	AJ20	—	LV <sub>DD</sub>	—
TSEC3_TXD[5] / cfg_tsec3_reduce	AK21	—	LV <sub>DD</sub>	—

- Binary value on LA[28:31] at power up

Note that there is no default for this PLL ratio; these signals must be pulled to the desired values. Also note that the DDR data rate is the determining factor in selecting the MPX bus frequency, since the MPX frequency must equal the DDR data rate.

**Table 68. MPX:SYSCLK Ratio**

Binary Value of LA[28:31] Signals	MPX:SYSCLK Ratio
0000	Reserved
0001	Reserved
0010	2:1
0011	3:1
0100	4:1
0101	5:1
0110	6:1
0111	Reserved
1000	8:1
1001	9:1

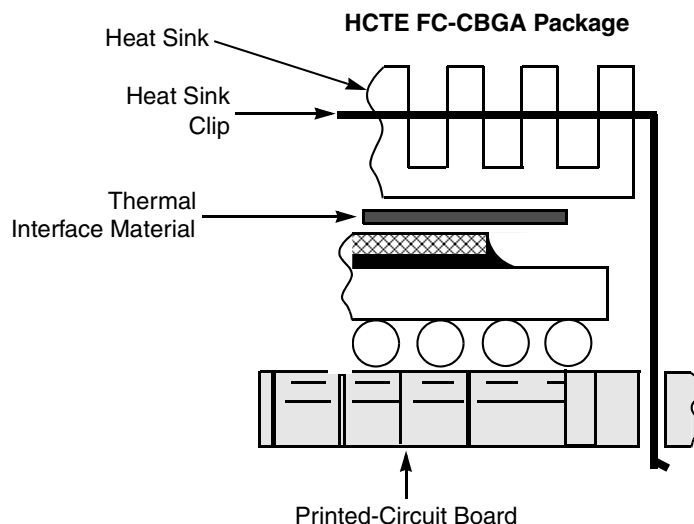
### 18.3 e600 to MPX clock PLL Ratio

[Table 69](#) describes the clock ratio between the platform and the e600 core clock. This ratio is determined by the binary value of LDP[0:3], LA[27](cfg\_core\_pll[0:4] - reset config name) at power up, as shown in [Table 69](#).

**Table 69. e600 Core to MPX Clock Ratio**

Binary Value of LDP[0:3], LA[27] Signals	e600 core: MPX Clock Ratio
01000	2:1
01100	2.5:1
10000	3:1
11100	3.5:1
10100	4:1
01110	4.5:1

### 18.4 Frequency Options



**Figure 59. FC-CBGA Package Exploded Cross-Sectional View with Several Heat Sink Options**

There are several commercially-available heat sinks for the MPC8641 provided by the following vendors:

Aavid Thermalloy 603-224-9988

80 Commercial St.

Concord, NH 03301

Internet: [www.aavidthermalloy.com](http://www.aavidthermalloy.com)

Advanced Thermal Solutions 781-769-2800

89 Access Road #27.

Norwood, MA 02062

Internet: [www.qats.com](http://www.qats.com)

Alpha Novatech 408-749-7601

473 Sapena Ct. #12

Santa Clara, CA 95054

Internet: [www.alphanovatech.com](http://www.alphanovatech.com)

Calgreg Thermal Solutions 888-732-6100

60 Alhambra Road, Suite 1

Warwick, RI 02886

Internet: [www.calgreg.com](http://www.calgreg.com)

International Electronic Research Corporation (IERC) 818-842-7277

413 North Moss St.

Burbank, CA 91502

Internet: [www.ctscorp.com](http://www.ctscorp.com)

Millennium Electronics (MEI) 408-436-8770

Loroco Sites

671 East Brokaw Road

San Jose, CA 95112

Internet: [www.mei-thermal.com](http://www.mei-thermal.com)

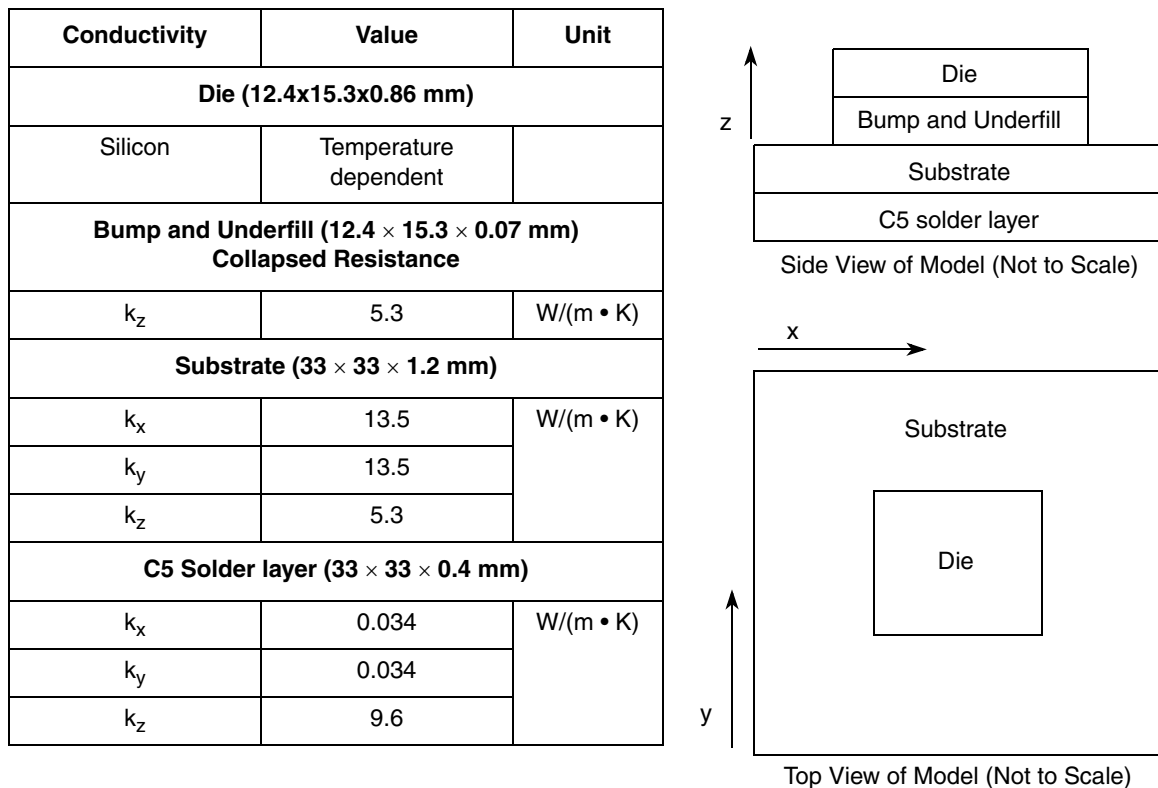


Figure 62. Recommended Thermal Model of MPC8641

## 19.2.4 Temperature Diode

The MPC8641 has a temperature diode on the microprocessor that can be used in conjunction with other system temperature monitoring devices (such as Analog Devices, ADT7461™). These devices use the negative temperature coefficient of a diode operated at a constant current to determine the temperature of the microprocessor and its environment. It is recommended that each device be individually calibrated.

The following are the specifications of the MPC8641 on-board temperature diode:

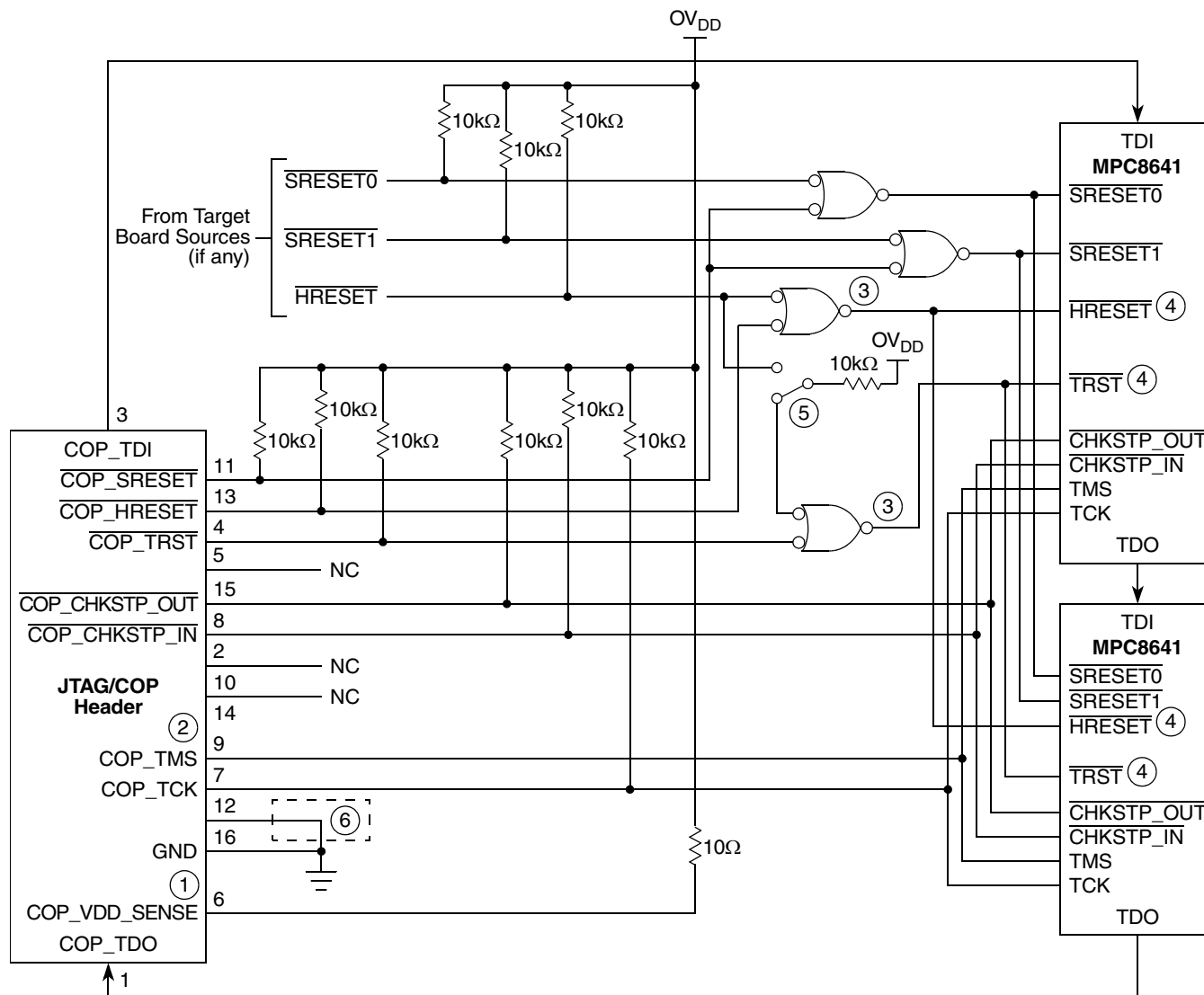
$$V_f > 0.40 \text{ V}$$

$$V_f < 0.90 \text{ V}$$

An approximate value of the ideality may be obtained by calibrating the device near the expected operating temperature.

Ideality factor is defined as the deviation from the ideal diode equation:

$$I_{fw} = I_s \left[ e^{\frac{qV_f}{nKT}} - 1 \right]$$


**Notes:**

1. Populate this with a 10Ω resistor for short circuit/current-limiting protection.
2. KEY location; pin 14 is not physically present on the COP header.
3. Use a AND gate with sufficient drive strength to drive two inputs.
4. The COP port and target board should be able to independently assert  $\overline{\text{HRESET}}$  and  $\overline{\text{TRST}}$  to the processor in order to fully control the processor as shown above.
5. This switch is included as a precaution for BSDL testing. The switch should be open during BSDL testing to avoid accidentally asserting the  $\overline{\text{TRST}}$  line. If BSDL testing is not being performed, this switch should be closed or removed.
6. Although pin 12 is defined as a No-Connect, some debug tools may use pin 12 as an additional GND pin for improved signal integrity.

**Figure 69. JTAG/COP Interface Connection for Multiple MPC8641 Devices in Daisy Chain Configuration**