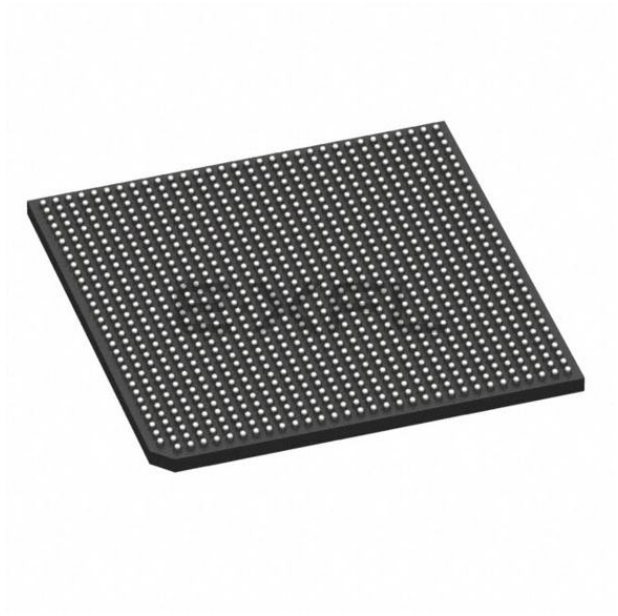

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e600
Number of Cores/Bus Width	2 Core, 32-Bit
Speed	1.333GHz
Co-Processors/DSP	-
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (4)
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	-
Package / Case	1023-BCBGA, FCCBGA
Supplier Device Package	1023-FCCBGA (33x33)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc8641dtvu1333je

Table 1. Absolute Maximum Ratings[1] (continued)

Characteristic		Symbol	Absolute Maximum Value	Unit	Notes
Input voltage	DDR and DDR2 SDRAM signals	D*n*_MV_{IN}	– 0.3 to (D*n*_GV_{DD} + 0.3)	V	5
	DDR and DDR2 SDRAM reference	D*n*_MV_{REF}	– 0.3 to (D*n*_GV_{DD}/2 + 0.3)	V	—
	Three-speed Ethernet signals	LV_{IN} TV_{IN}	GND to (LV_{DD}+ 0.3) GND to (TV_{DD}+ 0.3)	V	5
	DUART, Local Bus, DMA, Multiprocessor Interrupts, System Control & Clocking, Debug, Test, Power management, I^2C, JTAG and Miscellaneous I/O voltage	OV_{IN}	GND to (OV_{DD}+ 0.3)	V	5
Storage temperature range		T_{STG}	–55 to 150	°C	—

Notes:

1. Functional and tested operating conditions are given in Table 2. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. Core 1 characteristics apply only to MPC8641D. If two separate power supplies are used for V_{DD}_Core0 and V_{DD}_Core1, they must be kept within 100 mV of each other during normal run time.
3. The –0.3 to 2.75 V range is for DDR and –0.3 to 1.98 V range is for DDR2.
4. The 3.63V maximum is only supported when the port is configured in GMII, MII, RMII, or TBI modes; otherwise the 2.75V maximum applies. See Section 8.2, "FIFO, GMII, MII, TBI, RGMII, RMII, and RTBI AC Timing Specifications," for details on the recommended operating conditions per protocol.
5. During run time (M,L,T,O)V_{IN} and D*n*_MV_{REF} may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 2.

2.1.2 Recommended Operating Conditions

Table 2 provides the recommended operating conditions for the MPC8641. Note that the values in Table 2 are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed. For details on order information and specific operating conditions for parts, see Section 21, "Ordering Information."

Table 2. Recommended Operating Conditions

Characteristic	Symbol	Recommended Value	Unit	Notes
Cores supply voltages	V_{DD}_Core0, V_{DD}_Core1	1.10 ± 50 mV	V	1, 2, 8
		1.05 ± 50 mV		1, 2, 7
		0.95 ± 50 mV		1, 2, 12
Cores PLL supply	AV_{DD}_Core0, AV_{DD}_Core1	1.10 ± 50 mV	V	8, 13
		1.05 ± 50 mV		7, 13
		0.95 ± 50 mV		12, 13
SerDes Transceiver Supply (Ports 1 and 2)	SV_{DD}	1.10 ± 50 mV	V	8, 11
		1.05 ± 50 mV		7, 11

should meet the MPC8641 input cycle-to-cycle jitter requirement. Frequency modulation and spread are separate concerns, and the MPC8641 is compatible with spread spectrum sources if the recommendations listed in Table 9 are observed.

Table 9. Spread Spectrum Clock Source Recommendations

At recommended operating conditions. See Table 2.

Parameter	Min	Max	Unit	Notes
Frequency modulation	—	50	kHz	1
Frequency spread	—	1.0	%	1, 2

Notes:
1. Guaranteed by design.
2. SYSCLK frequencies resulting from frequency spreading, and the resulting core and VCO frequencies, must meet the minimum and maximum specifications given in Table 8.

It is imperative to note that the processor's minimum and maximum SYSCLK, core, and VCO frequencies must not be exceeded regardless of the type of clock source. Therefore, systems in which the processor is operated at its maximum rated e600 core frequency should avoid violating the stated limits by using down-spreading only.

SD*n*_REF_CLK and $\overline{\text{SD}n\text{\_REF\_CLK}}$ was designed to work with a spread spectrum clock (+0 to 0.5% spreading at 30–33kHz rate is allowed), assuming both ends have same reference clock. For better results use a source without significant unintended modulation.

4.2 Real Time Clock Timing

The RTC input is sampled by the platform clock (MPX clock). The output of the sampling latch is then used as an input to the counters of the PIC. There is no jitter specification. The minimum pulse width of the RTC signal should be greater than 2x the period of the MPX clock. That is, minimum clock high time is $2 \times t_{MPX}$, and minimum clock low time is $2 \times t_{MPX}$. There is no minimum RTC frequency; RTC may be grounded if not needed.

4.3 eTSEC Gigabit Reference Clock Timing

Table 10 provides the eTSEC gigabit reference clocks (EC1_GTX_CLK125 and EC2_GTX_CLK125) AC timing specifications for the MPC8641.

Table 10. EC*n*_GTX_CLK125 AC Timing Specifications

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
EC*n*_GTX_CLK125 frequency	f_{G125}	—	125 ±100 ppm	—	MHz	3
EC*n*_GTX_CLK125 cycle time	t_{G125}	—	8	—	ns	—
EC*n*_GTX_CLK125 peak-to-peak jitter	t_{G125J}	—	—	250	ps	1

6.2 DDR SDRAM AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR SDRAM interface.

6.2.1 DDR SDRAM Input AC Timing Specifications

Table 18 provides the input AC timing specifications for the DDR2 SDRAM when D*n*_GV_{DD}(typ)=1.8 V.

Table 18. DDR2 SDRAM Input AC Timing Specifications for 1.8-V Interface

At recommended operating conditions

Parameter	Symbol	Min	Max	Unit	Notes
AC input low voltage 400, 533 MHz 600 MHz	V_{IL}	—	 D*n*_MV_{REF} – 0.25 D*n*_MV_{REF} – 0.20	V	—
AC input high voltage 400, 533 MHz 600 MHz	V_{IH}	 D*n*_MV_{REF} + 0.25 D*n*_MV_{REF} + 0.20	—	V	—

Table 19 provides the input AC timing specifications for the DDR SDRAM when D*n*_GV_{DD}(typ)=2.5 V.

Table 19. DDR SDRAM Input AC Timing Specifications for 2.5-V Interface

At recommended operating conditions.

Parameter	Symbol	Min	Max	Unit	Notes
AC input low voltage	V_{IL}	—	D*n*_MV_{REF} – 0.31	V	—
AC input high voltage	V_{IH}	D*n*_MV_{REF} + 0.31	—	V	—

Table 20 provides the input AC timing specifications for the DDR SDRAM interface.

Table 20. DDR SDRAM Input AC Timing Specifications

At recommended operating conditions.

Parameter	Symbol	Min	Max	Unit	Notes
Controller Skew for MDQS—MDQ/MECC	t_{CISKEW}	—		ps	1, 2
600 MHz	—	–240	240	—	3
533 MHz	—	–300	300	—	3
400 MHz	—	–365	365	—	—

Note:

1. t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that will be captured with MDQS[n]. This should be subtracted from the total timing budget.
2. The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called t_{DISKEW}.This can be determined by the following equation: t_{DISKEW} =+/–(T/4 – abs(t_{CISKEW})) where T is the clock period and abs(t_{CISKEW}) is the absolute value of t_{CISKEW}.
3. Maximum DDR1 frequency is 400 MHz.

8.2.4.2 TBI Receive AC Timing Specifications

Table 33 provides the TBI receive AC timing specifications.

Table 33. TBI Receive AC Timing Specifications

At recommended operating conditions with L/TV_{DD} of 3.3 V ± 5% and 2.5 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
PMA_RX_CLK[0:1] clock period	t_{TRX}[3]	—	16.0	—	ns
PMA_RX_CLK[0:1] skew	t_{SKTRX}	7.5	—	8.5	ns
PMA_RX_CLK[0:1] duty cycle	t_{TRXH}/t_{TRX}	40	—	60	%
RCG[9:0] setup time to rising PMA_RX_CLK	t_{TRDVKH}	2.5	—	—	ns
RCG[9:0] hold time to rising PMA_RX_CLK	t_{TRDXKH}	1.5	—	—	ns
PMA_RX_CLK[0:1] clock rise time (20%-80%)	t_{TRXR}[2]	0.7	—	2.4	ns
PMA_RX_CLK[0:1] clock fall time (80%-20%)	t_{TRXF}[2]	0.7	—	2.4	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{TRDVKH} symbolizes TBI receive timing (TR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{TRX} clock reference (K) going to the high (H) state or setup time. Also, t_{TRDXKH} symbolizes TBI receive timing (TR) with respect to the time data input signals (D) went invalid (X) relative to the t_{TRX} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{TRX} represents the TBI (T) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall). For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (TRX).
2. Guaranteed by design.
3. ±100 ppm tolerance on PMA_RX_CLK[0:1] frequency

Figure 17 shows the TBI receive AC timing diagram.

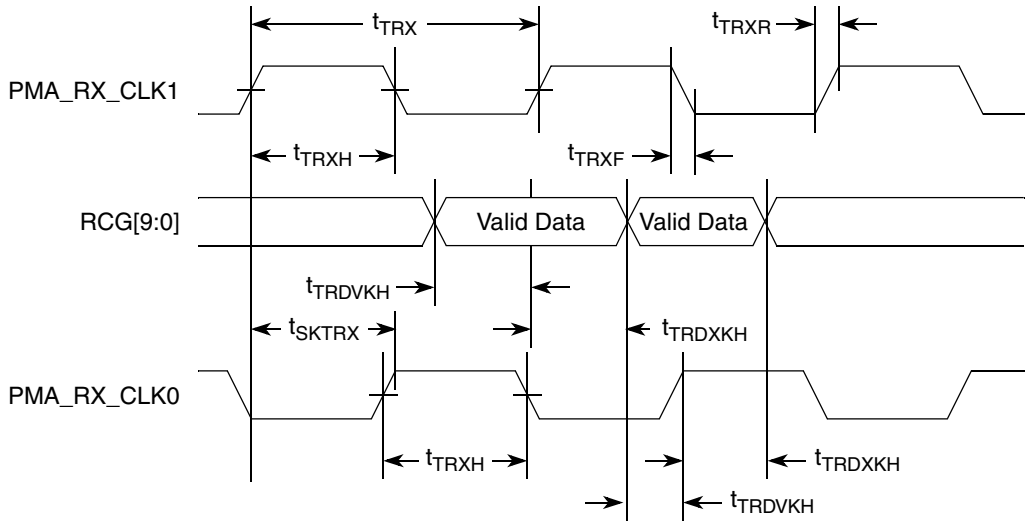


Figure 17. TBI Receive AC Timing Diagram

Table 35. RGMII and RTBI AC Timing Specifications (continued)

At recommended operating conditions with L/TV_{DD} of 2.5 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
Clock period duration [3]	t_{RGT}[5,6]	7.2	8.0	8.8	ns
Duty cycle for 10BASE-T and 100BASE-TX [3, 4]	t_{RGTH}/t_{RGT}[5]	40	50	60	%
Rise time (20%–80%)	t_{RGTR}[5]	—	—	0.75	ns
Fall time (80%–20%)	t_{RGTF}[5]	—	—	0.75	ns

Notes:

1. Note that, in general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII and RTBI timing. For example, the subscript of t_{RGT} represents the TBI (T) receive (RX) clock. Note also that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).
2. This implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 1.5 ns will be added to the associated clock signal.
3. For 10 and 100 Mbps, t_{RGT} scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned between.
5. Guaranteed by characterization
6. ±100 ppm tolerance on RX_CLK frequency

Figure 19 shows the RGMII and RTBI AC timing and multiplexing diagrams.

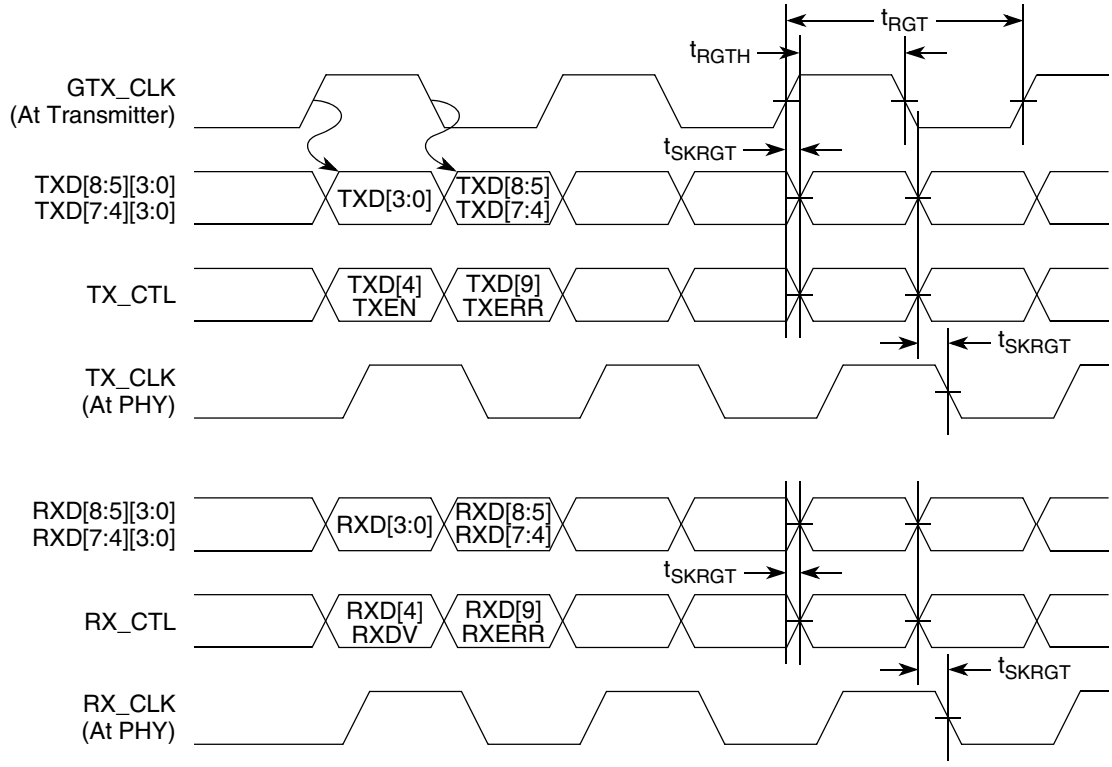


Figure 19. RGMII and RTBI AC Timing and Multiplexing Diagrams

Figure 34 provides the $\overline{\text{TRST}}$ timing diagram.

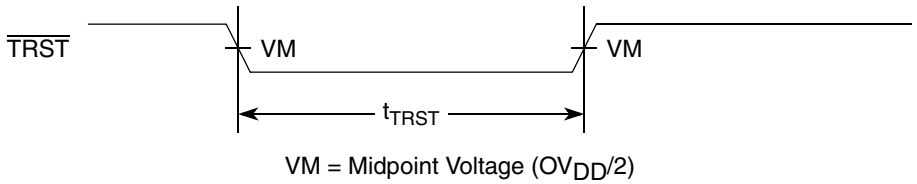


Figure 34. $\overline{\text{TRST}}$ Timing Diagram

Figure 35 provides the boundary-scan timing diagram.

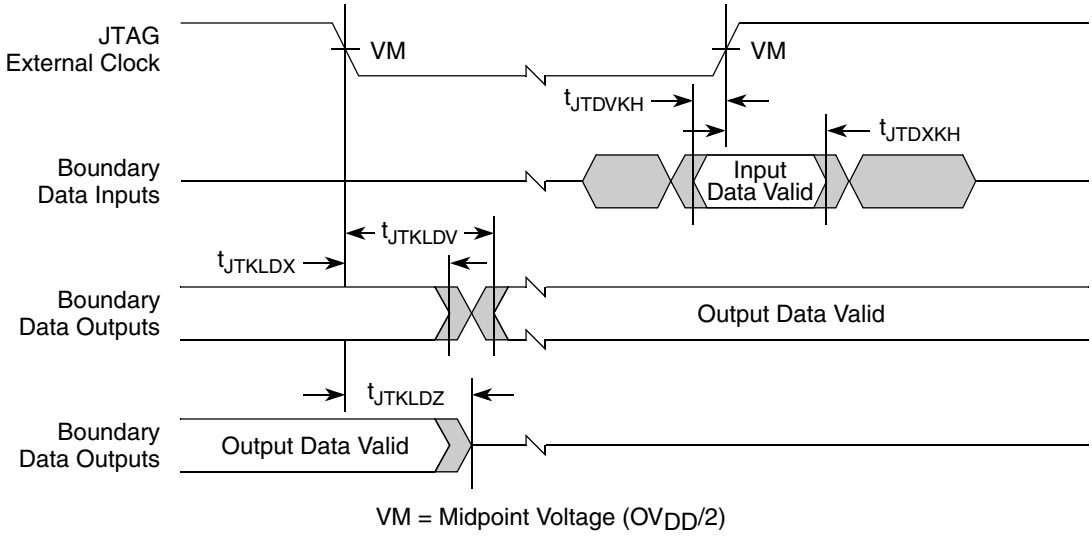


Figure 35. Boundary-Scan Timing Diagram

12 I²C

This section describes the DC and AC electrical characteristics for the I²C interfaces of the MPC8641.

12.1 I²C DC Electrical Characteristics

Table 45 provides the DC electrical characteristics for the I²C interfaces.

Table 45. I²C DC Electrical Characteristics

At recommended operating conditions with OV_{DD} of 3.3 V ± 5%.

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage level	V_{IH}	$0.7 \times OV_{DD}$	$OV_{DD} + 0.3$	V	—
Input low voltage level	V_{IL}	–0.3	$0.3 \times OV_{DD}$	V	—
Low level output voltage	V_{OL}	0	$0.2 \times OV_{DD}$	V	1
Pulse width of spikes which must be suppressed by the input filter	t_{I2KHKL}	0	50	ns	2
Input current each I/O pin (input voltage is between $0.1 \times OV_{DD}$ and $0.9 \times OV_{DD}$(max)	I_I	–10	10	μA	3

Figure 37 shows the AC timing diagram for the I^2C bus.

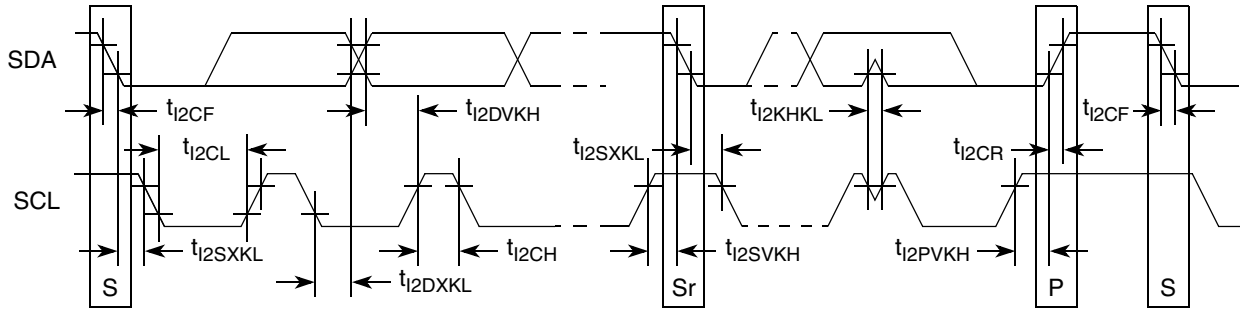


Figure 37. I^2C Bus AC Timing Diagram

13 High-Speed Serial Interfaces (HSSI)

The MPC8641D features two Serializer/Deserializer (SerDes) interfaces to be used for high-speed serial interconnect applications. The SerDes1 interface is dedicated for PCI Express data transfers. The SerDes2 can be used for PCI Express and/or Serial RapidIO data transfers.

This section describes the common portion of SerDes DC electrical specifications, which is the DC requirement for SerDes Reference Clocks. The SerDes data lane's transmitter and receiver reference circuits are also shown.

13.1 Signal Terms Definition

The SerDes utilizes differential signaling to transfer data across the serial link. This section defines terms used in the description and specification of differential signals.

Figure 38 shows how the signals are defined. For illustration purpose, only one SerDes lane is used for description. The figure shows waveform for either a transmitter output (SD*n*_TX and $\overline{\text{SD}n\text{\_TX}}$) or a receiver input (SD*n*_RX and $\overline{\text{SD}n\text{\_RX}}$). Each signal swings between A Volts and B Volts where A > B.

Using this waveform, the definitions are as follows. To simplify illustration, the following definitions assume that the SerDes transmitter and receiver operate in a fully symmetrical differential signaling environment.

1. **Single-Ended Swing**

   The transmitter output signals and the receiver input signals SD*n*_TX, $\overline{\text{SD}n\text{\_TX}}$, SD*n*_RX and $\overline{\text{SD}n\text{\_RX}}$ each have a peak-to-peak swing of A – B Volts. This is also referred as each signal wire's Single-Ended Swing.

2. **Differential Output Voltage, V_{OD}** (or **Differential Output Swing**):

   The Differential Output Voltage (or Swing) of the transmitter, V_{OD}, is defined as the difference of the two complimentary output voltages: $V_{SDn\_TX} - V_{\overline{SDn\_TX}}$. The V_{OD} value can be either positive or negative.

3. **Differential Input Voltage, V_{ID}** (or **Differential Input Swing**):

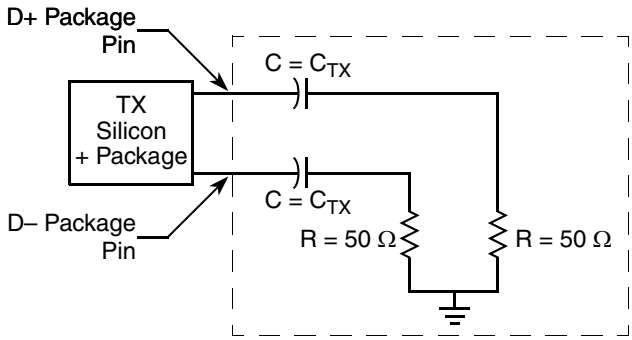


Figure 52. Compliance Test/Measurement Load

15 Serial RapidIO

This section describes the DC and AC electrical specifications for the RapidIO interface of the MPC8641, for the LP-Serial physical layer. The electrical specifications cover both single and multiple-lane links. Two transmitter types (short run and long run) on a single receiver are specified for each of three baud rates, 1.25, 2.50, and 3.125 GBaud.

Two transmitter specifications allow for solutions ranging from simple board-to-board interconnect to driving two connectors across a backplane. A single receiver specification is given that will accept signals from both the short run and long run transmitter specifications.

The short run transmitter specifications should be used mainly for chip-to-chip connections on either the same printed circuit board or across a single connector. This covers the case where connections are made to a mezzanine (daughter) card. The minimum swings of the short run specification reduce the overall power used by the transceivers.

The long run transmitter specifications use larger voltage swings that are capable of driving signals across backplanes. This allows a user to drive signals across two connectors and a backplane. The specifications allow a distance of at least 50 cm at all baud rates.

All unit intervals are specified with a tolerance of +/– 100 ppm. The worst case frequency difference between any transmit and receive clock will be 200 ppm.

To ensure interoperability between drivers and receivers of different vendors and technologies, AC coupling at the receiver input must be used.

15.1 DC Requirements for Serial RapidIO SD*n*_REF_CLK and SD*n*_REF_CLK

For more information, see Section 13.2, “SerDes Reference Clocks.”

15.2 AC Requirements for Serial RapidIO SD*n*_REF_CLK and SD*n*_REF_CLK

Table 51 lists AC requirements.

15.4 Equalization

With the use of high speed serial links, the interconnect media will cause degradation of the signal at the receiver. Effects such as Inter-Symbol Interference (ISI) or data dependent jitter are produced. This loss can be large enough to degrade the eye opening at the receiver beyond what is allowed in the specification. To negate a portion of these effects, equalization can be used. The most common equalization techniques that can be used are:

- A passive high pass filter network placed at the receiver. This is often referred to as passive equalization.
- The use of active circuits in the receiver. This is often referred to as adaptive equalization.

15.5 Explanatory Note on Transmitter and Receiver Specifications

AC electrical specifications are given for transmitter and receiver. Long run and short run interfaces at three baud rates (a total of six cases) are described.

The parameters for the AC electrical specifications are guided by the XAUI electrical interface specified in Clause 47 of IEEE 802.3ae-2002.

XAUI has similar application goals to serial RapidIO, as described in Section 8.1. The goal of this standard is that electrical designs for serial RapidIO can reuse electrical designs for XAUI, suitably modified for applications at the baud intervals and reaches described herein.

15.6 Transmitter Specifications

LP-Serial transmitter electrical and timing specifications are stated in the text and tables of this section.

The differential return loss, S11, of the transmitter in each case shall be better than

- –10 dB for (Baud Frequency)/10 < Freq(f) < 625 MHz, and
- –10 dB + 10log(f/625 MHz) dB for 625 MHz ≤ Freq(f) ≤ Baud Frequency

The reference impedance for the differential return loss measurements is 100 Ohm resistive. Differential return loss includes contributions from on-chip circuitry, chip packaging and any off-chip components related to the driver. The output impedance requirement applies to all valid output levels.

It is recommended that the 20%–80% rise/fall time of the transmitter, as measured at the transmitter output, in each case have a minimum value 60 ps.

It is recommended that the timing skew at the output of an LP-Serial transmitter between the two signals that comprise a differential pair not exceed 25 ps at 1.25 GB, 20 ps at 2.50 GB and 15 ps at 3.125 GB.

16 Package

This section details package parameters and dimensions.

16.1 Package Parameters for the MPC8641

The package parameters are as provided in the following list. The package type is 33 mm × 33 mm, 1023 pins. There are two package options: high-lead Flip Chip-Ceramic Ball Grid Array (FC-CBGA), and lead-free (FC-CBGA).

For all package types:

Die size	12.1 mm × 14.7 mm
Package outline	33 mm × 33 mm
Interconnects	1023
Pitch	1 mm
Total Capacitor count	43 caps; 100 nF each

For high-lead FC-CBGA (package option: HCTE[1] HX)

Maximum module height	2.97 mm
Minimum module height	2.47 mm
Solder Balls	89.5% Pb 10.5% Sn
Ball diameter (typical[2])	0.60 mm

For RoHS lead-free FC-CBGA (package option: HCTE[1] VU) and lead-free FC-CBGA (package option: HCTE[1] VJ)

Maximum module height	2.77 mm
Minimum module height	2.27 mm
Solder Balls	95.5% Sn 4.0% Ag 0.5% Cu
Ball diameter (typical[2])	0.60 mm

[1] High-coefficient of thermal expansion

[2] Typical ball diameter is before reflow

Table 63. MPC8641 Signal Reference by Functional Block (continued)

Name[1]	Package Pin Number	Pin Type	Power Supply	Notes
SD1_PLL_TPA	T28	Analog	SV_{DD}	13, 18
SD1_DLL_TPD	N28	O	SV_{DD}	13, 17
SD1_DLL_TPA	P31	Analog	SV_{DD}	13, 18
High Speed I/O Interface 2 (SERDES 2)[4]				
SD2_TX[0:3]	Y24, AA27, AB25, AC27	O	SV_{DD}	—
SD2_TX[4:7]	AE27, AG27, AJ27, AL27	O	SV_{DD}	34
$\overline{\text{SD2\_TX}}$[0:3]	Y25, AA28, AB26, AC28	O	SV_{DD}	—
$\overline{\text{SD2\_TX}}$[4:7]	AE28, AG28, AJ28, AL28	O	SV_{DD}	34
SD2_RX[0:3]	Y30, AA32, AB30, AC32	I	SV_{DD}	32
SD2_RX[4:7]	AH30, AJ32, AK30, AL32	I	SV_{DD}	32, 35
$\overline{\text{SD2\_RX}}$[0:3]	Y29, AA31, AB29, AC31	I	SV_{DD}	—
$\overline{\text{SD2\_RX}}$[4:7]	AH29, AJ31, AK29, AL31	I	SV_{DD}	35
SD2_REF_CLK	AE32	I	SV_{DD}	—
$\overline{\text{SD2\_REF\_CLK}}$	AE31	I	SV_{DD}	—
SD2_IMP_CAL_TX	AM29	Analog	SV_{DD}	19
SD2_IMP_CAL_RX	AA26	Analog	SV_{DD}	30
SD2_PLL_TPD	AF29	O	SV_{DD}	13, 17
SD2_PLL_TPA	AF31	Analog	SV_{DD}	13, 18
SD2_DLL_TPD	AD29	O	SV_{DD}	13, 17
SD2_DLL_TPA	AD30	Analog	SV_{DD}	13, 18
Special Connection Requirement pins				
No Connects	K24, K25, P28, P29, W26, W27, AD25, AD26	—	—	13
Reserved	H30, R32, V28, AG32	—	—	14
Reserved	H29, R31, W28, AG31	—	—	15
Reserved	AD24, AG26	—	—	16
Ethernet Miscellaneous Signals[5]				
EC1_GTX_CLK125	AL23	I	LV_{DD}	39
EC2_GTX_CLK125	AM23	I	TV_{DD}	39
EC_MDC	G31	O	OV_{DD}	—
EC_MDIO	G32	I/O	OV_{DD}	—
eTSEC Port 1 Signals[5]				

Table 63. MPC8641 Signal Reference by Functional Block (continued)

Name[1]	Package Pin Number	Pin Type	Power Supply	Notes
IRQ[9]/DMA_DREQ[3]	B30	I	OV_{DD}	10
IRQ[10]/DMA_DACK[3]	C30	I	OV_{DD}	9, 10
IRQ[11]/DMA_DDONE[3]	D30	I	OV_{DD}	9, 10
IRQ_OUT	J26	O	OV_{DD}	7, 11
DUART Signals[5]				
UART_SIN[0:1]	B32, C32	I	OV_{DD}	—
UART_SOUT[0:1]	D31, A32	O	OV_{DD}	—
UART_CTS[0:1]	A31, B31	I	OV_{DD}	—
UART_RTS[0:1]	C31, E30	O	OV_{DD}	—
I^2C Signals				
IIC1_SDA	A16	I/O	OV_{DD}	7, 11
IIC1_SCL	B17	I/O	OV_{DD}	7, 11
IIC2_SDA	A21	I/O	OV_{DD}	7, 11
IIC2_SCL	B21	I/O	OV_{DD}	7, 11
System Control Signals[5]				
HRESET	B18	I	OV_{DD}	—
HRESET_REQ	K18	O	OV_{DD}	—
SMI_0	L15	I	OV_{DD}	—
SMI_1	L16	I	OV_{DD}	12, *S4*
SRESET_0	C20	I	OV_{DD}	—
SRESET_1	C21	I	OV_{DD}	12, *S4*
CKSTP_IN	L18	I	OV_{DD}	—
CKSTP_OUT	L17	O	OV_{DD}	7, 11
READY/TRIG_OUT	J13	O	OV_{DD}	10, 25
Debug Signals[5]				
TRIG_IN	J14	I	OV_{DD}	—
TRIG_OUT/READY	J13	O	OV_{DD}	10, 25
D1_MSRCID[0:1]/ LB_SRCID[0:1]	F15, K15	O	OV_{DD}	6, 10
D1_MSRCID[2]/ LB_SRCID[2]	K14	O	OV_{DD}	10, 25
D1_MSRCID[3:4]/ LB_SRCID[3:4]	H15, G15	O	OV_{DD}	10
D2_MSRCID[0:4]	E16, C17, F16, H16, K16	O	OV_{DD}	—

Table 63. MPC8641 Signal Reference by Functional Block (continued)

Name[1]	Package Pin Number	Pin Type	Power Supply	Notes
$SENSEV_{SS}$_Core0	P14	Core0 GND sensing pin	—	31
$SENSEV_{SS}$_Core1	V20	Core1 GND sensing pin	—	12, 31, *S3*
$SENSEV_{DD}$_PLAT	N18	V_{DD}_PLAT sensing pin	—	28
$SENSEV_{SS}$_PLAT	P18	Platform GND sensing pin	—	29
$D1\_GV_{DD}$	B11, B14, D10, D13, F9, F12, H8, H11, H14, K10, K13, L8, P8, R6, U8, V6, W10, Y8, AA6, AB10, AC8, AD12, AE10, AF8, AG12, AH10, AJ8, AJ14, AK12, AL10, AL16	SDRAM 1 I/O supply	$D1\_GV_{DD}$ 2.5 - DDR 1.8 DDR2	—
$D2\_GV_{DD}$	B2, B5, B8, D4, D7, E2, F6, G4, H2, J6, K4, L2, M6, N4, P2, T4, U2, W4, Y2, AB4, AC2, AD6, AE4, AF2, AG6, AH4, AJ2, AK6, AL4, AM2	SDRAM 2 I/O supply	$D2\_GV_{DD}$ 2.5 V - DDR 1.8 V - DDR2	—
OV_{DD}	B22, B25, B28, D17, D24, D27, F19, F22, F26, F29, G17, H21, H24, K19, K23, M21, AM30	DUART, Local Bus, DMA, Multiprocessor Interrupts, System Control & Clocking, Debug, Test, JTAG, Power management, I^2C, JTAG and Miscellaneous I/O voltage	OV_{DD} 3.3 V	—
LV_{DD}	AC20, AD23, AH22	TSEC1 and TSEC2 I/O voltage	LV_{DD} 2.5/3.3 V	—
TV_{DD}	AC17, AG18, AK20	TSEC3 and TSEC4 I/O voltage	TV_{DD} 2.5/3.3 V	—
SV_{DD}	H31, J29, K28, K32, L30, M28, M31, N29, R30, T31, U29, V32, W30, Y31, AA29, AB32, AC30, AD31, AE29, AG30, AH31, AJ29, AK32, AL30, AM31	Transceiver Power Supply SerDes	SV_{DD} 1.05/1.1 V	—
XV_{DD}_SRDS1	K26, L24, M27, N25, P26, R24, R28, T27, U25, V26	Serial I/O Power Supply for SerDes Port 1	XV_{DD}_SRDS1 1.05/1.1 V	—

Table 63. MPC8641 Signal Reference by Functional Block (continued)

Name[1]	Package Pin Number	Pin Type	Power Supply	Notes
XV_{DD}_SRDS2	AA25, AB28, AC26, AD27, AE25, AF28, AH27, AK28, AM27, W24, Y27	Serial I/O Power Supply for SerDes Port 2	XV_{DD}_SRDS2 1.05/1.1 V	—
V_{DD}_Core0	L12, L13, L14, M13, M15, N12, N14, P11, P13, P15, R12, R14, T11, T13, T15, U12, U14, V11, V13, V15, W12, W14, Y12, Y13, Y15, AA12, AA14, AB13	Core 0 voltage supply	V_{DD}_Core0 0.95/1.05/1.1 V	—
V_{DD}_Core1	R16, R18, R20, T17, T19, T21, T23, U16, U18, U22, V17, V19, V21, V23, W16, W18, W20, W22, Y17, Y19, Y21, Y23, AA16, AA18, AA20, AA22, AB23, AC24	Core 1 voltage supply	V_{DD}_Core1 0.95/1.05/1.1 V	12, *S1*
V_{DD}_PLAT	M16, M17, M18, N16, N20, N22, P17, P19, P21, P23, R22	Platform supply voltage	V_{DD}_PLAT 1.05/1.1 V	—
AV_{DD}_Core0	B20	Core 0 PLL Supply	AV_{DD}_Core0 0.95/1.05/1.1 V	—
AV_{DD}_Core1	A19	Core 1 PLL Supply	AV_{DD}_Core1 0.95/1.05/1.1 V	12, *S2*
AV_{DD}_PLAT	B19	Platform PLL supply voltage	AV_{DD}_PLAT 1.05/1.1 V	—
AV_{DD}_LB	A20	Local Bus PLL supply voltage	AV_{DD}_LB 1.05/1.1 V	—
AV_{DD}_SRDS1	P32	SerDes Port 1 PLL & DLL Power Supply	AV_{DD}_SRDS1 1.05/1.1 V	—
AV_{DD}_SRDS2	AF32	SerDes Port 2 PLL & DLL Power Supply	AV_{DD}_SRDS2 1.05/1.1 V	—
GND	C3, C6, C9, C12, C15, C23, C26, E5, E8, E11, E14, E18, E25, E28, F3, G7, G10, G13, G20, G23, G27, G30, H5, J3, J9, J12, J15, J22, J25, K7, L5, L20, M3, M9, M12, N7, N11, N13, N15, N17, N19, N21, N23, P5, P12, P16, P20, P22, R3, R9, R11, R13, R15, R17, R19, R21, R23, T7, T12, T14, T16, T18, T20, T22, U5, U11,U13, U15, U17, U19, U21, U23, V3, V9, V12, V14, V16, V18, V22, W7, W11, W13, W15, W17, W19, W21, W23,Y5, Y14, Y16, Y18, Y20, Y22, AA3, AA9, AA13, AA15, AA17, AA19, AA21, AA23, AB7, AB24, AC5, AC11, AD3, AD9, AD15, AE7, AE13, AE18, AF5, AF11, AF21, AF24, AG3, AG9, AH7, AH13, AJ5, AJ11, AK3, AK9, AK15, AK19, AK23, AL7, AL13	GND	—	—

Table 63. MPC8641 Signal Reference by Functional Block (continued)

Name[1]	Package Pin Number	Pin Type	Power Supply	Notes

37.This pin is only an output in FIFO mode when used as Rx Flow Control.

38.This pin functions as cfg_dram_type[0 or 1] at reset and MUST BE VALID BEFORE HRESET ASSERTION in device sleep mode.

39. Should be pulled to ground if unused (such as in FIFO, MII and RMII modes).

40. See Section 18.4.2, “Platform to FIFO Restrictions” for clock speed limitations for this pin when used in FIFO mode.

41. The phase between the output clocks TSEC1_GTX_CLK and TSEC2_GTX_CLK (ports 1 and 2) is no more than 100 ps. The phase between the output clocks TSEC3_GTX_CLK and TSEC4_GTX_CLK (ports 3 and 4) is no more than 100 ps.

42. For systems which boot from Local Bus (GPCM)-controlled flash, a pullup on LGPL4 is required.

Special Notes for Single Core Device:

S1. Solder ball for this signal will not be populated in the single core package.

S2. The PLL filter from V_{DD}_Core1 to AV_{DD}_Core1 should be removed. AV_{DD}_Core1 should be pulled to ground with a weak (2–10 kΩ) resistor. See Section 20.2.1, “PLL Power Supply Filtering” for more details.

S3. This pin should be pulled to GND for the single core device.

S4. No special requirement for this pin on single core device. Pin should be tied to power supply as directed for dual core.

18 Clocking

This section describes the PLL configuration of the MPC8641. Note that the platform clock is identical to the MPX clock.

18.1 Clock Ranges

Table 64 provides the clocking specifications for the processor cores and Table 65 provides the clocking specifications for the memory bus. Table 66 provides the clocking for the Platform/MPX bus and Table 67 provides the clocking for the Local bus.

Table 64. Processor Core Clocking Specifications

Characteristic	Maximum Processor Core Frequency								Unit	Notes
	1000 MHz		1250MHz		1333MHz		1500 MHz			
	Min	Max	Min	Max	Min	Max	Min	Max		
e600 core processor frequency	800	1000	800	1250	800	1333	800	1500	MHz	1, 2

Notes:

1. **Caution:** The MPX clock to SYSCLK ratio and e600 core to MPX clock ratio settings must be chosen such that the resulting SYSCLK frequency, e600 (core) frequency, and MPX clock frequency do not exceed their respective maximum or minimum operating frequencies. Refer to Section 18.2, “MPX to SYSCLK PLL Ratio,” and Section 18.3, “e600 to MPX clock PLL Ratio,” for ratio settings.
2. The minimum e600 core frequency is based on the minimum platform clock frequency of 400 MHz.

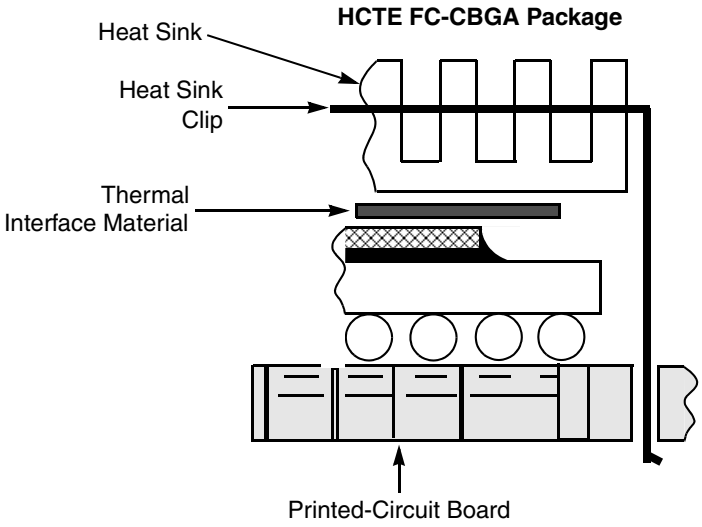


Figure 59. FC-CBGA Package Exploded Cross-Sectional View with Several Heat Sink Options

There are several commercially-available heat sinks for the MPC8641 provided by the following vendors:

Aavid Thermalloy 80 Commercial St. Concord, NH 03301 Internet: www.aavidthermalloy.com	603-224-9988
Advanced Thermal Solutions 89 Access Road #27. Norwood, MA02062 Internet: www.qats.com	781-769-2800
Alpha Novatech 473 Sapena Ct. #12 Santa Clara, CA 95054 Internet: www.alphanovatech.com	408-749-7601
Calgreg Thermal Solutions 60 Alhambra Road, Suite 1 Warwick, RI 02886 Internet: www.calgreg.com	888-732-6100
International Electronic Research Corporation (IERC) 413 North Moss St. Burbank, CA 91502 Internet: www.ctscorp.com	818-842-7277
Millennium Electronics (MEI) Loroco Sites 671 East Brokaw Road San Jose, CA 95112 Internet: www.mei-thermal.com	408-436-8770

example, assuming a T_i of 30°C, a T_r of 5°C, a package $R_{\theta JC}$ = 0.1, and a typical power consumption (P_d) of 43.4 W, the following expression for T_j is obtained:

Die-junction temperature: $T_j = 30°C + 5°C + (0.1°C/W + 0.2°C/W + \theta_{sa}) \times 43.4\ W$

For this example, a $R_{\theta sa}$ value of 1.32 °C/W or less is required to maintain the die junction temperature below the maximum value of Table 2.

Though the die junction-to-ambient and the heat sink-to-ambient thermal resistances are a common figure-of-merit used for comparing the thermal performance of various microelectronic packaging technologies, one should exercise caution when only using this metric in determining thermal management because no single parameter can adequately describe three-dimensional heat flow. The final die-junction operating temperature is not only a function of the component-level thermal resistance, but the system-level design and its operating conditions. In addition to the component's power consumption, a number of factors affect the final operating die-junction temperature—airflow, board population (local heat flux of adjacent components), heat sink efficiency, heat sink placement, next-level interconnect technology, system air temperature rise, altitude, and so on.

Due to the complexity and variety of system-level boundary conditions for today's microelectronic equipment, the combined effects of the heat transfer mechanisms (radiation, convection, and conduction) may vary widely. For these reasons, we recommend using conjugate heat transfer models for the board as well as system-level designs.

For system thermal modeling, the MPC8641 thermal model is shown in Figure 62. Four cuboids are used to represent this device. The die is modeled as 12.4x15.3 mm at a thickness of 0.86 mm. See Section 3, "Power Characteristics" for power dissipation details. The substrate is modeled as a single block 33x33x1.2 mm with orthotropic conductivity: 13.5 W/(m • K) in the xy-plane and 5.3 W/(m • K) in the z-direction. The die is centered on the substrate. The bump/underfill layer is modeled as a collapsed thermal resistance between the die and substrate with a conductivity of 5.3 W/(m • K) in the thickness dimension of 0.07 mm. Because the bump/underfill is modeled with zero physical dimension (collapsed height), the die thickness was slightly enlarged to provide the correct height. The C5 solder layer is modeled as a cuboid with dimensions 33x33x0.4 mm and orthotropic thermal conductivity of 0.034 W/(m • K) in the xy-plane and 9.6 W/(m • K) in the z-direction. An LGA solder layer would be modeled as a collapsed thermal resistance with thermal conductivity of 9.6W/(m • K) and an effective height of 0.1 mm. The thermal model uses approximate dimensions to reduce grid. Please refer to the case outline for actual dimensions.

Local Bus - If parity is not used, tie LDP[0:3] to ground via a 4.7 kΩ resistor, tie LPBSE to OV_{DD} via a 4.7 kΩ resistor (pull-up resistor). For systems which boot from Local Bus (GPCM)-controlled flash, a pullup on LGPL4 is required.

SerDes - Receiver lanes configured for PCI Express are allowed to be disconnected (as would occur when a PCI Express slot is connected but not populated). Directions for terminating the SerDes signals is discussed in Section 20.5.1, "Guidelines for High-Speed Interface Termination."

20.5.1 Guidelines for High-Speed Interface Termination

20.5.1.1 SerDes Interface

The high-speed SerDes interface can be disabled through the POR input cfg_io_ports[0:3] and through the DEVDISR register in software. If a SerDes port is disabled through the POR input the user can not enable it through the DEVDISR register in software. However, if a SerDes port is enabled through the POR input the user can disable it through the DEVDISR register in software. Disabling a SerDes port through software should be done on a temporary basis. Power is always required for the SerDes interface, even if the port is disabled through either mechanism. Table 72 describes the possible enabled/disabled scenarios for a SerDes port. The termination recommendations must be followed for each port.

Table 72. SerDes Port Enabled/Disabled Configurations

	Disabled through POR input	Enabled through POR input
Enabled through DEVDISR	SerDes port is disabled (and cannot be enabled through DEVDISR) Complete termination required (Reference Clock not required)	SerDes port is enabled Partial termination may be required[1] (Reference Clock is required)
Disabled through DEVDISR	SerDes port is disabled (through POR input) Complete termination required (Reference Clock not required)	SerDes port is disabled after software disables port Same termination requirements as when the port is enabled through POR input[2] (Reference Clock is required)

Notes:

1 Partial Termination when a SerDes port is enabled through both POR input and DEVDISR is determined by the SerDes port mode. If the port is in x8 PCI Express mode, no termination is required because all pins are being used. If the port is in x1/x2/x4 PCI Express mode, termination is required on the unused pins. If the port is in x4 Serial RapidIO mode termination is required on the unused pins.

2 If a SerDes port is enabled through the POR input and then disabled through DEVDISR, no hardware changes are required. Termination of the SerDes port should follow what is required when the port is enabled through both POR input and DEVDISR. See Note 1 for more information.

If the high-speed SerDes port requires complete or partial termination, the unused pins should be terminated as described in this section.

The following pins must be left unconnected (floating):

- SD*n*_TX[7:0]
- $\overline{\text{SD}n\text{\_TX}}$[7:0]

21 Ordering Information

Ordering information for the parts fully covered by this specification document is provided in Section 21.1, "Part Numbers Fully Addressed by This Document."

21.1 Part Numbers Fully Addressed by This Document

Table 74 provides the Freescale part numbering nomenclature for the MPC8641. Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Freescale sales office. In addition to the processor frequency, the part numbering scheme also includes an application modifier which may specify special application conditions. Each part number also contains a revision code which refers to the die mask revision number.

Table 74. Part Numbering Nomenclature

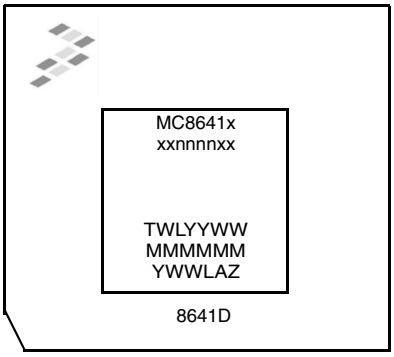
MC	nnnn	x	xx	nnnn	x	x
Product Code	**Part Identifier**	**Core Count**	**Package [1]**	**Core Processor Frequency [2] (MHz)**	**DDR speed (MHz)**	**Product Revision Level**
MC	8641	Blank = Single Core D = Dual Core	HX = High-lead HCTE FC-CBGA VU = RoHS lead-free HCTE FC-CBGA[5] VJ = lead-free HCTE FC-CBGA[6]	1000, 1250, 1333, 1500	N = 500 MHz[4] K = 600 MHz J = 533 MHz H = 500 MHz G = 400 MHz	Revision B = 2.0 System Version Register Value for Rev B: 0x8090_0020 - MPC8641 0x8090_0120 - MPC8641D Revision C = 2.1 System Version Register Value for Rev C: 0x8090_0021 - MPC8641 0x8090_0121 - MPC8641D Revision E = 3.0 System Version Register Value for Rev E: 0x8090_0030 - MPC8641 0x8090_0130 - MPC8641D

Notes:

1. See Section 16, "Package," for more information on available package types.
2. Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by part number specifications may support other maximum core frequencies.
3. The P prefix in a Freescale part number designates a "Pilot Production Prototype" as defined by Freescale SOP 3-13. These parts have only preliminary reliability and characterization data. Before pilot production prototypes may be shipped, written authorization from the customer must be on file in the applicable sales office acknowledging the qualification status and the fact that product changes may still occur while shipping pilot production prototypes.
4. Part Number MC8641xxx1000NX is our low V_{DD}_Core*n* device. V_{DD}_Core*n* = 0.95 V and V_{DD}_PLAT = 1.05 V.
5. VU part number is RoHS compliant with the permitted exception of the C4 die bumps.
6. VJ part number is entirely lead-free including the C4 die bumps.

21.2 Part Marking

Parts are marked as the example shown in Figure 70.



NOTE:
TWLYYWW is the test code
MMMMMM is the M00 (mask) number.
YWWLAZ is the assembly traceability code.

Figure 70. Part Marking for FC-CBGA Device

22 Document Revision History

Table 76 provides a revision history for the MPC8641D hardware specification.

Table 76. Document Revision History

Revision	Date	Substantive Change(s)
3	05/2014	• Updated the Serial RapidIO equation in Section 4.4, “Platform Frequency Requirements for PCI-Express and Serial RapidIO” • Updated Section 19.2.4, “Temperature Diode,” by removing the ideality factor value. • Added VJ package type designator and footnotes to Table 74, “Part Numbering Nomenclature” and Section 16.1, “Package Parameters for the MPC8641.”
2	07/2009	• Added note 8 to Table 49, “Differential Transmitter (TX) Output Specifications.” • Added Revision E to Table 74, “Part Numbering Nomenclature.”
1	11/2008	• Added Section 4.4, “Platform Frequency Requirements for PCI-Express and Serial RapidIO.” • Removed the statement “Note that core processor speed of 1500 MHz is only available for the MPC8641D (dual core)” from Note 2 in Table 74 because a 1500 MHz core is offered for both MPC8641D (dual core) and MPC8641 (single core). • Added Note 8 to Figure 57 and Figure 58.
0	07/2008	• Initial Release