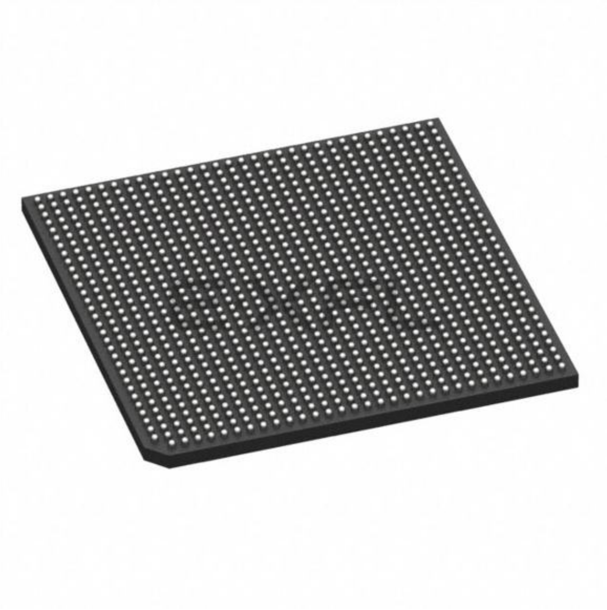

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e600
Number of Cores/Bus Width	2 Core, 32-Bit
Speed	1.0GHz
Co-Processors/DSP	-
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (4)
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	1023-BCBGA, FCCBGA
Supplier Device Package	1023-FCCBGA (33x33)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc8641dvu1000gb

1.1 Key Features

The following lists an overview of the MPC8641 key feature set:

- Major features of the e600 core are as follows:
  - High-performance, 32-bit superscalar microprocessor that implements the PowerPC ISA
  - Eleven independent execution units and three register files
    - Branch processing unit (BPU)
    - Four integer units (IUs) that share 32 GPRs for integer operands
    - 64-bit floating-point unit (FPU)
    - Four vector units and a 32-entry vector register file (VRs)
    - Three-stage load/store unit (LSU)
  - Three issue queues, FIQ, VIQ, and GIQ, can accept as many as one, two, and three instructions, respectively, in a cycle.
  - Rename buffers
  - Dispatch unit
  - Completion unit
  - Two separate 32-Kbyte instruction and data level 1 (L1) caches
  - Integrated 1-Mbyte, eight-way set-associative unified instruction and data level 2 (L2) cache with ECC
  - 36-bit real addressing
  - Separate memory management units (MMUs) for instructions and data
  - Multiprocessing support features
  - Power and thermal management
  - Performance monitor
  - In-system testability and debugging features
  - Reliability and serviceability
- MPX coherency module (MCM)
  - Ten local address windows plus two default windows
  - Optional low memory offset mode for core 1 to allow for address disambiguation
- Address translation and mapping units (ATMUs)
  - Eight local access windows define mapping within local 36-bit address space
  - Inbound and outbound ATMUs map to larger external address spaces
  - Three inbound windows plus a configuration window on PCI Express
  - Four inbound windows plus a default window on serial RapidIO
  - Four outbound windows plus default translation for PCI Express
  - Eight outbound windows plus default translation for serial RapidIO with segmentation and sub-segmentation support

- DDR memory controllers
  - Dual 64-bit memory controllers (72-bit with ECC)
  - Support of up to a 300-MHz clock rate and a 600-MHz DDR2 SDRAM
  - Support for DDR, DDR2 SDRAM
  - Up to 16 Gbytes per memory controller
  - Cache line and page interleaving between memory controllers.
- Serial RapidIO interface unit
  - Supports *RapidIO Interconnect Specification*, Revision 1.2
  - Both 1x and 4x LP-Serial link interfaces
  - Transmission rates of 1.25-, 2.5-, and 3.125-Gbaud (data rates of 1.0-, 2.0-, and 2.5-Gbps) per lane
  - RapidIO–compliant message unit
  - RapidIO atomic transactions to the memory controller
- PCI Express interface
  - PCI Express 1.0a compatible
  - Supports x1, x2, x4, and x8 link widths
  - 2.5 Gbaud, 2.0 Gbps lane
- Four enhanced three-speed Ethernet controllers (eTSECs)
  - Three-speed support (10/100/1000 Mbps)
  - Four IEEE 802.3, 802.3u, 802.3x, 802.3z, 802.3ac, 802.3ab-compatible controllers
  - Support of the following physical interfaces: MII, RMII, GMII, RGMII, TBI, and RTBI
  - Support a full-duplex FIFO mode for high-efficiency ASIC connectivity
  - TCP/IP off-load
  - Header parsing
  - Quality of service support
  - VLAN insertion and deletion
  - MAC address recognition
  - Buffer descriptors are backward compatible with PowerQUICC II and PowerQUICC III programming models
  - RMON statistics support
  - MII management interface for control and status
- Programmable interrupt controller (PIC)
  - Programming model is compliant with the OpenPIC architecture
  - Supports 16 programmable interrupt and processor task priority levels
  - Supports 12 discrete external interrupts and 48 internal interrupts
  - Eight global high resolution timers/counters that can generate interrupts
  - Allows processors to interrupt each other with 32b messages

- Support for PCI-Express message-shared interrupts (MSIs)
- Local bus controller (LBC)
  - Multiplexed 32-bit address and data operating at up to 133 MHz
  - Eight chip selects support eight external slaves
- Integrated DMA controller
  - Four-channel controller
  - All channels accessible by both the local and the remote masters
  - Supports transfers to or from any local memory or I/O port
  - Ability to start and flow control each DMA channel from external 3-pin interface
- Device performance monitor
  - Supports eight 32-bit counters that count the occurrence of selected events
  - Ability to count up to 512 counter-specific events
  - Supports 64 reference events that can be counted on any of the 8 counters
  - Supports duration and quantity threshold counting
  - Burstiness feature that permits counting of burst events with a programmable time between bursts
  - Triggering and chaining capability
  - Ability to generate an interrupt on overflow
- Dual I^2C controllers
  - Two-wire interface
  - Multiple master support
  - Master or slave I^2C mode support
  - On-chip digital filtering rejects spikes on the bus
- Boot sequencer
  - Optionally loads configuration data from serial ROM at reset via the I^2C interface
  - Can be used to initialize configuration registers and/or memory
  - Supports extended I^2C addressing mode
  - Data integrity checked with preamble signature and CRC
- DUART
  - Two 4-wire interfaces (SIN, SOUT, $\overline{\text{RTS}}$, $\overline{\text{CTS}}$)
  - Programming model compatible with the original 16450 UART and the PC16550D
- IEEE 1149.1-compatible, JTAG boundary scan
- Available as 1023 pin Hi-CTE flip chip ceramic ball grid array (FC-CBGA)

NOTE

There is no required order sequence between the individual rails for this item (# 1). However, V_{DD}_PLAT, AV_{DD}_PLAT rails must reach 90% of their recommended value before the rail for Dn_GV_{DD}, and Dn_MV_{REF} (in next step) reaches 10% of their recommended value. AV_{DD} type supplies must be delayed with respect to their source supplies by the RC time constant of the PLL filter circuit described in Section 20.2.1, "PLL Power Supply Filtering."

2. D*n*_GV_{DD}, D*n*_MV_{REF}

NOTE

It is possible to leave the related power supply (D*n*_GV_{DD}, D*n*_MV_{REF}) turned off at reset for a DDR port that will not be used. Note that these power supplies can only be powered up again at reset for functionality to occur on the DDR port.

3. SYSCLK

The recommended order of power down is as follows:

1. D*n*_GV_{DD}, D*n*_MV_{REF}
2. All power rails other than DDR I/O (D*n*_GV_{DD}, D*n*_MV_{REF}).

NOTE

SYSCLK may be powered down simultaneous to either of item # 1 or # 2 in the power down sequence. Beyond this, the power supplies may power down simultaneously if the preservation of DDR*n* memory is not a concern.

See Figure 3 for more details on the Power and Reset Sequencing details.

The maximum power dissipation for individual power supplies of the MPC8641D is shown in Table 5.

Table 5. MPC8641D Individual Supply Maximum Power Dissipation [1]

Component Description	Supply Voltage (Volts)	Power (Watts)	Notes
Per Core voltage Supply	V_{DD}_Core0/V_{DD}_Core1 = 1.1 V @ 1500 MHz	21.00	
Per Core PLL voltage supply	AV_{DD}_Core0/AV_{DD}_Core1 = 1.1 V @ 1500 MHz	0.0125	
Per Core voltage Supply	V_{DD}_Core0/V_{DD}_Core1 = 1.05 V @ 1333 MHz	17.00	
Per Core PLL voltage supply	AV_{DD}_Core0/AV_{DD}_Core1 = 1.05 V @ 1333 MHz	0.0125	
Per Core voltage Supply	V_{DD}_Core0/V_{DD}_Core1 = 0.95 V @ 1000 MHz	11.50	5
Per Core PLL voltage supply	AV_{DD}_Core0/AV_{DD}_Core1 = 0.95 V @ 1000 MHz	0.0125	5
DDR Controller I/O voltage supply	D*n*_GV_{DD} = 2.5 V @ 400 MHz	0.80	2
	D*n*_GV_{DD} = 1.8 V @ 533 MHz	0.68	2
	D*n*_GV_{DD} = 1.8 V @ 600 MHz	0.77	2
16-bit FIFO @ 200 MHz eTsec 1&2/3&4 Voltage Supply	L/TV_{DD} = 3.3 V	0.11	2, 3
non-FIFO eTsec*n* Voltage Supply	L/TV_{DD} = 3.3 V	0.08	2
x8 SerDes transceiver Supply	SV_{DD} = 1.1 V	0.70	2
x8 SerDes I/O Supply	XV_{DD}_SRDS*n* = 1.1 V	0.66	2
SerDes PLL voltage supply Port 1 or 2	AV_{DD}_SRDS1/AV_{DD}_SRDS2 = 1.1 V	0.10	
Platform I/O Supply	OV_{DD} = 3.3 V	0.45	4
Platform source Supply	V_{DD}_PLAT = 1.1 V @ 600 MHz	12.00	
Platform source Supply	V_{DD}_PLAT = 1.05 Vn @ 500 MHz	9.80	5
Platform source Supply	V_{DD}_PLAT = 1.05 Vn @ 400 MHz	7.70	
Platform, Local Bus PLL voltage Supply	AV_{DD}_PLAT, AV_{DD}_LB = 1.1 V	0.0125	

Notes:
1. This is a maximum power supply number which is provided for power supply and board design information. The numbers are based on 100% bus utilization for each component. The components listed are not expected to have 100% bus usage simultaneously for all components. Actual numbers may vary based on activity.
2. Number is based on a per port/interface value.
3. This is based on one eTSEC port used. Since 16-bit FIFO mode involves two ports, the number will need to be multiplied by two for the total. The other eTSEC protocols dissipate less than this number per port. Note that the power needs to be multiplied by the number of ports used for the protocol for the total eTSEC port power dissipation.
4. This includes Local Bus, DUART, I^2C, DMA, Multiprocessor Interrupts, System Control & Clocking, Debug, Test, Power management, JTAG and Miscellaneous I/O voltage.
5. These power numbers are for Part Number MC8641xxx1000NX only. V_{DD}_Core*n* = 0.95 V and V_{DD}_PLAT = 1.05 V.

The power dissipation for the MPC8641 single core device is shown in Table 6.

Table 6. MPC8641 Power Dissipation (Single Core)

Power Mode	Core Frequency (MHz)	Platform Frequency (MHz)	V_{DD}_Coren, V_{DD}_PLAT (Volts)	Junction Temperature	Power (Watts)	Notes
Typical	1500 MHz	600 MHz	1.1 V	65 °C	20.3	1, 2
Thermal				105 °C	25.2	1, 3
Maxim					28.9	1, 4
Typical	1333 MHz	533 MHz	1.05 V	65 °C	16.3	1, 2
Thermal				105 °C	20.2	1, 3
Maximum					23.2	1, 4
Typical	1250 MHz	500 MHz	1.05 V	65 °C	16.3	1, 2
Thermal				105 °C	20.2	1, 3
Maximum					23.2	1, 4
Typical	1000 MHz	400 MHz	1.05 V	65 °C	16.3	1, 2
Thermal				105 °C	20.2	1, 3
Maximum					23.2	1, 4
Typical	1000 MHz	500 MHz	0.95 V, 1.05 V	65 °C	11.6	1, 2, 5
Thermal				105 °C	14.4	1, 3, 5
Maximum					16.5	1, 4, 5

Notes:

1. These values specify the power consumption at nominal voltage and apply to all valid processor bus frequencies and configurations. The values do not include power dissipation for I/O supplies.
2. Typical power is an average value measured at the nominal recommended core voltage (V_{DD}_Core*n*) and 65°C junction temperature (see Table 2)while running the Dhrystone 2.1 benchmark and achieving 2.3 Dhrystone MIPs/MHz.
3. Thermal power is the average power measured at nominal core voltage (V_{DD}_Core*n*) and maximum operating junction temperature (see Table 2) while running the Dhrystone 2.1 benchmark and achieving 2.3 Dhrystone MIPs/MHz and a typical workload on platform interfaces.
4. Maximum power is the maximum power measured at nominal core voltage (V_{DD}_Core*n*) and maximum operating junction temperature (see Table 2) while running a test which includes an entirely L1-cache-resident, contrived sequence of instructions which keep all the execution units maximally busy.
5. These power numbers are for Part Number MC8641xx1000NX only. V_{DD}_Core*n* = 0.95 V and V_{DD}_PLAT = 1.05 V.

Table 24. GMII, MII, RMII, TBI and FIFO DC Electrical Characteristics (continued)

Parameter	Symbol	Min	Max	Unit	Notes
Input low current (V_{IN} = GND)	I_{IL}	–600	—	μA	3

Notes:

[1] LV_{DD} supports eTSECs 1 and 2.
[2] TV_{DD} supports eTSECs 3 and 4.
[3] The symbol V_{IN}, in this case, represents the LV_{IN} and TV_{IN} symbols referenced in Table 1 and Table 2.

Table 25. GMII, RGMII, RTBI, TBI and FIFO DC Electrical Characteristics

Parameters	Symbol	Min	Max	Unit	Notes
Supply voltage 2.5 V	LV_{DD}/TV_{DD}	2.375	2.625	V	1,2
Output high voltage (LV_{DD}/TV_{DD} = Min, I_{OH} = –1.0 mA)	V_{OH}	2.00	—	V	—
Output low voltage (LV_{DD}/TV_{DD} = Min, I_{OL} = 1.0 mA)	V_{OL}	—	0.40	V	—
Input high voltage	V_{IH}	1.70	—	V	—
Input low voltage	V_{IL}	—	0.90	V	—
Input high current ($V_{IN} = LV_{DD}$, $V_{IN} = TV_{DD}$)	I_{IH}	—	10	μA	1, 2,3
Input low current (V_{IN} = GND)	I_{IL}	–15	—	μA	3

Note:

[1] LV_{DD} supports eTSECs 1 and 2.
[2] TV_{DD} supports eTSECs 3 and 4.
[3] Note that the symbol V_{IN}, in this case, represents the LV_{IN} and TV_{IN} symbols referenced in Table 1 and Table 2.

8.2 FIFO, GMII, MII, TBI, RGMII, RMII, and RTBI AC Timing Specifications

The AC timing specifications for FIFO, GMII, MII, TBI, RGMII, RMII and RTBI are presented in this section.

8.2.1 FIFO AC Specifications

The basis for the AC specifications for the eTSEC's FIFO modes is the double data rate RGMII and RTBI specifications, since they have similar performance and are described in a source-synchronous fashion like FIFO modes. However, the FIFO interface provides deliberate skew between the transmitted data and source clock in GMII fashion.

When the eTSEC is configured for FIFO modes, all clocks are supplied from external sources to the relevant eTSEC interface. That is, the transmit clock must be applied to the eTSEC*n*'s TSEC*n*_TX_CLK, while the receive clock must be applied to pin TSEC*n*_RX_CLK. The eTSEC internally uses the transmit

Table 29. GMII Receive AC Timing Specifications (continued)

At recommended operating conditions with L/TV_{DD} of 3.3 V ± 5% and 2.5 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
RX_CLK clock fall time (80%-20%)	t_{GRXF}[2]	—	—	1.0	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)\ (reference)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, t_{GRDVKH} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{RX} clock reference (K) going to the high state (H) or setup time. Also, t_{GRDXKL} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{GRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{GRX} represents the GMII (G) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Guaranteed by design.
3. ±100 ppm tolerance on RX_CLK frequency

Figure 11 provides the AC test load for eTSEC.

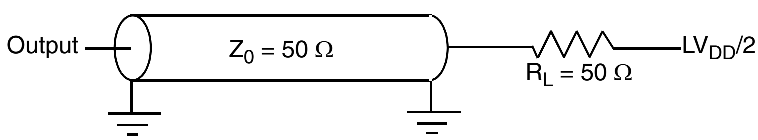


Figure 11. eTSEC AC Test Load

Figure 12 shows the GMII receive AC timing diagram.

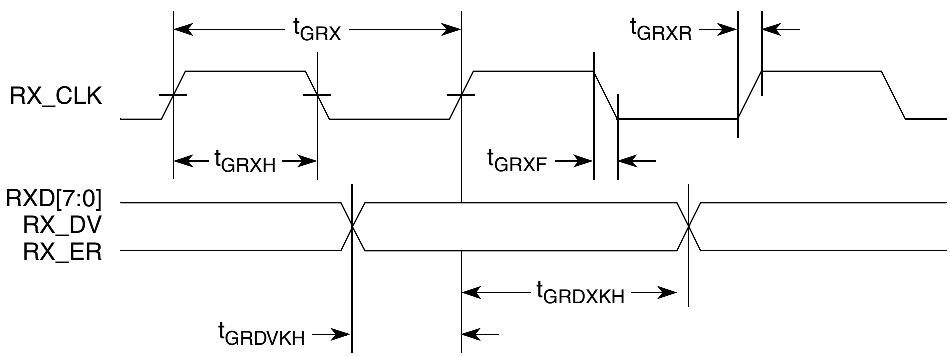


Figure 12. GMII Receive AC Timing Diagram

Table 35. RGMII and RTBI AC Timing Specifications (continued)

At recommended operating conditions with L/TV_{DD} of 2.5 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
Clock period duration [3]	t_{RGT}[5,6]	7.2	8.0	8.8	ns
Duty cycle for 10BASE-T and 100BASE-TX [3, 4]	t_{RGTH}/t_{RGT}[5]	40	50	60	%
Rise time (20%–80%)	t_{RGTR}[5]	—	—	0.75	ns
Fall time (80%–20%)	t_{RGTF}[5]	—	—	0.75	ns

Notes:

1. Note that, in general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII and RTBI timing. For example, the subscript of t_{RGT} represents the TBI (T) receive (RX) clock. Note also that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).
2. This implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 1.5 ns will be added to the associated clock signal.
3. For 10 and 100 Mbps, t_{RGT} scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned between.
5. Guaranteed by characterization
6. ±100 ppm tolerance on RX_CLK frequency

Figure 19 shows the RGMII and RTBI AC timing and multiplexing diagrams.

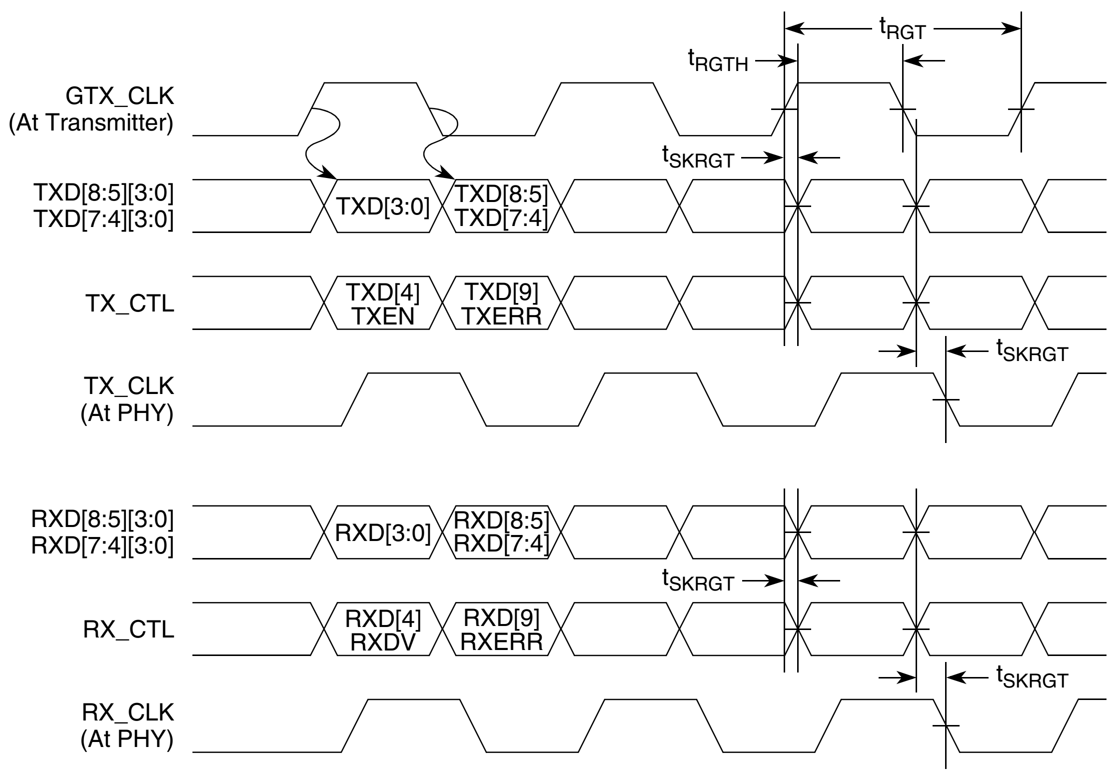


Figure 19. RGMII and RTBI AC Timing and Multiplexing Diagrams

9 Ethernet Management Interface Electrical Characteristics

The electrical characteristics specified here apply to MII management interface signals MDIO (management data input/output) and MDC (management data clock). The electrical characteristics for GMII, RGMII, RMII, TBI and RTBI are specified in "Section 8, "Ethernet: Enhanced Three-Speed Ethernet (eTSEC), MII Management."

9.1 MII Management DC Electrical Characteristics

The MDC and MDIO are defined to operate at a supply voltage of 3.3 V. The DC electrical characteristics for MDIO and MDC are provided in Table 38.

Table 38. MII Management DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
Supply voltage (3.3 V)	OV_{DD}	3.135	3.465	V
Output high voltage (OV_{DD} = Min, I_{OH} = –1.0 mA)	V_{OH}	2.10	—	V
Output low voltage (OV_{DD} =Min, I_{OL} = 1.0 mA)	V_{OL}	—	0.50	V
Input high voltage	V_{IH}	1.70	—	V
Input low voltage	V_{IL}	—	0.90	V
Input high current (OV_{DD} = Max, V_{IN} [1] = 2.1 V)	I_{IH}	—	40	μA
Input low current (OV_{DD} = Max, V_{IN} = 0.5 V)	I_{IL}	–600	—	μA

Note:
1. Note that the symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

9.2 MII Management AC Electrical Specifications

Table 39 provides the MII management AC timing specifications.

Table 39. MII Management AC Timing Specifications

At recommended operating conditions with OV_{DD} is 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit	Notes
MDC frequency	f_{MDC}	2.5	—	9.3	MHz	2, 4
MDC period	t_{MDC}	80	—	400	ns	—
MDC clock pulse width high	t_{MDCH}	32	—	—	ns	—
MDC to MDIO valid	t_{MDKHDV}	16*t_{MPXCLK}	—	—	ns	5
MDC to MDIO delay	t_{MDKHDX}	10	—	16*t_{MPXCLK}	ns	3, 5
MDIO to MDC setup time	t_{MDDVKH}	5	—	—	ns	—

— The SD*n*_REF_CLK input average voltage must be between 200 and 400 mV. Figure 42 shows the SerDes reference clock input requirement for single-ended signaling mode.

— To meet the input amplitude requirement, the reference clock inputs might need to be DC or AC-coupled externally. For the best noise performance, the reference of the clock could be DC or AC-coupled into the unused phase ($\overline{\text{SD}n\text{\_REF\_CLK}}$) through the same source impedance as the clock input (SD*n*_REF_CLK) in use.

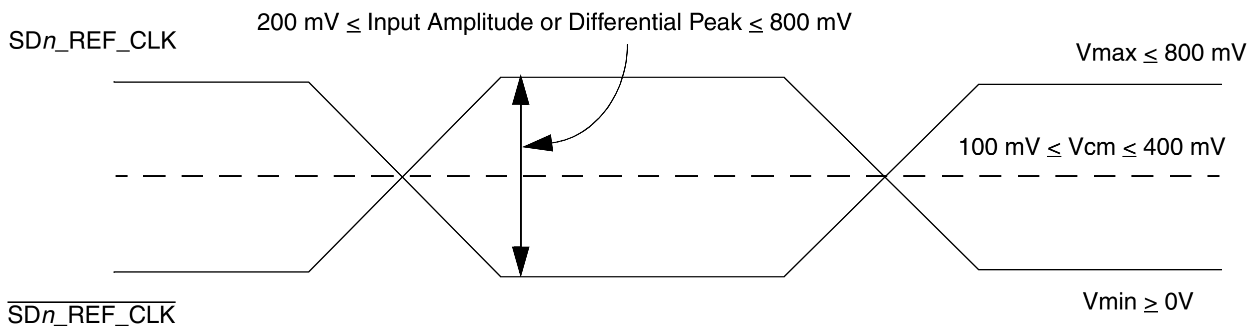


Figure 40. Differential Reference Clock Input DC Requirements (External DC-Coupled)

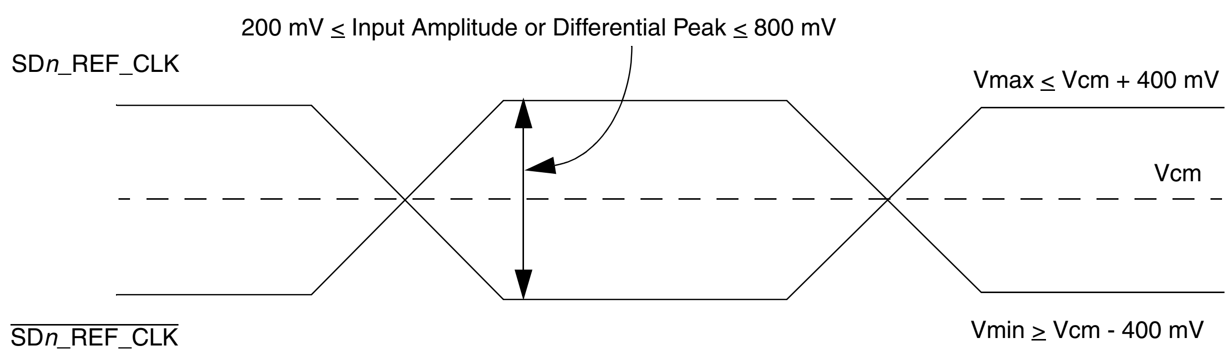


Figure 41. Differential Reference Clock Input DC Requirements (External AC-Coupled)

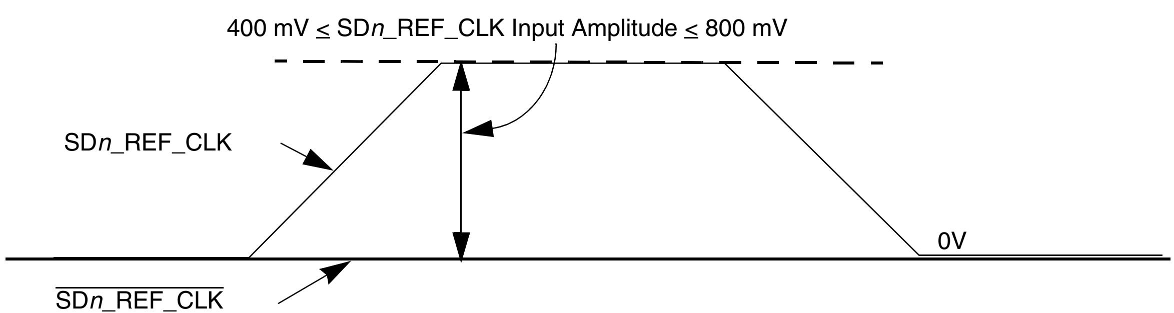


Figure 42. Single-Ended Reference Clock Input DC Requirements

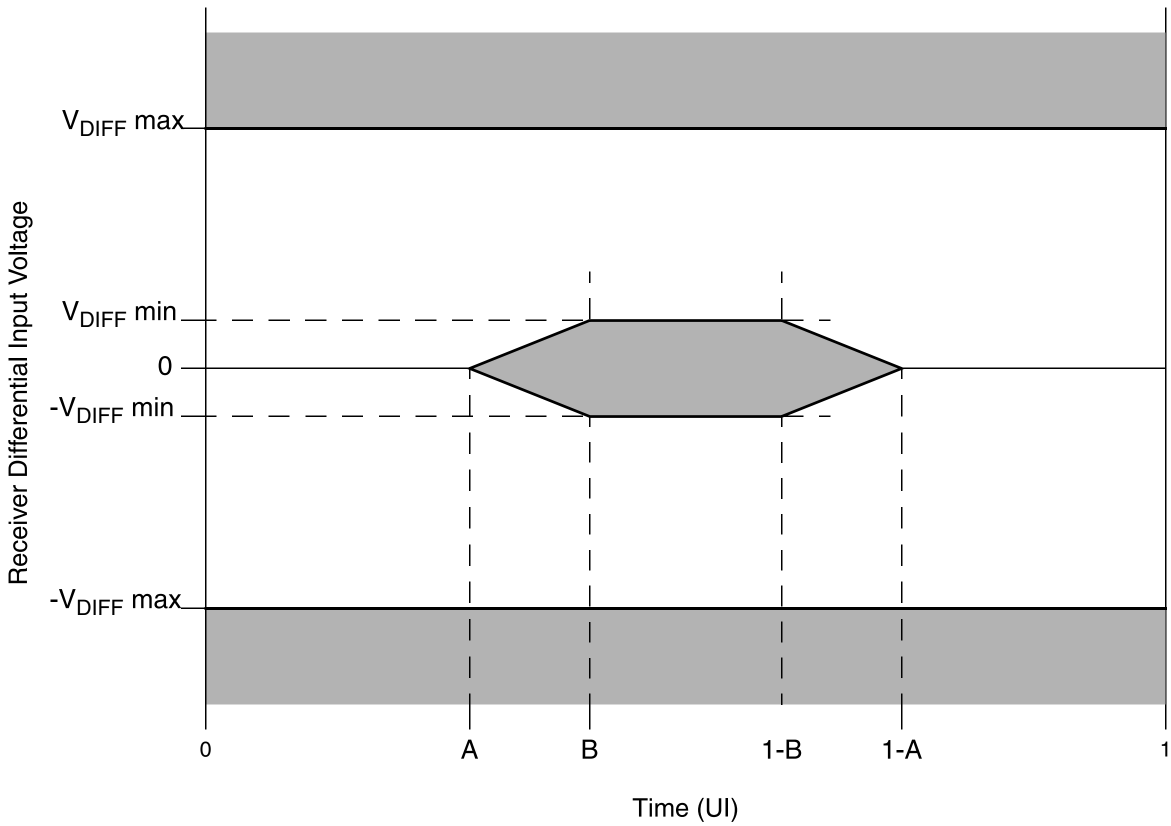


Figure 56. Receiver Input Compliance Mask

Table 62. Receiver Input Compliance Mask Parameters Exclusive of Sinusoidal Jitter

Receiver Type	V_{DIFF}min (mV)	V_{DIFF}max (mV)	A (UI)	B (UI)
1.25 GBaud	100	800	0.275	0.400
2.5 GBaud	100	800	0.275	0.400
3.125 GBaud	100	800	0.275	0.400

15.9 Measurement and Test Requirements

Since the LP-Serial electrical specification are guided by the XAUI electrical interface specified in Clause 47 of IEEE 802.3ae-2002, the measurement and test requirements defined here are similarly guided by Clause 47. In addition, the CJPAT test pattern defined in Annex 48A of IEEE 802.3ae-2002 is specified as the test pattern for use in eye pattern and jitter measurements. Annex 48B of IEEE 802.3ae-2002 is recommended as a reference for additional information on jitter test methods.

15.9.1 Eye Template Measurements

For the purpose of eye template measurements, the effects of a single-pole high pass filter with a 3 dB point at (Baud Frequency)/1667 is applied to the jitter. The data pattern for template measurements is the

Table 63. MPC8641 Signal Reference by Functional Block (continued)

Name[1]	Package Pin Number	Pin Type	Power Supply	Notes
$\overline{\text{LCS}}$[6]/DMA_DACK[2]	E23	O	OV_{DD}	7, 10
$\overline{\text{LCS}}$[7]/$\overline{\text{DMA\_DDONE}}$[2]	F23	O	OV_{DD}	7, 10
$\overline{\text{LWE}}$[0:3]/ LSDDQM[0:3]/ $\overline{\text{LBS}}$[0:3]	E21, F21, D22, E20	O	OV_{DD}	6
LBCTL	D21	O	OV_{DD}	—
LALE	E19	O	OV_{DD}	—
LGPL0/LSDA10	F20	O	OV_{DD}	25
LGPL1/$\overline{\text{LSDWE}}$	H20	O	OV_{DD}	25
LGPL2/$\overline{\text{LOE}}$/ $\overline{\text{LSDRAS}}$	J20	O	OV_{DD}	—
LGPL3/$\overline{\text{LSDCAS}}$	K20	O	OV_{DD}	6
LGPL4/$\overline{\text{LGTA}}$/ LUPWAIT/LPBSE	L21	I/O	OV_{DD}	42
LGPL5	J19	O	OV_{DD}	6
LCKE	H19	O	OV_{DD}	—
LCLK[0:2]	G19, L19, M20	O	OV_{DD}	—
LSYNC_IN	M19	I	OV_{DD}	—
LSYNC_OUT	D20	O	OV_{DD}	—
DMA Signals[5]				
$\overline{\text{DMA\_DREQ}}$[0:1]	E31, E32	I	OV_{DD}	—
$\overline{\text{DMA\_DREQ}}$[2]/$\overline{\text{LCS}}$[5]	B23	I	OV_{DD}	9, 10
$\overline{\text{DMA\_DREQ}}$[3]/IRQ[9]	B30	I	OV_{DD}	10
$\overline{\text{DMA\_DACK}}$[0:1]	D32, F30	O	OV_{DD}	—
$\overline{\text{DMA\_DACK}}$[2]/$\overline{\text{LCS}}$[6]	E23	O	OV_{DD}	10
$\overline{\text{DMA\_DACK}}$[3]/IRQ[10]	C30	O	OV_{DD}	9, 10
$\overline{\text{DMA\_DDONE}}$[0:1]	F31, F32	O	OV_{DD}	—
$\overline{\text{DMA\_DDONE}}$[2]/$\overline{\text{LCS}}$[7]	F23	O	OV_{DD}	10
$\overline{\text{DMA\_DDONE}}$[3]/IRQ[11]	D30	O	OV_{DD}	9, 10
Programmable Interrupt Controller Signals[5]				
$\overline{\text{MCP\_0}}$	F17	I	OV_{DD}	—
$\overline{\text{MCP \_1}}$	H17	I	OV_{DD}	12, *S4*
IRQ[0:8]	G28, G29, H27, J23, M23, J27, F28, J24, L23	I	OV_{DD}	—

Table 63. MPC8641 Signal Reference by Functional Block (continued)

Name[1]	Package Pin Number	Pin Type	Power Supply	Notes
D1_MDVAL/LB_DVAL	J16	O	OV_{DD}	10
D2_MDVAL	D19	O	OV_{DD}	—
Power Management Signals[5]				
ASLEEP	C19	O	OV_{DD}	—
System Clocking Signals[5]				
SYSCLK	G16	I	OV_{DD}	—
RTC	K17	I	OV_{DD}	32
CLK_OUT	B16	O	OV_{DD}	23
Test Signals[5]				
$\overline{\text{LSSD\_MODE}}$	C18	I	OV_{DD}	26
TEST_MODE[0:3]	C16, E17, D18, D16	I	OV_{DD}	26
JTAG Signals[5]				
TCK	H18	I	OV_{DD}	—
TDI	J18	I	OV_{DD}	24
TDO	G18	O	OV_{DD}	23
TMS	F18	I	OV_{DD}	24
$\overline{\text{TRST}}$	A17	I	OV_{DD}	24
Miscellaneous[5]				
Spare	J17	—	—	13
GPOUT[0:7]/ TSEC1_TXD[0:7]	AF25, AC23, AG24, AG23, AE24, AE23, AE22, AD22	O	OV_{DD}	6, 10
GPIN[0:7]/ TSEC1_RXD[0:7]	AL25, AL24, AK26, AK25, AM26, AF26, AH24, AG25	I	OV_{DD}	10
GPOUT[8:15]/ TSEC2_TXD[0:7]	AB20, AJ23, AJ22, AD19, AH23, AH21, AG22, AG21	O	OV_{DD}	10
GPIN[8:15]/ TSEC2_RXD[0:7]	AL22, AK22, AM21, AH20, AG20, AF20, AF23, AF22	I	OV_{DD}	10
Additional Analog Signals				
TEMP_ANODE	AA11	Thermal	—	—
TEMP_CATHODE	Y11	Thermal	—	—
Sense, Power and GND Signals				
SENSEV_{DD}_Core0	M14	V_{DD}_Core0 sensing pin	—	31
SENSEV_{DD}_Core1	U20	V_{DD}_Core1 sensing pin	—	12,31, *S1*

Table 63. MPC8641 Signal Reference by Functional Block (continued)

Name[1]	Package Pin Number	Pin Type	Power Supply	Notes
AGND_SRDS1	P30	SerDes Port 1 Ground pin for AV_{DD}_SRDS1	—	—
AGND_SRDS2	AF30	SerDes Port 2 Ground pin for AV_{DD}_SRDS2	—	—
SGND	H28, H32, J30, K31, L28, L29, M32, N30, R29, T32, U30, V31, W29,Y32 AA30, AB31, AC29, AD32, AE30, AG29, AH32, AJ30, AK31, AL29, AM32	Ground pins for SV_{DD}	—	—
XGND	K27, L25, M26, N24, P27, R25, T26, U24, V27, W25, Y28, AA24, AB27, AC25, AD28, AE26, AF27, AH28, AJ26, AK27, AL26, AM28	Ground pins for XV_{DD}_SRDS*n*	—	—
Reset Configuration Signals[20]				
TSEC1_TXD[0] / cfg_alt_boot_vec	AF25	—	LV_{DD}	—
TSEC1_TXD[1]/ cfg_platform_freq	AC23	—	LV_{DD}	21
TSEC1_TXD[2:4]/ cfg_device_id[5:7]	AG24, AG23, AE24	—	LV_{DD}	—
TSEC1_TXD[5]/ cfg_tsec1_reduce	AE23	—	LV_{DD}	—
TSEC1_TXD[6:7]/ cfg_tsec1_prtcl[0:1]	AE22, AD22	—	LV_{DD}	—
TSEC2_TXD[0:3]/ cfg_rom_loc[0:3]	AB20, AJ23, AJ22, AD19	—	LV_{DD}	—
TSEC2_TXD[4], TSEC2_TX_ER/ cfg_dram_type[0:1]	AH23, AB19	—	LV_{DD}	38
TSEC2_TXD[5]/ cfg_tsec2_reduce	AH21	—	LV_{DD}	—
TSEC2_TXD[6:7]/ cfg_tsec2_prtcl[0:1]	AG22, AG21	—	LV_{DD}	—
TSEC3_TXD[0:1]/ cfg_spare[0:1]	AL21, AJ21	O	TV_{DD}	33
TSEC3_TXD[2]/ cfg_core1_enable	AM20	O	TV_{DD}	—
TSEC3_TXD[3]/ cfg_core1_lm_offset	AJ20	—	LV_{DD}	—
TSEC3_TXD[5]/ cfg_tsec3_reduce	AK21	—	LV_{DD}	—

18.4.1 SYSCLK to Platform Frequency Options

Table 70 shows some SYSCLK frequencies and the expected MPX frequency values based on the MPX clock to SYSCLK ratio. Note that frequencies between 400 MHz and 500 MHz are NOT supported on the platform. See note regarding *cfg_platform_freq* in Section 17, "Signal Listings," because it is a reset configuration pin that is related to platform frequency.

Table 70. Frequency Options of SYSCLK with Respect to Platform/MPX Clock Speed

MPX to SYSCLK Ratio	SYSCLK (MHz)					
	66	83	100	111	133	167
	Platform/MPX Frequency (MHz)[1]					
2						
3					400	500
4			400		533	
5			500	555		
6	400	500	600			
8	533					
9	600					

[1] SYSCLK frequency range is 66-167 MHz. Platform clock/ MPX frequency range is 400 MHz, 500-600 MHz.

18.4.2 Platform to FIFO Restrictions

Please note the following FIFO maximum speed restrictions based on platform speed.

For FIFO GMII mode:

FIFO TX/RX clock frequency <= platform clock frequency/4.2

For example, if the platform frequency is 533 MHz, the FIFO TX/RX clock frequency should be no more than 127 MHz

For FIFO encoded mode:

FIFO TX/RX clock frequency <= platform clock frequency/3.2

For example, if the platform frequency is 533 MHz, the FIFO TX/RX clock frequency should be no more than 167 MHz

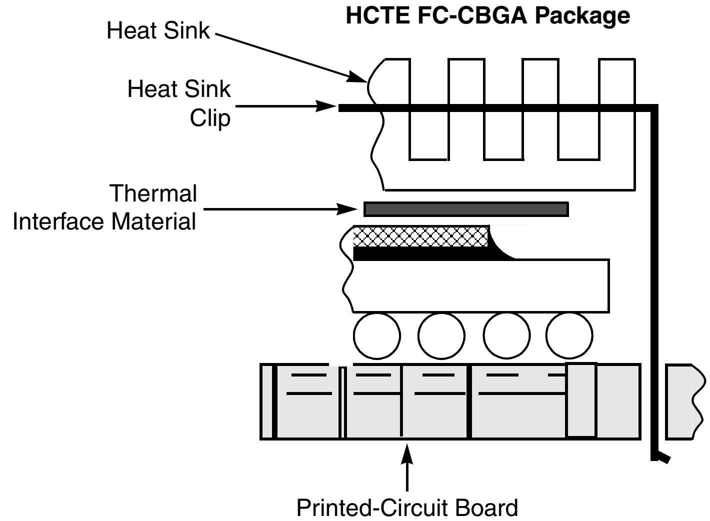


Figure 59. FC-CBGA Package Exploded Cross-Sectional View with Several Heat Sink Options

There are several commercially-available heat sinks for the MPC8641 provided by the following vendors:

Aavid Thermalloy 80 Commercial St. Concord, NH 03301 Internet: www.aavidthermalloy.com	603-224-9988
Advanced Thermal Solutions 89 Access Road #27. Norwood, MA02062 Internet: www.qats.com	781-769-2800
Alpha Novatech 473 Sapena Ct. #12 Santa Clara, CA 95054 Internet: www.alphanovatech.com	408-749-7601
Calgreg Thermal Solutions 60 Alhambra Road, Suite 1 Warwick, RI 02886 Internet: www.calgreg.com	888-732-6100
International Electronic Research Corporation (IERC) 413 North Moss St. Burbank, CA 91502 Internet: www.ctscorp.com	818-842-7277
Millennium Electronics (MEI) Loroco Sites 671 East Brokaw Road San Jose, CA 95112 Internet: www.mei-thermal.com	408-436-8770

The following pins must be connected to GND:

- SD*n*_RX[7:0]
- $\overline{\text{SD}n\text{\_RX}}$[7:0]
- SD*n*_REF_CLK
- $\overline{\text{SD}n\text{\_REF\_CLK}}$

NOTE

It is recommended to power down the unused lane through SRDS1CR1[0:7] register (offset = 0xE_0F08) and SRDS2CR1[0:7] register (offset = 0xE_0F44.) (This prevents the oscillations and holds the receiver output in a fixed state.) that maps to SERDES lane 0 to lane 7 accordingly.

For other directions on reserved or no-connects pins see Section 17, "Signal Listings."

20.6 Pull-Up and Pull-Down Resistor Requirements

The MPC8641 requires weak pull-up resistors (2–10 kΩ is recommended) on all open drain type pins.

The following pins must NOT be pulled down during power-on reset: TSEC4_TXD[4], LGPL0/LSDA10, LGPL1/$\overline{\text{LSDWE}}$, TRIG_OUT/READY, and D1_MSRCID[2].

The following are factory test pins and require strong pull up resistors (100 Ω –1 kΩ) to OVDD

LSSD_MODE, TEST_MODE[0:3].The following pins require weak pull up resistors (2–10 kΩ) to their specific power supplies: LCS[0:4], LCS[5]/DMA_DREQ2, LCS[6]/DMA_DACK[2], LCS[7]/DMA_DDONE[2], IRQ_OUT, IIC1_SDA, IIC1_SCL, IIC2_SDA, IIC2_SCL, and CKSTP_OUT.

The following pins should be pulled to ground with a 100-Ω resistor: SD1_IMP_CAL_TX, SD2_IMP_CAL_TX. The following pins should be pulled to ground with a 200-Ω resistor: SD1_IMP_CAL_RX, SD2_IMP_CAL_RX.

TSEC*n*_TX_EN signals require an external 4.7-kΩ pull down resistor to prevent PHY from seeing a valid Transmit Enable before it is actively driven.

When the platform frequency is 400 MHz, TSEC1_TXD[1] must be pulled down at reset.

TSEC2_TXD[4] and TSEC2_TX_ER pins function as cfg_dram_type[0 or 1] at reset and MUST BE VALID BEFORE HRESET ASSERTION when coming out of device sleep mode.

20.6.1 Special instructions for Single Core device

The mechanical drawing for the single core device does not have all the solder balls that exist on the single core device. This includes all the balls for VDD_Core1 and $\text{SENSEV}_{\text{DD}}$_Core1 which exist on the package for the dual core device, but not on the single core package. A solder ball is present for $\text{SENSEV}_{\text{SS}}$_Core1 and needs to be connected to ground with a weak (2-10 kΩ) pull down resistor. Likewise, AV_{DD}_Core1 needs to be pulled to ground as shown in Figure 64.

The mechanical drawing for the single core device is located in Section 16.2, "Mechanical Dimensions of the MPC8641 FC-CBGA."

The COP interface has a standard header, shown in Figure 67, for connection to the target system, and is based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

The COP header adds many benefits such as breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features. An inexpensive option can be to leave the COP header unpopulated until needed.

There is no standardized way to number the COP header shown in Figure 67; consequently, many different pin numbers have been observed from emulator vendors. Some are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom, while still others number the pins counter clockwise from pin 1 (as with an IC). Regardless of the numbering, the signal placement recommended in Figure 67 is common to all known emulators.

For a multi-processor non-daisy chain configuration, Figure 68, can be duplicated for each processor. The recommended daisy chain configuration is shown in Figure 69. Please consult with your tool vendor to determine which configuration is supported by their emulator.

20.9.1 Termination of Unused Signals

If the JTAG interface and COP header will not be used, Freescale recommends the following connections:

- $\overline{\text{TRST}}$ should be tied to $\overline{\text{HRESET}}$ through a 0 kΩ isolation resistor so that it is asserted when the system reset signal ($\overline{\text{HRESET}}$) is asserted, ensuring that the JTAG scan chain is initialized during the power-on reset flow. Freescale recommends that the COP header be designed into the system as shown in Figure 68. If this is not possible, the isolation resistor will allow future access to $\overline{\text{TRST}}$ in case a JTAG interface may need to be wired onto the system in future debug situations.
- Tie TCK to OV_{DD} through a 10 kΩ resistor. This will prevent TCK from changing state and reading incorrect data into the device.
- No connection is required for TDI, TMS, or TDO.

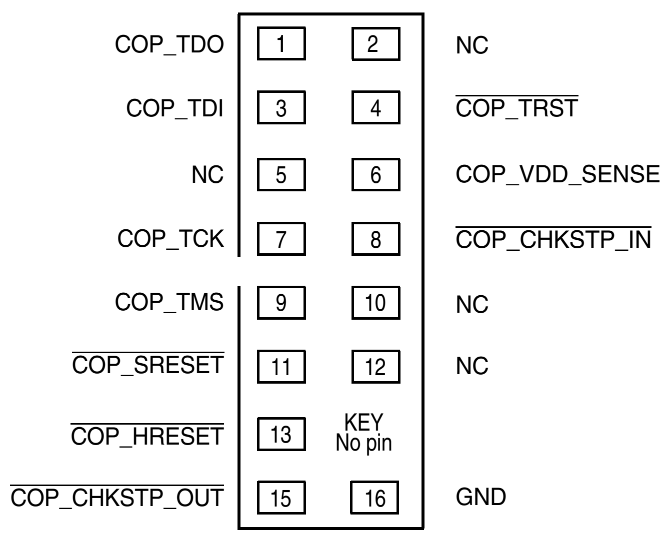
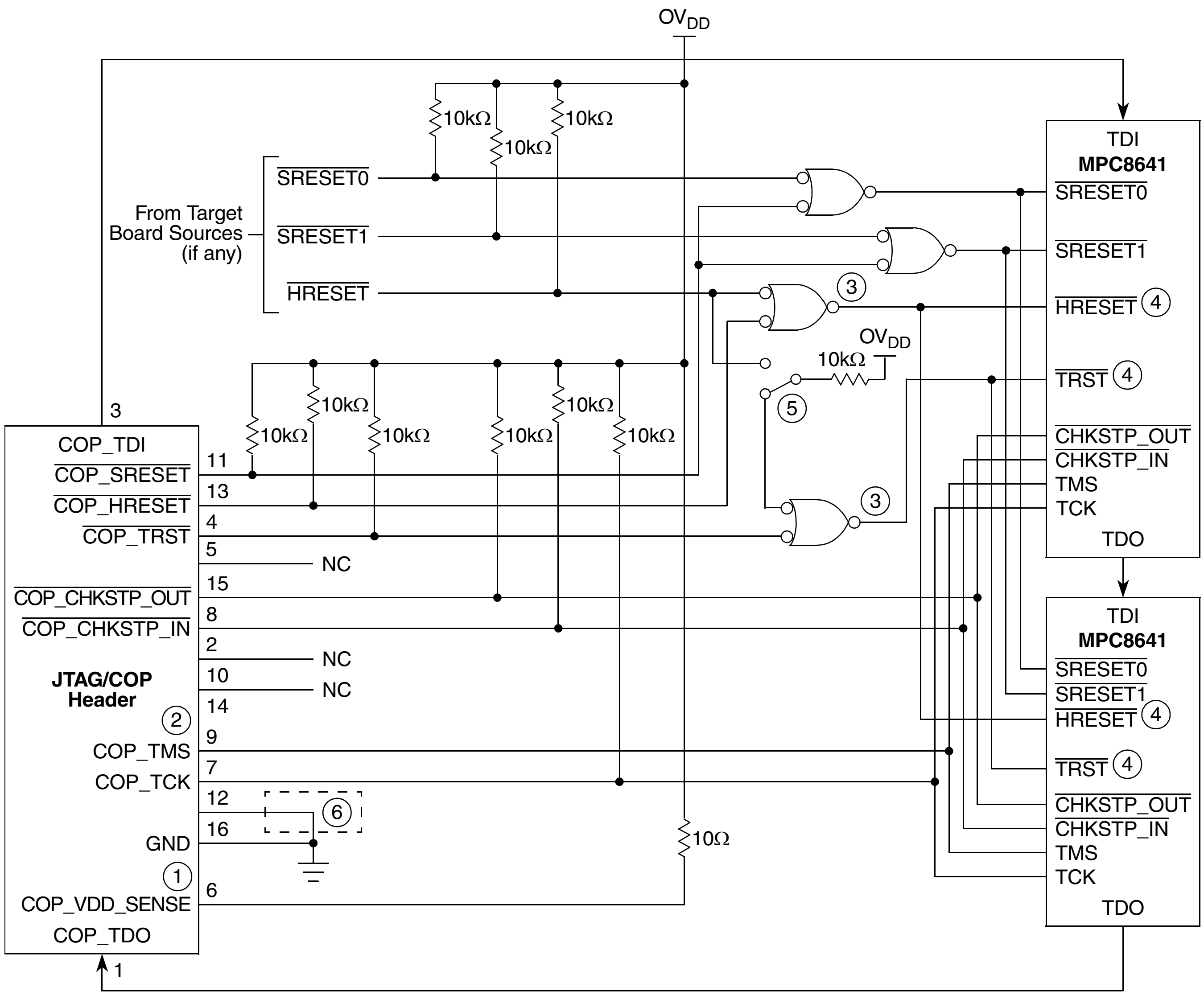


Figure 67. COP Connector Physical Pinout



Notes:

1. Populate this with a 10Ω resistor for short circuit/current-limiting protection.
2. KEY location; pin 14 is not physically present on the COP header.
3. Use a AND gate with sufficient drive strength to drive two inputs.
4. The COP port and target board should be able to independently assert $\overline{\text{HRESET}}$ and $\overline{\text{TRST}}$ to the processor in order to fully control the processor as shown above.
5. This switch is included as a precaution for BSDL testing. The switch should be open during BSDL testing to avoid accidentally asserting the $\overline{\text{TRST}}$ line. If BSDL testing is not being performed, this switch should be closed or removed.
6. Although pin 12 is defined as a No-Connect, some debug tools may use pin 12 as an additional GND pin for improved signal integrity.

Figure 69. JTAG/COP Interface Connection for Multiple MPC8641 Devices in Daisy Chain Configuration