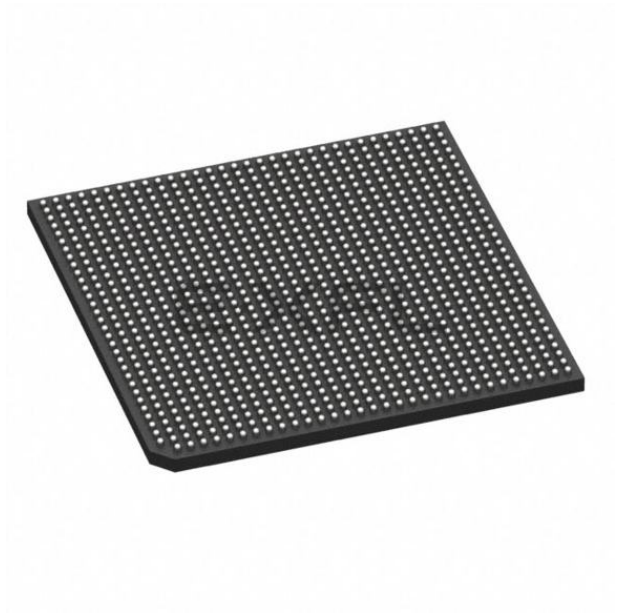

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e600
Number of Cores/Bus Width	2 Core, 32-Bit
Speed	1.0GHz
Co-Processors/DSP	-
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (4)
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	1023-BCBGA, FCCBGA
Supplier Device Package	1023-FCCBGA (33x33)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc8641dvu1000gc

2 Electrical Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC8641. The MPC8641 is currently targeted to these specifications.

2.1 Overall DC Electrical Characteristics

This section covers the ratings, conditions, and other characteristics.

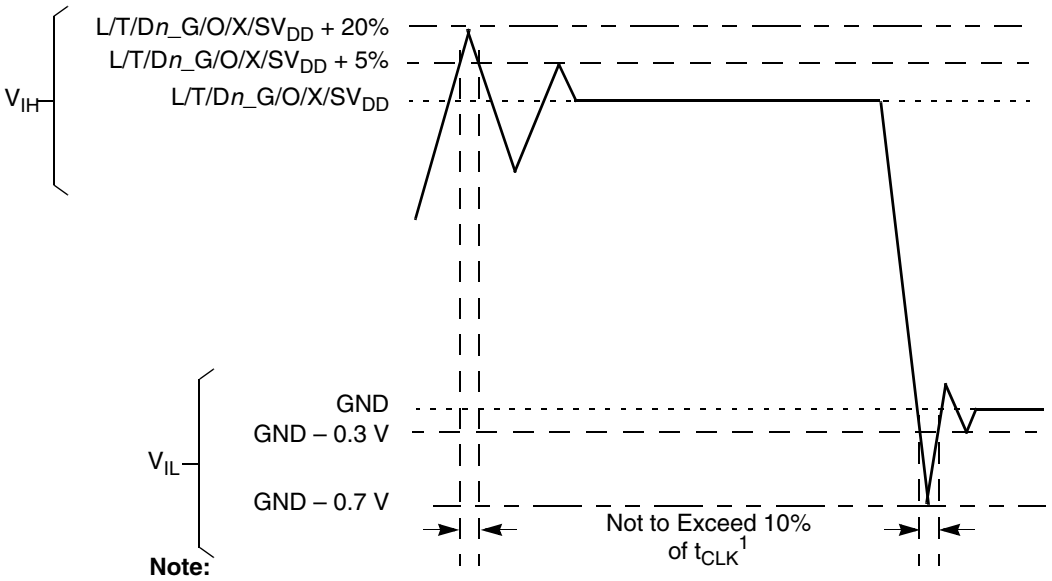
2.1.1 Absolute Maximum Ratings

Table 1 provides the absolute maximum ratings.

Table 1. Absolute Maximum Ratings[1]

Characteristic	Symbol	Absolute Maximum Value	Unit	Notes
Cores supply voltages	V_{DD}_Core0, V_{DD}_Core1	–0.3 to 1.21 V	V	2
Cores PLL supply	AV_{DD}_Core0, AV_{DD}_Core1	–0.3 to 1.21 V	V	—
SerDes Transceiver Supply (Ports 1 and 2)	SV_{DD}	–0.3 to 1.21 V	V	—
SerDes Serial I/O Supply Port 1	XV_{DD}_SRDS1	–0.3 to 1.21V	V	—
SerDes Serial I/O Supply Port 2	XV_{DD}_SRDS2	–0.3 to 1.21 V	V	—
SerDes DLL and PLL supply voltage for Port 1 and Port 2	AV_{DD}_SRDS1, AV_{DD}_SRDS2	–0.3 to 1.21V	V	—
Platform Supply voltage	V_{DD}_PLAT	–0.3 to 1.21V	V	—
Local Bus and Platform PLL supply voltage	AV_{DD}_LB, AV_{DD}_PLAT	–0.3 to 1.21V	V	—
DDR and DDR2 SDRAM I/O supply voltages	D1_GV_{DD}, D2_GV_{DD}	–0.3 to 2.75 V	V	3
		–0.3 to 1.98 V	V	3
eTSEC 1 and 2 I/O supply voltage	LV_{DD}	–0.3 to 3.63 V	V	4
		–0.3 to 2.75 V	V	4
eTSEC 3 and 4 I/O supply voltage	TV_{DD}	–0.3 to 3.63 V	V	4
		–0.3 to 2.75 V	V	4
Local Bus, DUART, DMA, Multiprocessor Interrupts, System Control & Clocking, Debug, Test, Power management, I^2C, JTAG and Miscellaneous I/O voltage	OV_{DD}	–0.3 to 3.63 V	V	—

Figure 2 shows the undershoot and overshoot voltages at the interfaces of the MPC8641.



Note:
1. t_{CLK} references clocks for various functional blocks as follows:

DDR*n* = 10% of D*n*_MCK period
eTSEC*n* = 10% of EC*n*_GTX_CLK125 period
Local Bus = 10% of LCLK[0:2] period
I^2C = 10% of SYSCLK
JTAG = 10% of SYSCLK

Figure 2. Overshoot/Undershoot Voltage for D*n*_M/O/L/TV_{IN}

The MPC8641 core voltage must always be provided at nominal V_{DD}_Core*n* (See Table 2 for actual recommended core voltage). Voltage to the processor interface I/Os are provided through separate sets of supply pins and must be provided at the voltages shown in Table 2. The input voltage threshold scales with respect to the associated I/O supply voltage. OV_{DD} and L/TV_{DD} based receivers are simple CMOS I/O circuits and satisfy appropriate LVCMOS type specifications. The DDR SDRAM interface uses a single-ended differential receiver referenced to each externally supplied D*n*_MV_{REF} signal (nominally set to D*n*_GV_{DD}/2) as is appropriate for the (SSTL-18 and SSTL-25) electrical signaling standards.

2.1.3 Output Driver Characteristics

Table 3 provides information on the characteristics of the output driver strengths. The values are preliminary estimates.

Table 3. Output Drive Capability

Driver Type	Programmable Output Impedance (Ω)	Supply Voltage	Notes
DDR1 signal	18 36 (half strength mode)	D*n*_GV_{DD} = 2.5 V	4, 9
DDR2 signal	18 36 (half strength mode)	D*n*_GV_{DD} = 1.8 V	1, 5, 9
Local Bus signals	45 25	OV_{DD} = 3.3 V	2, 6
eTSEC/10/100 signals	45	T/LV_{DD} = 3.3 V	6
	30	T/LV_{DD} = 2.5 V	6
DUART, DMA, Multiprocessor Interrupts, System Control & Clocking, Debug, Test, Power management, JTAG and Miscellaneous I/O voltage	45	OV_{DD} = 3.3 V	6
I^2C	150	OV_{DD} = 3.3 V	7
SRIO, PCI Express	100	SV_{DD} = 1.1/1.05 V	3, 8

Notes:
1. See the DDR Control Driver registers in the MPC8641D reference manual for more information.
2. Only the following local bus signals have programmable drive strengths: LALE, LAD[0:31], LDP[0:3], LA[27:31], LCKE, LCS[1:2], LWE[0:3], LGPL1, LGPL2, LGPL3, LGPL4, LGPL5, LCLK[0:2]. The other local bus signals have a fixed drive strength of 45 Ω. See the POR Impedance Control register in the MPC8641D reference manual for more information about local bus signals and their drive strength programmability.
3. See Section 17, "Signal Listings," for details on resistor requirements for the calibration of SD*n*_IMP_CAL_TX and SD*n*_IMP_CAL_RX transmit and receive signals.
4. Stub Series Terminated Logic (SSTL-25) type pins.
5. Stub Series Terminated Logic (SSTL-18) type pins.
6. Low Voltage Transistor-Transistor Logic (LVTTL) type pins.
7. Open Drain type pins.
8. Low Voltage Differential Signaling (LVDS) type pins.
9. The drive strength of the DDR interface in half strength mode is at T_j = 105C and at D*n*_GV_{DD} (min).

2.2 Power Up/Down Sequence

The MPC8641 requires its power rails to be applied in a specific sequence in order to ensure proper device operation.

NOTE

The recommended maximum ramp up time for power supplies is 20 milliseconds.

The chronological order of power up is as follows:

1. All power rails other than DDR I/O (D*n*_GV_{DD}, and D*n*_MV_{REF}).

4 Input Clocks

Table 7 provides the system clock (SYSCLK) DC specifications for the MPC8641.

Table 7. SYSCLK DC Electrical Characteristics (OVDD = 3.3 V ± 165 mV)

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	–0.3	0.8	V
Input current (V_{IN} [1] = 0 V or V_{IN} = V_{DD})	I_{IN}	—	±5	μA

Note:
1. Note that the symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

4.1 System Clock Timing

Table 8 provides the system clock (SYSCLK) AC timing specifications for the MPC8641.

Table 8. SYSCLK AC Timing Specifications

At recommended operating conditions (see Table 2) with OV_{DD} = 3.3 V ± 165 mV.

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
SYSCLK frequency	f_{SYSCLK}	66	—	166.66	MHz	1
SYSCLK cycle time	t_{SYSCLK}	6	—	—	ns	—
SYSCLK rise and fall time	t_{KH}, t_{KL}	0.6	1.0	1.2	ns	2
SYSCLK duty cycle	t_{KHK}/t_{SYSCLK}	40	—	60	%	3
SYSCLK jitter	—	—	—	150	ps	4, 5

Notes:
1. **Caution:** The MPX clock to SYSCLK ratio and e600 core to MPX clock ratio settings must be chosen such that the resulting SYSCLK frequency, e600 (core) frequency, and MPX clock frequency do not exceed their respective maximum or minimum operating frequencies. See Section 18.2, “MPX to SYSCLK PLL Ratio,” and Section 18.3, “e600 to MPX clock PLL Ratio,” for ratio settings.
2. Rise and fall times for SYSCLK are measured at 0.4 V and 2.7 V.
3. Timing is guaranteed by design and characterization.
4. This represents the short term jitter only and is guaranteed by design.
5. The SYSCLK driver’s closed loop jitter bandwidth should be <500 kHz at –20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track SYSCLK drivers with the specified jitter. Note that the frequency modulation for SYSCLK reduces significantly for the spread spectrum source case. This is to guarantee what is supported based on design.

4.1.1 SYSCLK and Spread Spectrum Sources

Spread spectrum clock sources are an increasingly popular way to control electromagnetic interference emissions (EMI) by spreading the emitted noise to a wider spectrum and reducing the peak noise magnitude in order to meet industry and government requirements. These clock sources intentionally add long-term jitter in order to diffuse the EMI spectral content. The jitter specification given in Table 8 considers short-term (cycle-to-cycle) jitter only and the clock generator’s cycle-to-cycle output jitter

Table 15 provides the recommended operating conditions for the DDR SDRAM component(s) when D*n*_GV_{DD}(typ) = 2.5 V.

Table 15. DDR SDRAM DC Electrical Characteristics for D*n*_GV_{DD} (typ) = 2.5 V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
I/O supply voltage	D*n*_GV_{DD}	2.375	2.625	V	1
I/O reference voltage	D*n*_MV_{REF}	0.49 × D*n*_GV_{DD}	0.51 × D*n*_GV_{DD}	V	2
I/O termination voltage	V_{TT}	D*n*_MV_{REF} – 0.04	D*n*_MV_{REF} + 0.04	V	3
Input high voltage	V_{IH}	D*n*_MV_{REF} + 0.15	D*n*_GV_{DD} + 0.3	V	—
Input low voltage	V_{IL}	–0.3	D*n*_MV_{REF}– 0.15	V	—
Output leakage current	I_{OZ}	–50	50	μA	4
Output high current (V_{OUT} = 1.95 V)	I_{OH}	–16.2	—	mA	—
Output low current (V_{OUT} = 0.35 V)	I_{OL}	16.2	—	mA	—

Notes:
1. D*n*_GV_{DD} is expected to be within 50 mV of the DRAM D*n*_GV_{DD} at all times.
2. MV_{REF} is expected to be equal to 0.5 × D*n*_GV_{DD}, and to track D*n*_GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on D*n*_MV_{REF} may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to D*n*_MV_{REF}. This rail should track variations in the DC level of D*n*_MV_{REF}.
4. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ D*n*_GV_{DD}.

Table 16 provides the DDR capacitance when D*n*_GV_{DD} (typ)=2.5 V.

Table 16. DDR SDRAM Capacitance for D*n*_GV_{DD} (typ) = 2.5 V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input/output capacitance: DQ, DQS	C_{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS	C_{DIO}	—	0.5	pF	1

Note:
1. This parameter is sampled. D*n*_GV_{DD} = 2.5 V ± 0.125 V, f = 1 MHz, T_A = 25°C, V_{OUT} = D*n*_GVDD/2, V_{OUT} (peak-to-peak) = 0.2 V.

Table 17 provides the current draw characteristics for MV_{REF}.

Table 17. Current Draw Characteristics for MV_{REF}

Parameter / Condition	Symbol	Min	Max	Unit	Note
Current draw for MV_{REF}	I_{MVREF}	—	500	μA	1

1. The voltage regulator for MV_{REF} must be able to supply up to 500 μA current.

Table 21. DDR SDRAM Output AC Timing Specifications (continued)

At recommended operating conditions.

Parameter	Symbol [1]	Min	Max	Unit	Notes
$\overline{\text{MCS}}$[n] output hold with respect to MCK	t_{DDKHCX}			ns	3
600 MHz		1.10	—		7
533 MHz		1.48	—		7
400 MHz		1.95	—		
MCK to MDQS Skew	t_{DDKHMH}	–0.6	0.6	ns	4
MDQ/MECC/MDM output setup with respect to MDQS	t_{DDKHDS}, t_{DDKLDS}			ps	5
600 MHz		500	—		7
533 MHz		590	—		7
400 MHz		700	—		
MDQ/MECC/MDM output hold with respect to MDQS	t_{DDKHDX}, t_{DDKLDX}			ps	5
600 MHz		500	—		7
533 MHz		590	—		7
400 MHz		700	—		
MDQS preamble start	t_{DDKHMP}	$-0.5 \times t_{MCK} - 0.6$	$-0.5 \times t_{MCK} + 0.6$	ns	6

Table 29. GMII Receive AC Timing Specifications (continued)

At recommended operating conditions with L/TV_{DD} of 3.3 V ± 5% and 2.5 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
RX_CLK clock fall time (80%-20%)	t_{GRXF}[2]	—	—	1.0	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{GRDVKH} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{RX} clock reference (K) going to the high state (H) or setup time. Also, t_{GRDXKL} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{GRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{GRX} represents the GMII (G) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Guaranteed by design.
3. ±100 ppm tolerance on RX_CLK frequency

Figure 11 provides the AC test load for eTSEC.

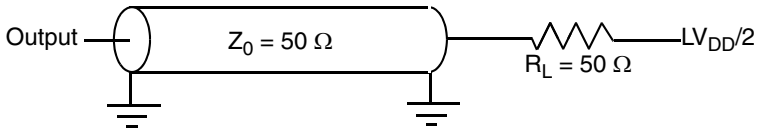


Figure 11. eTSEC AC Test Load

Figure 12 shows the GMII receive AC timing diagram.

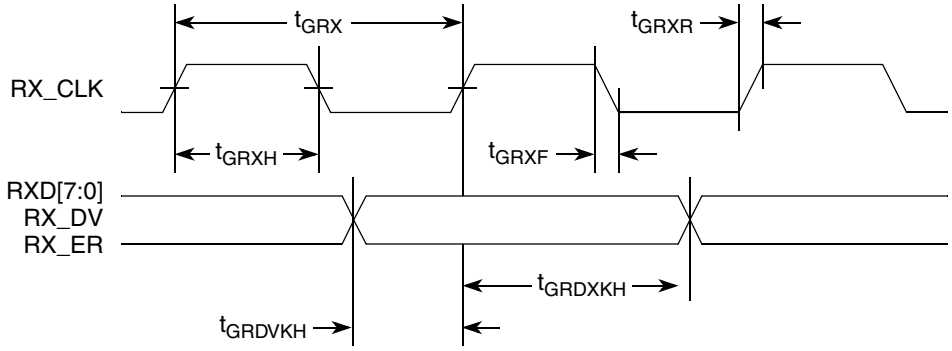


Figure 12. GMII Receive AC Timing Diagram

8.2.4 TBI AC Timing Specifications

This section describes the TBI transmit and receive AC timing specifications.

8.2.4.1 TBI Transmit AC Timing Specifications

Table 32 provides the TBI transmit AC timing specifications.

Table 32. TBI Transmit AC Timing Specifications

At recommended operating conditions with L/TV_{DD} of 3.3 V ± 5% and 2.5 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
TCG[9:0] setup time GTX_CLK going high	t_{TTKHDV}	2.0	—	—	ns
TCG[9:0] hold time from GTX_CLK going high	t_{TTKHDX}	1.0	—	—	ns
GTX_CLK rise time (20%–80%)	t_{TTXR}[2]	—	—	1.0	ns
GTX_CLK fall time (80%–20%)	t_{TTXF}[2]	—	—	1.0	ns

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{TTKHDV} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the valid state (V) or setup time. Also, t_{TTKHDX} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the invalid state (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{TTX} represents the TBI (T) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Guaranteed by design.

Figure 16 shows the TBI transmit AC timing diagram.

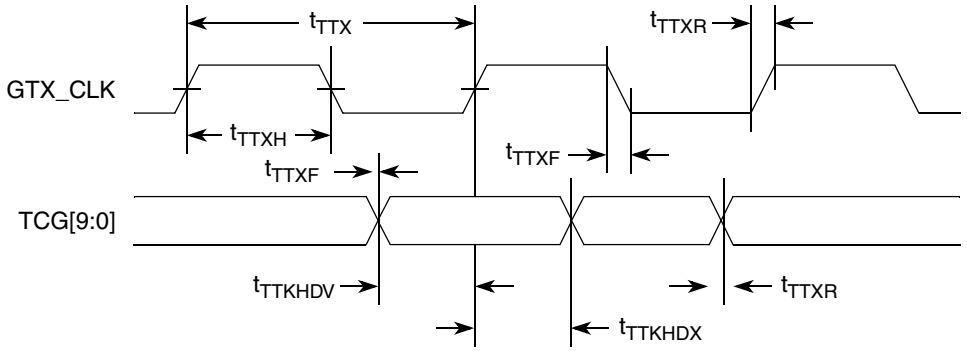


Figure 16. TBI Transmit AC Timing Diagram

Table 35. RGMII and RTBI AC Timing Specifications (continued)

At recommended operating conditions with L/TV_{DD} of 2.5 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
Clock period duration [3]	t_{RGT}[5,6]	7.2	8.0	8.8	ns
Duty cycle for 10BASE-T and 100BASE-TX [3, 4]	t_{RGTH}/t_{RGT}[5]	40	50	60	%
Rise time (20%–80%)	t_{RGTR}[5]	—	—	0.75	ns
Fall time (80%–20%)	t_{RGTF}[5]	—	—	0.75	ns

Notes:

1. Note that, in general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII and RTBI timing. For example, the subscript of t_{RGT} represents the TBI (T) receive (RX) clock. Note also that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).
2. This implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 1.5 ns will be added to the associated clock signal.
3. For 10 and 100 Mbps, t_{RGT} scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned between.
5. Guaranteed by characterization
6. ±100 ppm tolerance on RX_CLK frequency

Figure 19 shows the RGMII and RTBI AC timing and multiplexing diagrams.

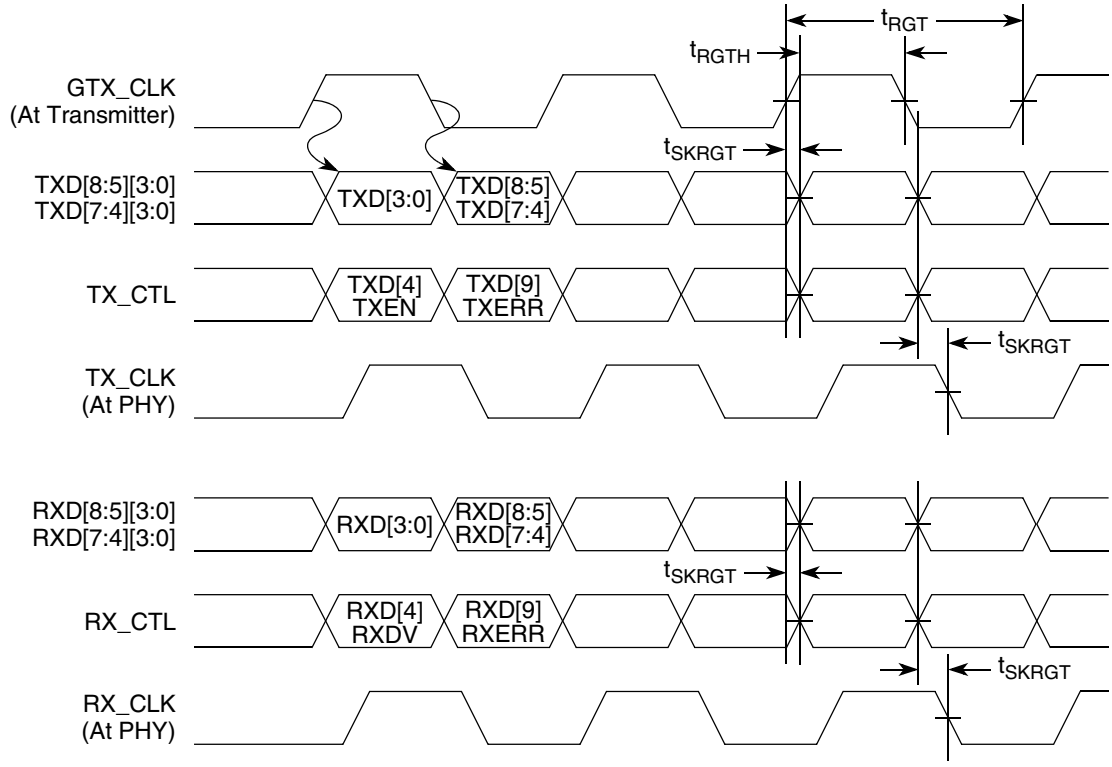


Figure 19. RGMII and RTBI AC Timing and Multiplexing Diagrams

Table 41. Local Bus Timing Parameters (OV_{DD} = 3.3 V)m - PLL Enabled (continued)

Parameter	Symbol [1]	Min	Max	Unit	Notes
Local bus clock to LALE assertion	$t_{LBKHOV4}$	—	2.3	ns	3
Output hold from local bus clock (except LAD/LDP and LALE)	$t_{LBKHOX1}$	0.7	—	ns	—
Output hold from local bus clock for LAD/LDP	$t_{LBKHOX2}$	0.7	—	ns	3
Local bus clock to output high Impedance (except LAD/LDP and LALE)	$t_{LBKHOZ1}$	—	2.5	ns	5
Local bus clock to output high impedance for LAD/LDP	$t_{LBKHOZ2}$	—	2.5	ns	5

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(First two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(First two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one(1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to LSYNC_IN for PLL enabled and internal local bus clock for PLL bypass mode.
3. All signals are measured from $OV_{DD}/2$ of the rising edge of LSYNC_IN for PLL enabled or internal local bus clock for PLL bypass mode to $0.4 \times OV_{DD}$ of the signal in question for 3.3-V signaling levels.
4. Input timings are measured at the pin.
5. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
6. t_{LBOTOT} is a measurement of the minimum time between the negation of LALE and any change in LAD. t_{LBOTOT} is programmed with the LBCR[AHD] parameter.
7. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at $BV_{DD}/2$.
8. Guaranteed by design.

Figure 25 provides the AC test load for the local bus.

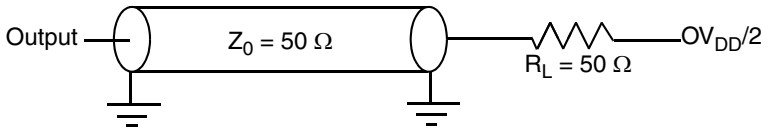


Figure 25. Local Bus AC Test Load

Figure 26 to Figure 31 show the local bus signals.

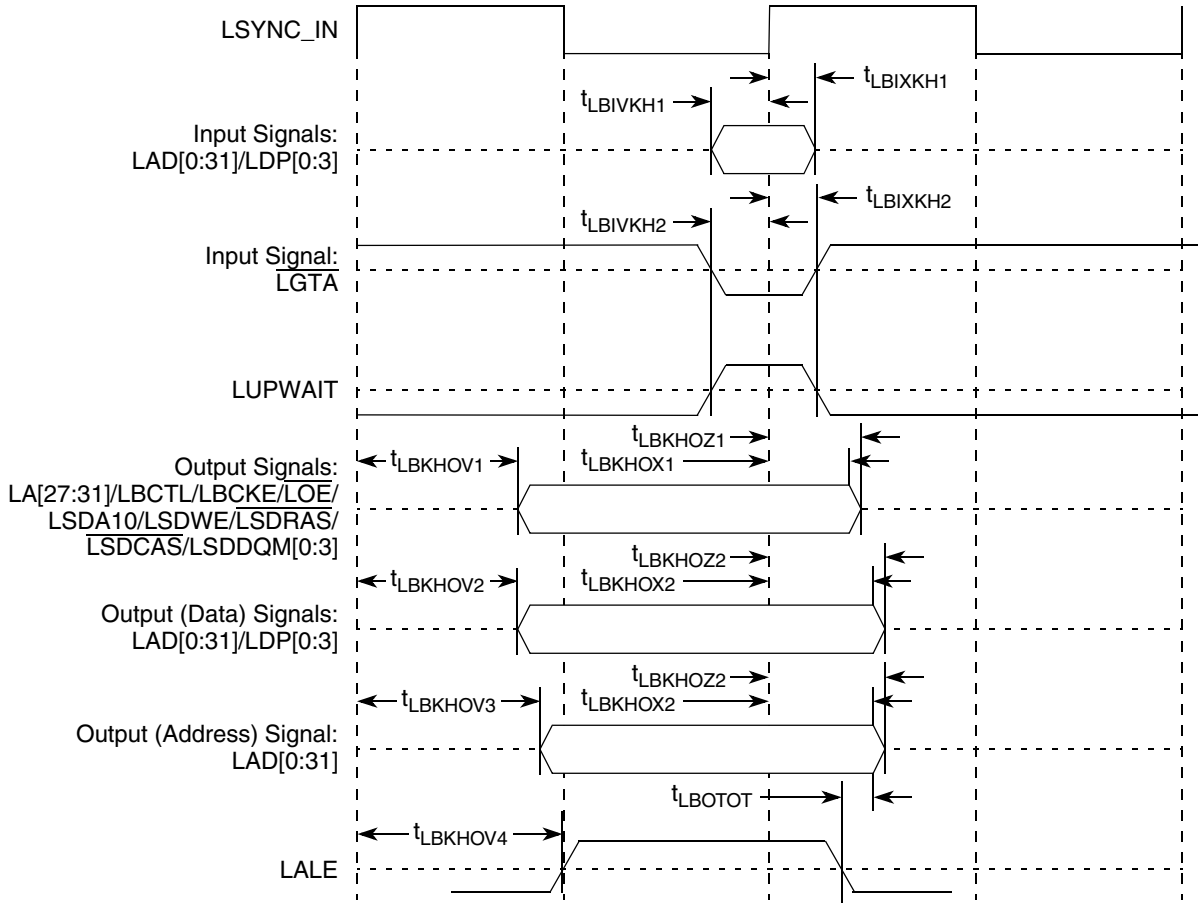


Figure 26. Local Bus Signals (PLL Enabled)

NOTE

PLL bypass mode is recommended when LBIU frequency is at or below 83 MHz. When LBIU operates above 83 MHz, LBIU PLL is recommended to be enabled.

Table 42 describes the general timing parameters of the local bus interface at OV_{DD} = 3.3 V with PLL bypassed.

Table 42. Local Bus Timing Parameters—PLL Bypassed

Parameter	Symbol [1]	Min	Max	Unit	Notes
Local bus cycle time	t_{LBK}	12	—	ns	2
Local bus duty cycle	t_{LBKH}/t_{LBK}	45	55	%	—
Internal launch/capture clock to LCLK delay	t_{LBKHKT}	2.3	3.9	ns	8
Input setup to local bus clock (except $\overline{\text{LGTA}}$/LUPWAIT)	$t_{LBIVKH1}$	5.7	—	ns	4, 5
$\overline{\text{LGTA}}$/LUPWAIT input setup to local bus clock	$t_{LBIVKL2}$	5.6	—	ns	4, 5
Input hold from local bus clock (except $\overline{\text{LGTA}}$/LUPWAIT)	$t_{LBIXKH1}$	–1.8	—	ns	4, 5

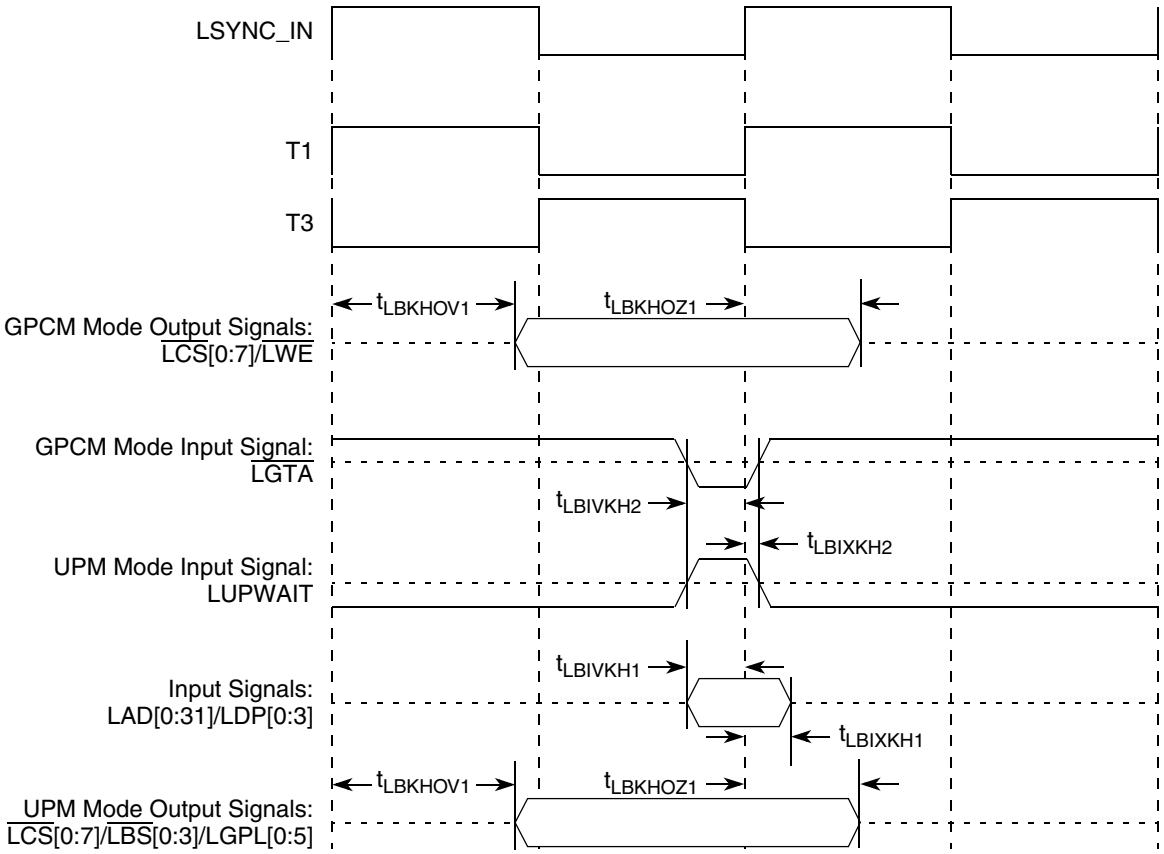


Figure 28. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 2 (clock ratio of 4) (PLL Enabled)

Figure 34 provides the $\overline{\text{TRST}}$ timing diagram.

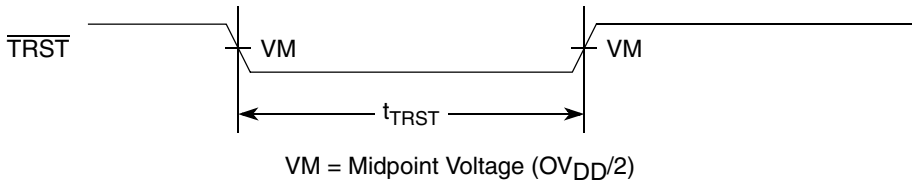


Figure 34. $\overline{\text{TRST}}$ Timing Diagram

Figure 35 provides the boundary-scan timing diagram.

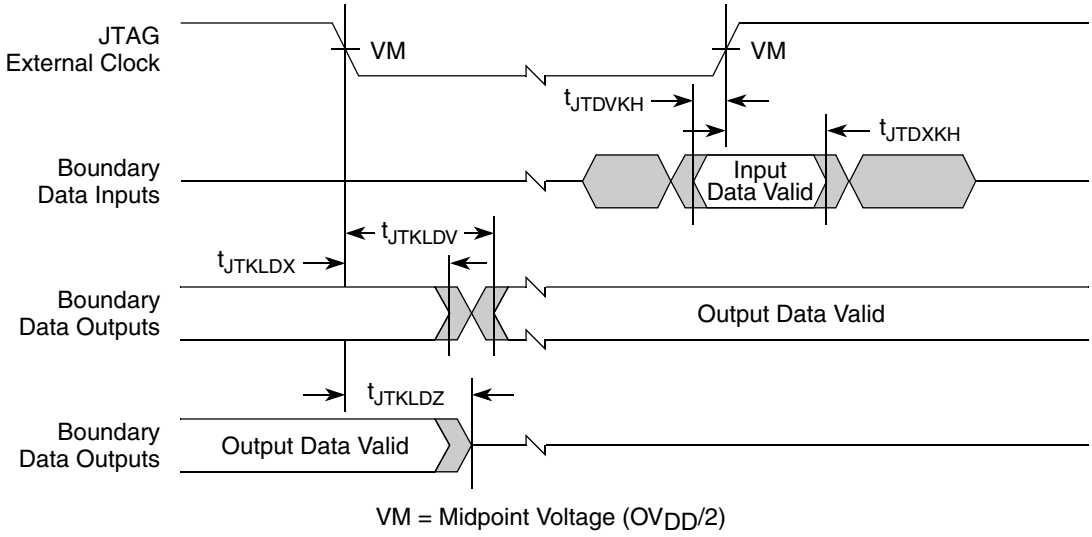


Figure 35. Boundary-Scan Timing Diagram

12 I²C

This section describes the DC and AC electrical characteristics for the I²C interfaces of the MPC8641.

12.1 I²C DC Electrical Characteristics

Table 45 provides the DC electrical characteristics for the I²C interfaces.

Table 45. I²C DC Electrical Characteristics

At recommended operating conditions with OV_{DD} of 3.3 V ± 5%.

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage level	V_{IH}	$0.7 \times OV_{DD}$	$OV_{DD} + 0.3$	V	—
Input low voltage level	V_{IL}	–0.3	$0.3 \times OV_{DD}$	V	—
Low level output voltage	V_{OL}	0	$0.2 \times OV_{DD}$	V	1
Pulse width of spikes which must be suppressed by the input filter	t_{I2KHKL}	0	50	ns	2
Input current each I/O pin (input voltage is between $0.1 \times OV_{DD}$ and $0.9 \times OV_{DD}$(max)	I_I	–10	10	μA	3

provide additional margin to adequately compensate for the degraded minimum Receiver eye diagram (shown in Figure 51) expected at the input Receiver based on some adequate combination of system simulations and the Return Loss measured looking into the RX package and silicon. The RX eye diagram must be aligned in time using the jitter median to locate the center of the eye diagram.

The eye diagram must be valid for any 250 consecutive UIs.

A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.

NOTE

The reference impedance for return loss measurements is 50Ω to ground for both the D+ and D- line (that is, as measured by a Vector Network Analyzer with 50Ω probes—see Figure 52). Note that the series capacitors, C_{TX}, are optional for the return loss measurement.

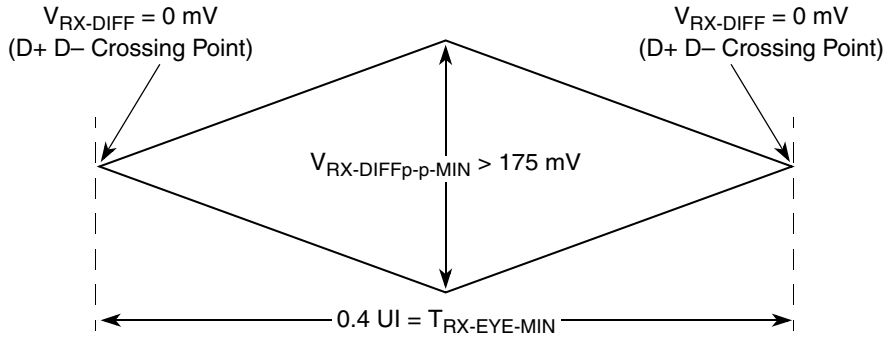


Figure 51. Minimum Receiver Eye Timing and Voltage Compliance Specification

14.5.1 Compliance Test and Measurement Load

The AC timing and voltage parameters must be verified at the measurement point, as specified within 0.2 inches of the package pins, into a test/measurement load shown in Figure 52.

NOTE

The allowance of the measurement point to be within 0.2 inches of the package pins is meant to acknowledge that package/board routing may benefit from D+ and D– not being exactly matched in length at the package pin boundary.

15.4 Equalization

With the use of high speed serial links, the interconnect media will cause degradation of the signal at the receiver. Effects such as Inter-Symbol Interference (ISI) or data dependent jitter are produced. This loss can be large enough to degrade the eye opening at the receiver beyond what is allowed in the specification. To negate a portion of these effects, equalization can be used. The most common equalization techniques that can be used are:

- A passive high pass filter network placed at the receiver. This is often referred to as passive equalization.
- The use of active circuits in the receiver. This is often referred to as adaptive equalization.

15.5 Explanatory Note on Transmitter and Receiver Specifications

AC electrical specifications are given for transmitter and receiver. Long run and short run interfaces at three baud rates (a total of six cases) are described.

The parameters for the AC electrical specifications are guided by the XAUI electrical interface specified in Clause 47 of IEEE 802.3ae-2002.

XAUI has similar application goals to serial RapidIO, as described in Section 8.1. The goal of this standard is that electrical designs for serial RapidIO can reuse electrical designs for XAUI, suitably modified for applications at the baud intervals and reaches described herein.

15.6 Transmitter Specifications

LP-Serial transmitter electrical and timing specifications are stated in the text and tables of this section.

The differential return loss, S11, of the transmitter in each case shall be better than

- –10 dB for (Baud Frequency)/10 < Freq(f) < 625 MHz, and
- –10 dB + 10log(f/625 MHz) dB for 625 MHz ≤ Freq(f) ≤ Baud Frequency

The reference impedance for the differential return loss measurements is 100 Ohm resistive. Differential return loss includes contributions from on-chip circuitry, chip packaging and any off-chip components related to the driver. The output impedance requirement applies to all valid output levels.

It is recommended that the 20%–80% rise/fall time of the transmitter, as measured at the transmitter output, in each case have a minimum value 60 ps.

It is recommended that the timing skew at the output of an LP-Serial transmitter between the two signals that comprise a differential pair not exceed 25 ps at 1.25 GB, 20 ps at 2.50 GB and 15 ps at 3.125 GB.

Table 63. MPC8641 Signal Reference by Functional Block (continued)

Name[1]	Package Pin Number	Pin Type	Power Supply	Notes
D1_MDVAL/LB_DVAL	J16	O	OV_{DD}	10
D2_MDVAL	D19	O	OV_{DD}	—
Power Management Signals[5]				
ASLEEP	C19	O	OV_{DD}	—
System Clocking Signals[5]				
SYSCLK	G16	I	OV_{DD}	—
RTC	K17	I	OV_{DD}	32
CLK_OUT	B16	O	OV_{DD}	23
Test Signals[5]				
$\overline{\text{LSSD\_MODE}}$	C18	I	OV_{DD}	26
TEST_MODE[0:3]	C16, E17, D18, D16	I	OV_{DD}	26
JTAG Signals[5]				
TCK	H18	I	OV_{DD}	—
TDI	J18	I	OV_{DD}	24
TDO	G18	O	OV_{DD}	23
TMS	F18	I	OV_{DD}	24
$\overline{\text{TRST}}$	A17	I	OV_{DD}	24
Miscellaneous[5]				
Spare	J17	—	—	13
GPOUT[0:7]/ TSEC1_TXD[0:7]	AF25, AC23, AG24, AG23, AE24, AE23, AE22, AD22	O	OV_{DD}	6, 10
GPIN[0:7]/ TSEC1_RXD[0:7]	AL25, AL24, AK26, AK25, AM26, AF26, AH24, AG25	I	OV_{DD}	10
GPOUT[8:15]/ TSEC2_TXD[0:7]	AB20, AJ23, AJ22, AD19, AH23, AH21, AG22, AG21	O	OV_{DD}	10
GPIN[8:15]/ TSEC2_RXD[0:7]	AL22, AK22, AM21, AH20, AG20, AF20, AF23, AF22	I	OV_{DD}	10
Additional Analog Signals				
TEMP_ANODE	AA11	Thermal	—	—
TEMP_CATHODE	Y11	Thermal	—	—
Sense, Power and GND Signals				
$SENSEV_{DD}$_Core0	M14	V_{DD}_Core0 sensing pin	—	31
$SENSEV_{DD}$_Core1	U20	V_{DD}_Core1 sensing pin	—	12,31, *S1*

Table 63. MPC8641 Signal Reference by Functional Block (continued)

Name[1]	Package Pin Number	Pin Type	Power Supply	Notes

37.This pin is only an output in FIFO mode when used as Rx Flow Control.

38.This pin functions as cfg_dram_type[0 or 1] at reset and MUST BE VALID BEFORE HRESET ASSERTION in device sleep mode.

39. Should be pulled to ground if unused (such as in FIFO, MII and RMII modes).

40. See Section 18.4.2, “Platform to FIFO Restrictions” for clock speed limitations for this pin when used in FIFO mode.

41. The phase between the output clocks TSEC1_GTX_CLK and TSEC2_GTX_CLK (ports 1 and 2) is no more than 100 ps. The phase between the output clocks TSEC3_GTX_CLK and TSEC4_GTX_CLK (ports 3 and 4) is no more than 100 ps.

42. For systems which boot from Local Bus (GPCM)-controlled flash, a pullup on LGPL4 is required.

Special Notes for Single Core Device:

S1. Solder ball for this signal will not be populated in the single core package.

S2. The PLL filter from V_{DD}_Core1 to AV_{DD}_Core1 should be removed. AV_{DD}_Core1 should be pulled to ground with a weak (2–10 kΩ) resistor. See Section 20.2.1, “PLL Power Supply Filtering” for more details.

S3. This pin should be pulled to GND for the single core device.

S4. No special requirement for this pin on single core device. Pin should be tied to power supply as directed for dual core.

18 Clocking

This section describes the PLL configuration of the MPC8641. Note that the platform clock is identical to the MPX clock.

18.1 Clock Ranges

Table 64 provides the clocking specifications for the processor cores and Table 65 provides the clocking specifications for the memory bus. Table 66 provides the clocking for the Platform/MPX bus and Table 67 provides the clocking for the Local bus.

Table 64. Processor Core Clocking Specifications

Characteristic	Maximum Processor Core Frequency								Unit	Notes
	1000 MHz		1250MHz		1333MHz		1500 MHz			
	Min	Max	Min	Max	Min	Max	Min	Max		
e600 core processor frequency	800	1000	800	1250	800	1333	800	1500	MHz	1, 2

Notes:

1. **Caution:** The MPX clock to SYSCLK ratio and e600 core to MPX clock ratio settings must be chosen such that the resulting SYSCLK frequency, e600 (core) frequency, and MPX clock frequency do not exceed their respective maximum or minimum operating frequencies. Refer to Section 18.2, “MPX to SYSCLK PLL Ratio,” and Section 18.3, “e600 to MPX clock PLL Ratio,” for ratio settings.
2. The minimum e600 core frequency is based on the minimum platform clock frequency of 400 MHz.

20 System Design Information

This section provides electrical and thermal design recommendations for successful application of the MPC8641.

20.1 System Clocking

This device includes six PLLs, as follows:

1. The platform PLL generates the platform clock from the externally supplied SYSCLK input. The frequency ratio between the platform and SYSCLK is selected using the platform PLL ratio configuration bits as described in Section 18.2, "MPX to SYSCLK PLL Ratio."
2. The dual e600 Core PLLs generate the e600 clock from the externally supplied input.
3. The local bus PLL generates the clock for the local bus.
4. There are two internal PLLs for the SerDes block.

20.2 Power Supply Design and Sequencing

20.2.1 PLL Power Supply Filtering

Each of the PLLs listed above is provided with power through independent power supply pins.

There are a number of ways to reliably provide power to the PLLs, but the recommended solution is to provide independent filter circuits per PLL power supply as illustrated in Figure 64, one to each of the AV_{DD} type pins. By providing independent filters to each PLL the opportunity to cause noise injection from one PLL to the other is reduced.

This circuit is intended to filter noise in the PLLs resonant frequency range from a 500 kHz to 10 MHz range. It should be built with surface mount capacitors with minimum Effective Series Inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

Each circuit should be placed as close as possible to the specific AV_{DD} type pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the AV_{DD} type pin, which is on the periphery of the footprint, without the inductance of vias.

Figure 63 and Figure 64 show the PLL power supply filter circuits for the platform and cores, respectively.

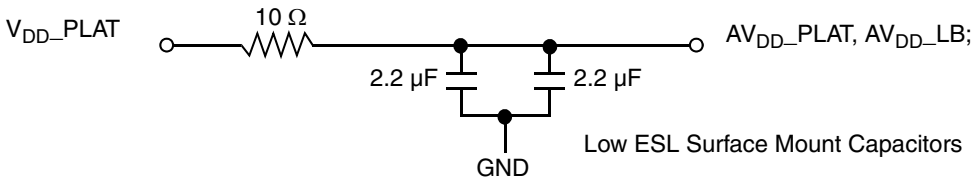


Figure 63. MPC8641 PLL Power Supply Filter Circuit (for platform and Local Bus)

Local Bus - If parity is not used, tie LDP[0:3] to ground via a 4.7 kΩ resistor, tie LPBSE to OV_{DD} via a 4.7 kΩ resistor (pull-up resistor). For systems which boot from Local Bus (GPCM)-controlled flash, a pullup on LGPL4 is required.

SerDes - Receiver lanes configured for PCI Express are allowed to be disconnected (as would occur when a PCI Express slot is connected but not populated). Directions for terminating the SerDes signals is discussed in Section 20.5.1, "Guidelines for High-Speed Interface Termination."

20.5.1 Guidelines for High-Speed Interface Termination

20.5.1.1 SerDes Interface

The high-speed SerDes interface can be disabled through the POR input cfg_io_ports[0:3] and through the DEVDISR register in software. If a SerDes port is disabled through the POR input the user can not enable it through the DEVDISR register in software. However, if a SerDes port is enabled through the POR input the user can disable it through the DEVDISR register in software. Disabling a SerDes port through software should be done on a temporary basis. Power is always required for the SerDes interface, even if the port is disabled through either mechanism. Table 72 describes the possible enabled/disabled scenarios for a SerDes port. The termination recommendations must be followed for each port.

Table 72. SerDes Port Enabled/Disabled Configurations

	Disabled through POR input	Enabled through POR input
Enabled through DEVDISR	SerDes port is disabled (and cannot be enabled through DEVDISR) Complete termination required (Reference Clock not required)	SerDes port is enabled Partial termination may be required[1] (Reference Clock is required)
Disabled through DEVDISR	SerDes port is disabled (through POR input) Complete termination required (Reference Clock not required)	SerDes port is disabled after software disables port Same termination requirements as when the port is enabled through POR input[2] (Reference Clock is required)

Notes:

1 Partial Termination when a SerDes port is enabled through both POR input and DEVDISR is determined by the SerDes port mode. If the port is in x8 PCI Express mode, no termination is required because all pins are being used. If the port is in x1/x2/x4 PCI Express mode, termination is required on the unused pins. If the port is in x4 Serial RapidIO mode termination is required on the unused pins.

2 If a SerDes port is enabled through the POR input and then disabled through DEVDISR, no hardware changes are required. Termination of the SerDes port should follow what is required when the port is enabled through both POR input and DEVDISR. See Note 1 for more information.

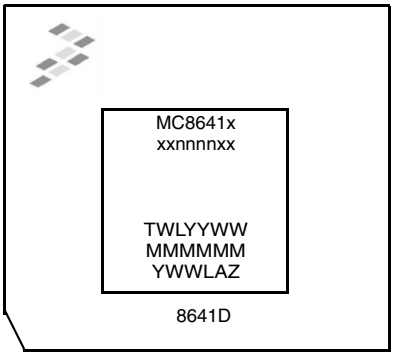
If the high-speed SerDes port requires complete or partial termination, the unused pins should be terminated as described in this section.

The following pins must be left unconnected (floating):

- SD*n*_TX[7:0]
- $\overline{\text{SD}n\text{\_TX}}$[7:0]

21.2 Part Marking

Parts are marked as the example shown in Figure 70.



NOTE:
TWLYYWW is the test code
MMMMMM is the M00 (mask) number.
YWWLAZ is the assembly traceability code.

Figure 70. Part Marking for FC-CBGA Device

22 Document Revision History

Table 76 provides a revision history for the MPC8641D hardware specification.

Table 76. Document Revision History

Revision	Date	Substantive Change(s)
3	05/2014	• Updated the Serial RapidIO equation in Section 4.4, “Platform Frequency Requirements for PCI-Express and Serial RapidIO” • Updated Section 19.2.4, “Temperature Diode,” by removing the ideality factor value. • Added VJ package type designator and footnotes to Table 74, “Part Numbering Nomenclature” and Section 16.1, “Package Parameters for the MPC8641.”
2	07/2009	• Added note 8 to Table 49, “Differential Transmitter (TX) Output Specifications.” • Added Revision E to Table 74, “Part Numbering Nomenclature.”
1	11/2008	• Added Section 4.4, “Platform Frequency Requirements for PCI-Express and Serial RapidIO.” • Removed the statement “Note that core processor speed of 1500 MHz is only available for the MPC8641D (dual core)” from Note 2 in Table 74 because a 1500 MHz core is offered for both MPC8641D (dual core) and MPC8641 (single core). • Added Note 8 to Figure 57 and Figure 58.
0	07/2008	• Initial Release