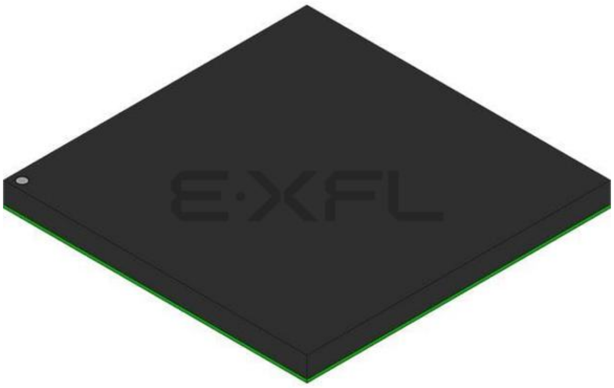

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e600
Number of Cores/Bus Width	2 Core, 32-Bit
Speed	1.0GHz
Co-Processors/DSP	-
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (4)
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	1023-BCBGA, FCCBGA
Supplier Device Package	1023-FCCBGA (33x33)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc8641dvu1000ge

2 Electrical Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC8641. The MPC8641 is currently targeted to these specifications.

2.1 Overall DC Electrical Characteristics

This section covers the ratings, conditions, and other characteristics.

2.1.1 Absolute Maximum Ratings

Table 1 provides the absolute maximum ratings.

Table 1. Absolute Maximum Ratings[1]

Characteristic	Symbol	Absolute Maximum Value	Unit	Notes
Cores supply voltages	V_{DD}_Core0, V_{DD}_Core1	–0.3 to 1.21 V	V	2
Cores PLL supply	AV_{DD}_Core0, AV_{DD}_Core1	–0.3 to 1.21 V	V	—
SerDes Transceiver Supply (Ports 1 and 2)	SV_{DD}	–0.3 to 1.21 V	V	—
SerDes Serial I/O Supply Port 1	XV_{DD}_SRDS1	–0.3 to 1.21V	V	—
SerDes Serial I/O Supply Port 2	XV_{DD}_SRDS2	–0.3 to 1.21 V	V	—
SerDes DLL and PLL supply voltage for Port 1 and Port 2	AV_{DD}_SRDS1, AV_{DD}_SRDS2	–0.3 to 1.21V	V	—
Platform Supply voltage	V_{DD}_PLAT	–0.3 to 1.21V	V	—
Local Bus and Platform PLL supply voltage	AV_{DD}_LB, AV_{DD}_PLAT	–0.3 to 1.21V	V	—
DDR and DDR2 SDRAM I/O supply voltages	D1_GV_{DD}, D2_GV_{DD}	–0.3 to 2.75 V	V	3
		–0.3 to 1.98 V	V	3
eTSEC 1 and 2 I/O supply voltage	LV_{DD}	–0.3 to 3.63 V	V	4
		–0.3 to 2.75 V	V	4
eTSEC 3 and 4 I/O supply voltage	TV_{DD}	–0.3 to 3.63 V	V	4
		–0.3 to 2.75 V	V	4
Local Bus, DUART, DMA, Multiprocessor Interrupts, System Control & Clocking, Debug, Test, Power management, I^2C, JTAG and Miscellaneous I/O voltage	OV_{DD}	–0.3 to 3.63 V	V	—

3 Power Characteristics

The power dissipation for the dual core MPC8641D device is shown in Table 4.

Table 4. MPC8641D Power Dissipation (Dual Core)

<table>
<tr><th>Power Mode</th><th>Core Frequency (MHz)</th><th>Platform Frequency (MHz)</th><th>V_{DD}_Coren, V_{DD}_PLAT (Volts)</th><th>Junction Temperature</th><th>Power (Watts)</th><th>Notes</th></tr>
<tr><td>Typical</td><td rowspan="3">1500 MHz</td><td rowspan="3">600 MHz</td><td rowspan="3">1.1 V</td><td>65 °C</td><td>32.1</td><td>1, 2</td></tr>
<tr><td>Thermal</td><td rowspan="2">105 °C</td><td>43.4</td><td>1, 3</td></tr>
<tr><td>Maximum</td><td>49.9</td><td>1, 4</td></tr>
<tr><td>Typical</td><td rowspan="3">1333 MHz</td><td rowspan="3">533 MHz</td><td rowspan="3">1.05 V</td><td>65 °C</td><td>23.9</td><td>1, 2</td></tr>
<tr><td>Thermal</td><td rowspan="2">105 °C</td><td>30.0</td><td>1, 3</td></tr>
<tr><td>Maximum</td><td>34.1</td><td>1, 4</td></tr>
<tr><td>Typical</td><td rowspan="3">1250 MHz</td><td rowspan="3">500 MHz</td><td rowspan="3">1.05 V</td><td>65 °C</td><td>23.9</td><td>1, 2</td></tr>
<tr><td>Thermal</td><td rowspan="2">105 °C</td><td>30.0</td><td>1, 3</td></tr>
<tr><td>Maximum</td><td>34.1</td><td>1, 4</td></tr>
<tr><td>Typical</td><td rowspan="3">1000 MHz</td><td rowspan="3">400 MHz</td><td rowspan="3">1.05 V</td><td>65 °C</td><td>23.9</td><td>1, 2</td></tr>
<tr><td>Thermal</td><td rowspan="2">105 °C</td><td>30.0</td><td>1, 3</td></tr>
<tr><td>Maximum</td><td>34.1</td><td>1, 4</td></tr>
<tr><td>Typical</td><td rowspan="3">1000 MHz</td><td rowspan="3">500 MHz</td><td rowspan="3">0.95 V,
1.05 V</td><td>65 °C</td><td>16.2</td><td>1, 2, 5</td></tr>
<tr><td>Thermal</td><td rowspan="2">105 °C</td><td>21.8</td><td>1, 3, 5</td></tr>
<tr><td>Maximum</td><td>25.0</td><td>1, 4, 5</td></tr>
</table>

Notes:

1. These values specify the power consumption at nominal voltage and apply to all valid processor bus frequencies and configurations. The values do not include power dissipation for I/O supplies.
2. Typical power is an average value measured at the nominal recommended core voltage (V_{DD}_Core*n*) and 65°C junction temperature (see Table 2)while running the Dhrystone 2.1 benchmark and achieving 2.3 Dhrystone MIPs/MHz with one core at 100% efficiency and the second core at 65% efficiency.
3. Thermal power is the average power measured at nominal core voltage (V_{DD}_Core*n*) and maximum operating junction temperature (see Table 2) while running the Dhrystone 2.1 benchmark and achieving 2.3 Dhrystone MIPs/MHz on both cores and a typical workload on platform interfaces.
4. Maximum power is the maximum power measured at nominal core voltage (V_{DD}_Core*n*) and maximum operating junction temperature (see Table 2) while running a test which includes an entirely L1-cache-resident, contrived sequence of instructions which keep all the execution units maximally busy on both cores.
5. These power numbers are for Part Number MC8641Dxx1000NX only. V_{DD}_Core*n* = 0.95 V and V_{DD}_PLAT = 1.05 V.

The power dissipation for the MPC8641 single core device is shown in Table 6.

Table 6. MPC8641 Power Dissipation (Single Core)

Power Mode	Core Frequency (MHz)	Platform Frequency (MHz)	V_{DD}_Coren, V_{DD}_PLAT (Volts)	Junction Temperature	Power (Watts)	Notes
Typical	1500 MHz	600 MHz	1.1 V	65 °C	20.3	1, 2
Thermal				105 °C	25.2	1, 3
Maxim					28.9	1, 4
Typical	1333 MHz	533 MHz	1.05 V	65 °C	16.3	1, 2
Thermal				105 °C	20.2	1, 3
Maximum					23.2	1, 4
Typical	1250 MHz	500 MHz	1.05 V	65 °C	16.3	1, 2
Thermal				105 °C	20.2	1, 3
Maximum					23.2	1, 4
Typical	1000 MHz	400 MHz	1.05 V	65 °C	16.3	1, 2
Thermal				105 °C	20.2	1, 3
Maximum					23.2	1, 4
Typical	1000 MHz	500 MHz	0.95 V, 1.05 V	65 °C	11.6	1, 2, 5
Thermal				105 °C	14.4	1, 3, 5
Maximum					16.5	1, 4, 5

Notes:

1. These values specify the power consumption at nominal voltage and apply to all valid processor bus frequencies and configurations. The values do not include power dissipation for I/O supplies.
2. Typical power is an average value measured at the nominal recommended core voltage (V_{DD}_Core*n*) and 65°C junction temperature (see Table 2)while running the Dhrystone 2.1 benchmark and achieving 2.3 Dhrystone MIPs/MHz.
3. Thermal power is the average power measured at nominal core voltage (V_{DD}_Core*n*) and maximum operating junction temperature (see Table 2) while running the Dhrystone 2.1 benchmark and achieving 2.3 Dhrystone MIPs/MHz and a typical workload on platform interfaces.
4. Maximum power is the maximum power measured at nominal core voltage (V_{DD}_Core*n*) and maximum operating junction temperature (see Table 2) while running a test which includes an entirely L1-cache-resident, contrived sequence of instructions which keep all the execution units maximally busy.
5. These power numbers are for Part Number MC8641xx1000NX only. V_{DD}_Core*n* = 0.95 V and V_{DD}_PLAT = 1.05 V.

5 RESET Initialization

This section describes the AC electrical specifications for the RESET initialization timing requirements of the MPC8641. Table 11 provides the RESET initialization AC timing specifications.

Table 11. RESET Initialization Timing Specifications

Parameter/Condition	Min	Max	Unit	Notes
Required assertion time of $\overline{\text{HRESET}}$	100	—	µs	—
Minimum assertion time for $\overline{\text{SRESET\_0}}$ & $\overline{\text{SRESET\_1}}$	3	—	SYSCLKs	1
Platform PLL input setup time with stable SYSCLK before $\overline{\text{HRESET}}$ negation	100	—	µs	2
Input setup time for POR configs (other than PLL config) with respect to negation of $\overline{\text{HRESET}}$	4	—	SYSCLKs	1
Input hold time for all POR configs (including PLL config) with respect to negation of $\overline{\text{HRESET}}$	2	—	SYSCLKs	1
Maximum valid-to-high impedance time for actively driven POR configs with respect to negation of $\overline{\text{HRESET}}$	—	5	SYSCLKs	1

Notes:
1. SYSCLK is the primary clock input for the MPC8641.
2 This is related to $\overline{\text{HRESET}}$ assertion time. Stable PLL configuration inputs are required when a stable SYSCLK is applied. See the *MPC8641D Integrated Host Processor Reference Manual* for more details on the power-on reset sequence.

Table 12 provides the PLL lock times.

Table 12. PLL Lock Times

Parameter/Condition	Min	Max	Unit	Notes
(Platform and E600) PLL lock times	—	100	µs	1
Local bus PLL	—	50	µs	—

Note:
1.The PLL lock time for e600 PLLs require an additional 255 MPX_CLK cycles.

Timing diagrams for FIFO appear in Figure 8 and Figure 9.

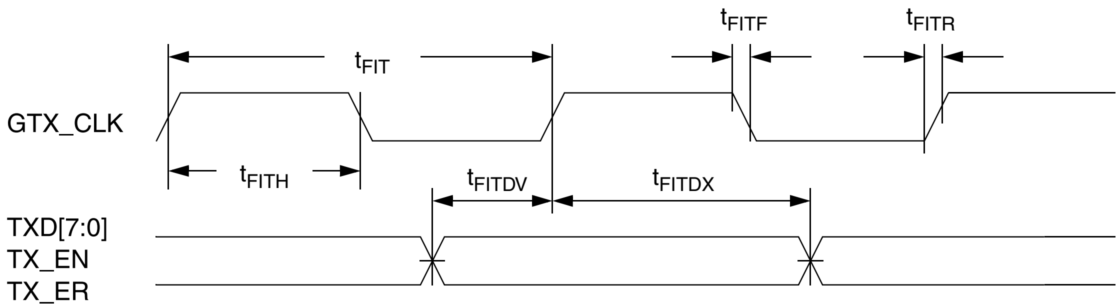


Figure 8. FIFO Transmit AC Timing Diagram

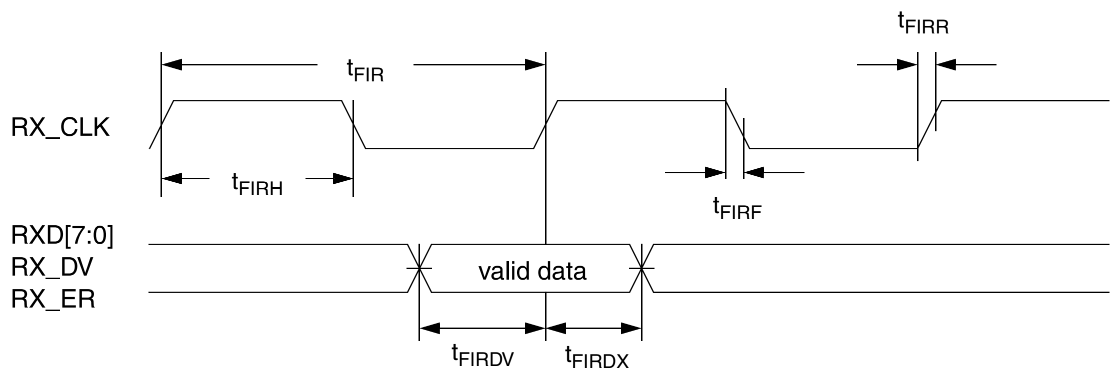


Figure 9. FIFO Receive AC Timing Diagram

8.2.2 GMII AC Timing Specifications

This section describes the GMII transmit and receive AC timing specifications.

8.2.2.1 GMII Transmit AC Timing Specifications

Table 28 provides the GMII transmit AC timing specifications.

Table 28. GMII Transmit AC Timing Specifications

At recommended operating conditions with L/TV_{DD} of 3.3 V ± 5% and 2.5 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
GMII data TXD[7:0], TX_ER, TX_EN setup time	t_{GTKHDV}	2.5	—	—	ns
GTX_CLK to GMII data TXD[7:0], TX_ER, TX_EN delay	t_{GTKHDX}	0.5	—	5.0	ns
GTX_CLK data clock rise time (20%-80%)	t_{GTXR} [2]	—	—	1.0	ns

8.2.7.2 RMII Receive AC Timing Specifications

Table 37. RMII Receive AC Timing Specifications

At recommended operating conditions with L/TV_{DD} of 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
REF_CLK clock period	t_{RMR}	15.0	20.0	25.0	ns
REF_CLK duty cycle	t_{RMRH}/t_{RMR}	35	50	65	%
REF_CLK peak-to-peak jitter	t_{RMRJ}	—	—	250	ps
Rise time REF_CLK (20%–80%)	t_{RMRR}	1.0	—	2.0	ns
Fall time REF_CLK (80%–20%)	t_{RMRF}	1.0	—	2.0	ns
RXD[1:0], CRS_DV, RX_ER setup time to REF_CLK rising edge	t_{RMRDV}	4.0	—	—	ns
RXD[1:0], CRS_DV, RX_ER hold time to REF_CLK rising edge	t_{RMRDX}	2.0	—	—	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 21 provides the AC test load for eTSEC.

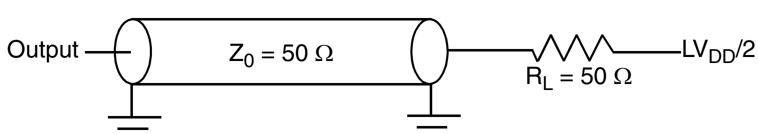


Figure 21. eTSEC AC Test Load

Figure 22 shows the RMII receive AC timing diagram.

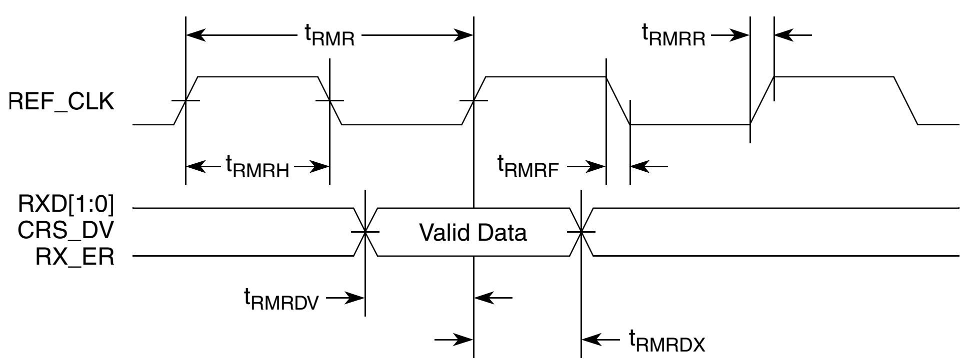


Figure 22. RMII Receive AC Timing Diagram

9 Ethernet Management Interface Electrical Characteristics

The electrical characteristics specified here apply to MII management interface signals MDIO (management data input/output) and MDC (management data clock). The electrical characteristics for GMII, RGMII, RMII, TBI and RTBI are specified in "Section 8, "Ethernet: Enhanced Three-Speed Ethernet (eTSEC), MII Management."

9.1 MII Management DC Electrical Characteristics

The MDC and MDIO are defined to operate at a supply voltage of 3.3 V. The DC electrical characteristics for MDIO and MDC are provided in Table 38.

Table 38. MII Management DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
Supply voltage (3.3 V)	OV_{DD}	3.135	3.465	V
Output high voltage (OV_{DD} = Min, I_{OH} = –1.0 mA)	V_{OH}	2.10	—	V
Output low voltage (OV_{DD} =Min, I_{OL} = 1.0 mA)	V_{OL}	—	0.50	V
Input high voltage	V_{IH}	1.70	—	V
Input low voltage	V_{IL}	—	0.90	V
Input high current (OV_{DD} = Max, V_{IN} [1] = 2.1 V)	I_{IH}	—	40	μA
Input low current (OV_{DD} = Max, V_{IN} = 0.5 V)	I_{IL}	–600	—	μA

Note:
1. Note that the symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

9.2 MII Management AC Electrical Specifications

Table 39 provides the MII management AC timing specifications.

Table 39. MII Management AC Timing Specifications

At recommended operating conditions with OV_{DD} is 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit	Notes
MDC frequency	f_{MDC}	2.5	—	9.3	MHz	2, 4
MDC period	t_{MDC}	80	—	400	ns	—
MDC clock pulse width high	t_{MDCH}	32	—	—	ns	—
MDC to MDIO valid	t_{MDKHDV}	$16*t_{MPXCLK}$	—	—	ns	5
MDC to MDIO delay	t_{MDKHDX}	10	—	$16*t_{MPXCLK}$	ns	3, 5
MDIO to MDC setup time	t_{MDDVKH}	5	—	—	ns	—

10 Local Bus

This section describes the DC and AC electrical specifications for the local bus interface of the MPC8641.

10.1 Local Bus DC Electrical Characteristics

Table 40 provides the DC electrical characteristics for the local bus interface operating at OV_{DD} = 3.3 V DC.

Table 40. Local Bus DC Electrical Characteristics (3.3 V DC)

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	–0.3	0.8	V
Input current (V_{IN} [1] = 0 V or V_{IN} = OV_{DD})	I_{IN}	—	±5	μA
High-level output voltage (OV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	OV_{DD} – 0.2	—	V
Low-level output voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.2	V

Note:

1. Note that the symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

10.2 Local Bus AC Electrical Specifications

Table 41 describes the timing parameters of the local bus interface at OV_{DD} = 3.3 V with PLL enabled. For information about the frequency range of local bus see Section 18.1, "Clock Ranges."

Table 41. Local Bus Timing Parameters (OV_{DD} = 3.3 V)m - PLL Enabled

Parameter	Symbol [1]	Min	Max	Unit	Notes
Local bus cycle time	t_{LBK}	7.5	—	ns	2
Local Bus Duty Cycle	t_{LBKH}/t_{LBK}	45	55	%	—
LCLK[n] skew to LCLK[m] or LSYNC_OUT	$t_{LBKSKEW}$	—	150	ps	7, 8
Input setup to local bus clock (except $\overline{\text{LGTA}}$/LUPWAIT)	$t_{LBIVKH1}$	1.8	—	ns	3, 4
$\overline{\text{LGTA}}$/LUPWAIT input setup to local bus clock	$t_{LBIVKH2}$	1.7	—	ns	3, 4
Input hold from local bus clock (except $\overline{\text{LGTA}}$/LUPWAIT)	$t_{LBIXKH1}$	1.0	—	ns	3, 4
$\overline{\text{LGTA}}$/LUPWAIT input hold from local bus clock	$t_{LBIXKH2}$	1.0	—	ns	3, 4
LALE output transition to LAD/LDP output transition (LATCH hold time)	t_{LBOTOT}	1.5	—	ns	6
Local bus clock to output valid (except LAD/LDP and LALE)	$t_{LBKHOV1}$	—	2.0	ns	—
Local bus clock to data valid for LAD/LDP	$t_{LBKHOV2}$	—	2.2	ns	—
Local bus clock to address valid for LAD	$t_{LBKHOV3}$	—	2.3	ns	—

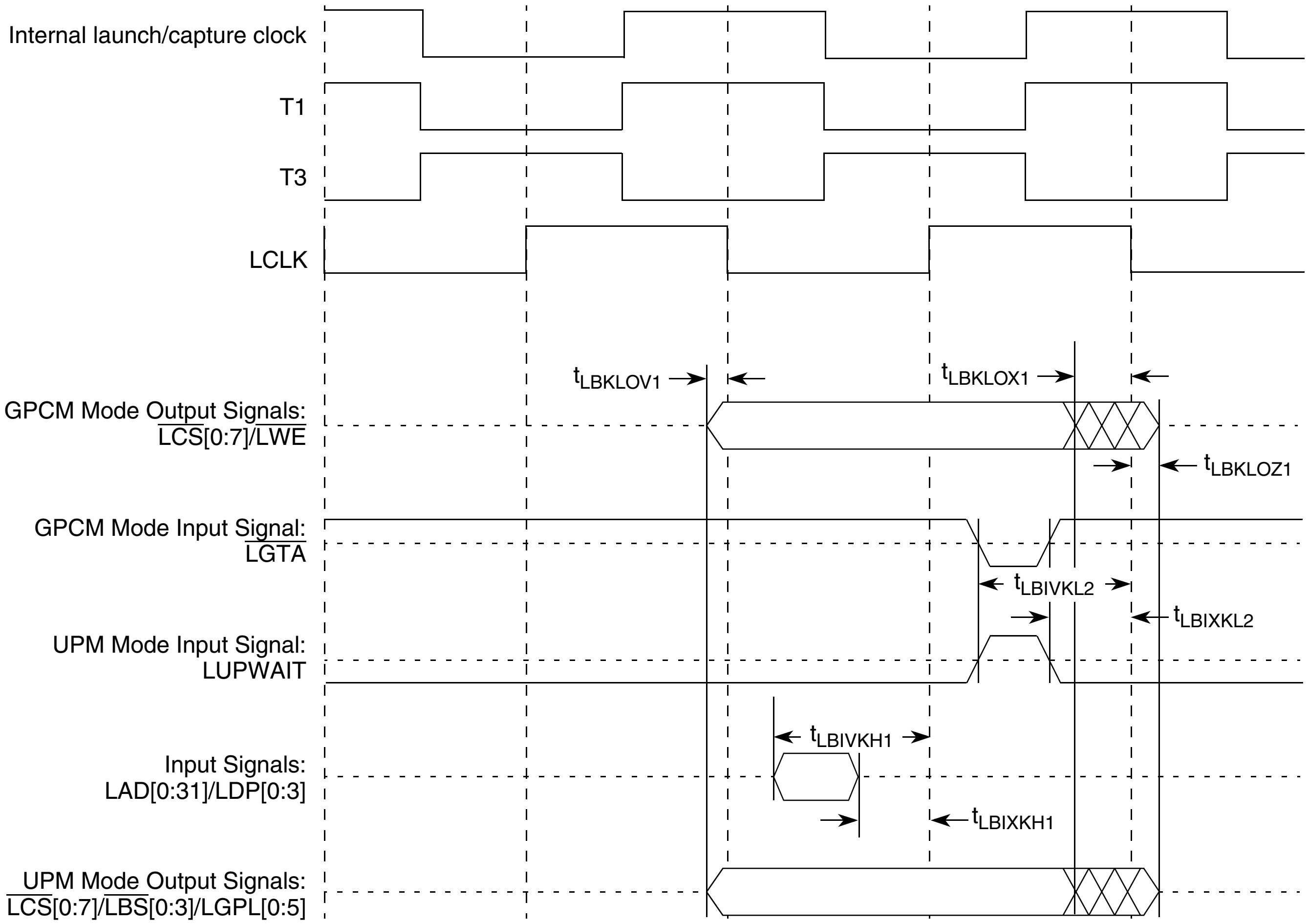


Figure 29. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 2 (clock ratio of 4) (PLL Bypass Mode)

13.2.3 Interfacing With Other Differential Signaling Levels

With on-chip termination to SGND, the differential reference clocks inputs are HCSL (High-Speed Current Steering Logic) compatible DC-coupled.

Many other low voltage differential type outputs like LVDS (Low Voltage Differential Signaling) can be used but may need to be AC-coupled due to the limited common mode input range allowed (100 to 400 mV) for DC-coupled connection.

LVPECL outputs can produce signal with too large amplitude and may need to be DC-biased at clock driver output first, then followed with series attenuation resistor to reduce the amplitude, in addition to AC-coupling.

NOTE

Figure 43 to Figure 46 below are for conceptual reference only. Due to the fact that clock driver chip's internal structure, output impedance and termination requirements are different between various clock driver chip manufacturers, it is very possible that the clock circuit reference designs provided by clock driver chip vendor are different from what is shown below. They might also vary from one vendor to the other. Therefore, Freescale Semiconductor can neither provide the optimal clock driver reference circuits, nor guarantee the correctness of the following clock driver connection reference circuits. The system designer is recommended to contact the selected clock driver chip vendor for the optimal reference circuits with the MPC8641D SerDes reference clock receiver requirement provided in this document.

14.1 DC Requirements for PCI Express SD*n*_REF_CLK and $\overline{\text{SD}n\text{\_REF\_CLK}}$

For more information, see Section 13.2, “SerDes Reference Clocks.”

14.2 AC Requirements for PCI Express SerDes Clocks

Table 48 lists AC requirements.

Table 48. SD*n*_REF_CLK and $\overline{\text{SD}n\text{\_REF\_CLK}}$ AC Requirements

Symbol	Parameter Description	Min	Typical	Max	Units	Notes
t_{REF}	REFCLK cycle time	—	10	—	ns	—
t_{REFCJ}	REFCLK cycle-to-cycle jitter. Difference in the period of any two adjacent REFCLK cycles	—	—	100	ps	—
t_{REFPJ}	Phase jitter. Deviation in edge location with respect to mean edge location	–50	—	50	ps	—

14.3 Clocking Dependencies

The ports on the two ends of a link must transmit data at a rate that is within 600 parts per million (ppm) of each other at all times. This is specified to allow bit rate clock sources with a +/– 300 ppm tolerance.

14.4 Physical Layer Specifications

The following is a summary of the specifications for the physical layer of PCI Express on this device. For further details as well as the specifications of the Transport and Data Link layer please use the PCI EXPRESS Base Specification. REV. 1.0a document.

14.4.1 Differential Transmitter (TX) Output

Table 49 defines the specifications for the differential output at all transmitters (TXs). The parameters are specified at the component pins.

Table 49. Differential Transmitter (TX) Output Specifications

Symbol	Parameter	Min	Nom	Max	Units	Comments
UI	Unit Interval	399.88	400	400.12	ps	Each UI is 400 ps ± 300 ppm. UI does not account for Spread Spectrum Clock dictated variations. See Note 1.
$V_{TX\text{-}DIFFp\text{-}p}$	Differential Peak-to-Peak Output Voltage	0.8	—	1.2	V	$V_{TX\text{-}DIFFp\text{-}p} = 2*\lvert V_{TX\text{-}D+} - V_{TX\text{-}D-}\rvert$ See Note 2.
$V_{TX\text{-}DE\text{-}RATIO}$	De- Emphasized Differential Output Voltage (Ratio)	–3.0	–3.5	–4.0	dB	Ratio of the $V_{TX\text{-}DIFFp\text{-}p}$ of the second and following bits after a transition divided by the $V_{TX\text{-}DIFFp\text{-}p}$ of the first bit after a transition. See Note 2.

Table 52. Short Run Transmitter AC Timing Specifications—1.25 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output Voltage,	V_O	–0.40	2.30	Volts	Voltage relative to COMMON of either signal comprising a differential pair
Differential Output Voltage	V_{DIFFPP}	500	1000	mV p-p	—
Deterministic Jitter	J_D	—	0.17	UI p-p	—
Total Jitter	J_T	—	0.35	UI p-p	—
Multiple output skew	S_{MO}	—	1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	800	800	ps	+/– 100 ppm

Table 53. Short Run Transmitter AC Timing Specifications—2.5 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output Voltage,	V_O	–0.40	2.30	Volts	Voltage relative to COMMON of either signal comprising a differential pair
Differential Output Voltage	V_{DIFFPP}	500	1000	mV p-p	—
Deterministic Jitter	J_D	—	0.17	UI p-p	—
Total Jitter	J_T	—	0.35	UI p-p	—
Multiple Output skew	S_{MO}	—	1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	400	400	ps	+/– 100 ppm

Table 54. Short Run Transmitter AC Timing Specifications—3.125 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output Voltage,	V_O	–0.40	2.30	Volts	Voltage relative to COMMON of either signal comprising a differential pair
Differential Output Voltage	V_{DIFFPP}	500	1000	mV p-p	—
Deterministic Jitter	J_D	—	0.17	UI p-p	—
Total Jitter	J_T	—	0.35	UI p-p	—

Table 54. Short Run Transmitter AC Timing Specifications—3.125 GBaud (continued)

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Multiple output skew	S_{MO}	—	1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	320	320	ps	+/– 100 ppm

Table 55. Long Run Transmitter AC Timing Specifications—1.25 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output Voltage,	V_O	–0.40	2.30	Volts	Voltage relative to COMMON of either signal comprising a differential pair
Differential Output Voltage	V_{DIFFPP}	800	1600	mV p-p	—
Deterministic Jitter	J_D	—	0.17	UI p-p	—
Total Jitter	J_T	—	0.35	UI p-p	—
Multiple output skew	S_{MO}	—	1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	800	800	ps	+/– 100 ppm

Table 56. Long Run Transmitter AC Timing Specifications—2.5 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output Voltage,	V_O	–0.40	2.30	Volts	Voltage relative to COMMON of either signal comprising a differential pair
Differential Output Voltage	V_{DIFFPP}	800	1600	mV p-p	—
Deterministic Jitter	J_D	—	0.17	UI p-p	—
Total Jitter	J_T	—	0.35	UI p-p	—
Multiple output skew	S_{MO}	—	1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	400	400	ps	+/– 100 ppm

8. Note that for MPC8641 (single core) the solder balls for the following signals/pins are not populated in the package: VDD_Core1 (R16, R18, R20, T17, T19, T21, T23, U16, U18, U22, V17, V19, V21, V23, W16, W18, W20, W22, Y17, Y19, Y21, Y23, AA16, AA18, AA20, AA22, AB23, AC24) and SENSEVDD_Core1 (U20).

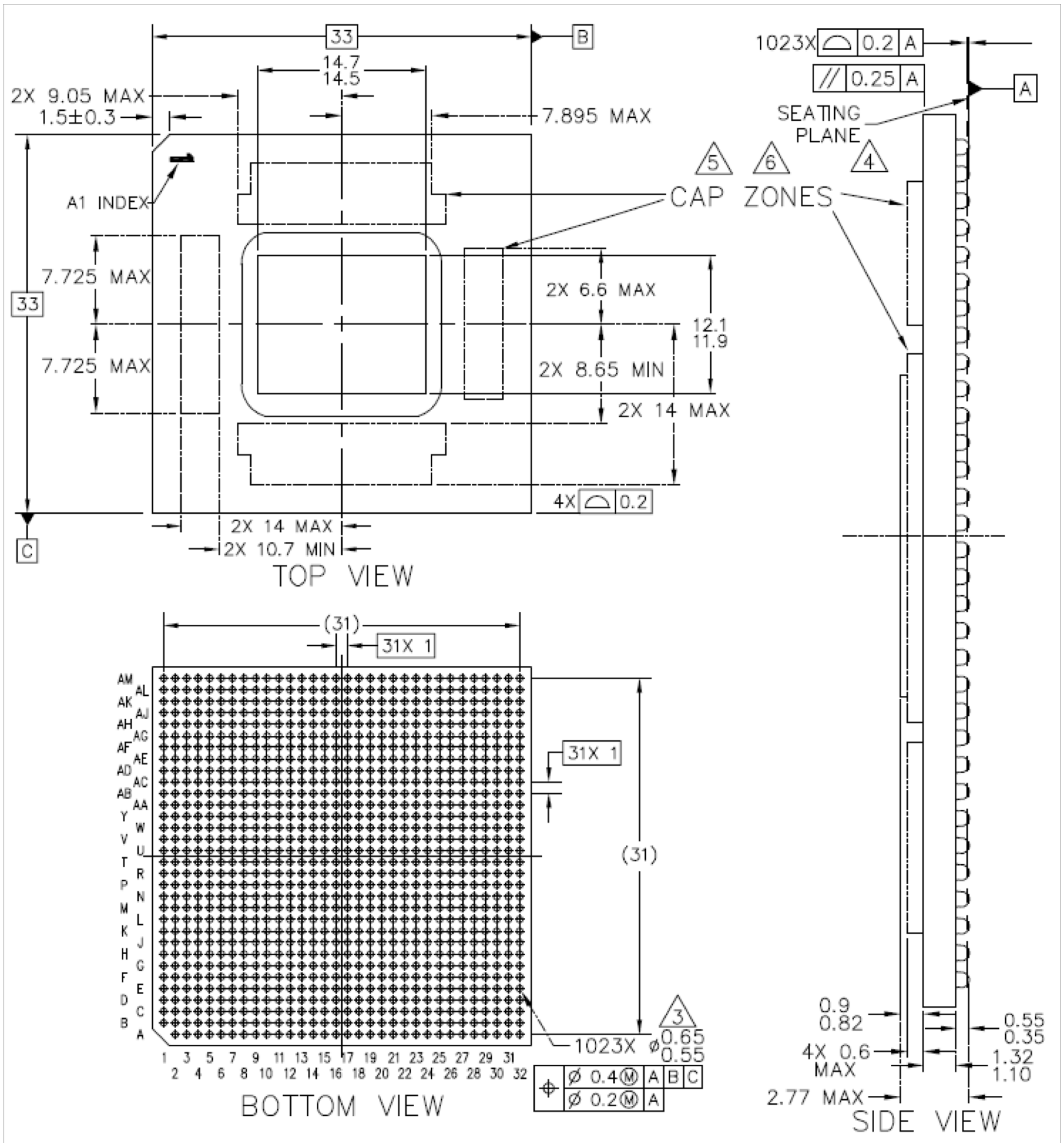


Figure 58. MPC8641D Lead-Free FC-CBGA Dimensions

NOTES for Figure 58

1. All dimensions are in millimeters.
2. Dimensions and tolerances per ASME Y14.5M-1994.
3. Maximum solder ball diameter measured parallel to datum A.
4. Datum A, the seating plane, is defined by the spherical crowns of the solder balls.
5. Capacitors may not be present on all devices.
6. Caution must be taken not to short capacitors or expose metal capacitor pads on package top.
7. All dimensions symmetrical about centerlines unless otherwise specified.
8. Note that for MPC8641 (single core) the solder balls for the following signals/pins are not populated in the package: VDD_Core1 (R16, R18, R20, T17, T19, T21, T23, U16, U18, U22, V17, V19, V21, V23, W16, W18, W20, W22, Y17, Y19, Y21, Y23, AA16, AA18, AA20, AA22, AB23, AC24) and SENSEVDD_Core1 (U20).

Table 63. MPC8641 Signal Reference by Functional Block (continued)

Name[1]	Package Pin Number	Pin Type	Power Supply	Notes
TSEC3_TX_EN	AH19	O	TV_{DD}	36
TSEC3_TX_ER	AH17	O	TV_{DD}	—
TSEC3_TX_CLK	AH18	I	TV_{DD}	40
TSEC3_GTX_CLK	AG19	O	TV_{DD}	41
TSEC3_CRS	AE15	I/O	TV_{DD}	37
TSEC3_COL	AF15	I	TV_{DD}	—
TSEC3_RXD[0:7]	AJ17, AE16, AH16, AH14, AJ19, AH15, AG16, AE19	I	TV_{DD}	—
TSEC3_RX_DV	AG15	I	TV_{DD}	—
TSEC3_RX_ER	AF16	I	TV_{DD}	—
TSEC3_RX_CLK	AJ18	I	TV_{DD}	40
eTSEC Port 4 Signals[5]				
TSEC4_TXD[0:3]	AC18, AC16, AD18, AD17	O	TV_{DD}	6
TSEC4_TXD[4]	AD16	O	TV_{DD}	25
TSEC4_TXD[5:7]	AB18, AB17, AB16	O	TV_{DD}	6
TSEC4_TX_EN	AF17	O	TV_{DD}	36
TSEC4_TX_ER	AF19	O	TV_{DD}	—
TSEC4_TX_CLK	AF18	I	TV_{DD}	40
TSEC4_GTX_CLK	AG17	O	TV_{DD}	41
TSEC4_CRS	AB14	I/O	TV_{DD}	37
TSEC4_COL	AC13	I	TV_{DD}	—
TSEC4_RXD[0:7]	AG14, AD13, AF13, AD14, AE14, AB15, AC14, AE17	I	TV_{DD}	—
TSEC4_RX_DV	AC15	I	TV_{DD}	—
TSEC4_RX_ER	AF14	I	TV_{DD}	—
TSEC4_RX_CLK	AG13	I	TV_{DD}	40
Local Bus Signals[5]				
LAD[0:31]	A30, E29, C29, D28, D29, H25, B29, A29, C28, L22, M22, A28, C27, H26, G26, B27, B26, A27, E27, G25, D26, E26, G24, F27, A26, A25, C25, H23, K22, D25, F25, H22	I/O	OV_{DD}	6
LDP[0:3]	A24, E24, C24, B24	I/O	OV_{DD}	6, 22
LA[27:31]	J21, K21, G22, F24, G21	O	OV_{DD}	6, 22
$\overline{\text{LCS}}$[0:4]	A22, C22, D23, E22, A23	O	OV_{DD}	7
$\overline{\text{LCS}}$[5]/$\overline{\text{DMA\_DREQ}}$[2]	B23	O	OV_{DD}	7, 9, 10

Another useful equation is:

$$V_H - V_L = n\frac{KT}{q}\left[\ln\frac{I_H}{I_L}\right]$$

Where:

I_{fw} = Forward current
I_s = Saturation current
V_d = Voltage at diode
V_f = Voltage forward biased
V_H = Diode voltage while I_H is flowing
V_L = Diode voltage while I_L is flowing
I_H = Larger diode bias current
I_L = Smaller diode bias current
q = Charge of electron (1.6×10^{-19} C)
n = Ideality factor (normally 1.0)
K = Boltzman's constant (1.38×10^{-23} Joules/K)
T = Temperature (Kelvins)

The ratio of I_H to I_L is usually selected to be 10:1. The above simplifies to the following:

$$V_H - V_L = 1.986 \times 10^{-4} \times nT$$

Solving for T, the equation becomes:

$$nT = \frac{V_H - V_L}{1.986 \times 10^{-4}}$$

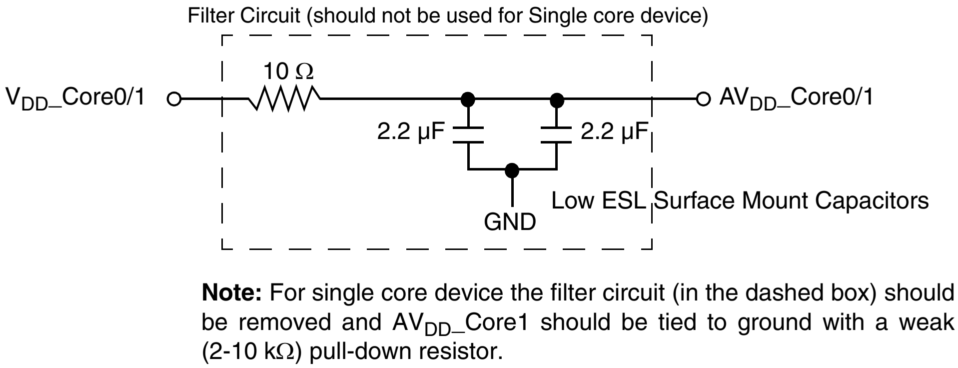
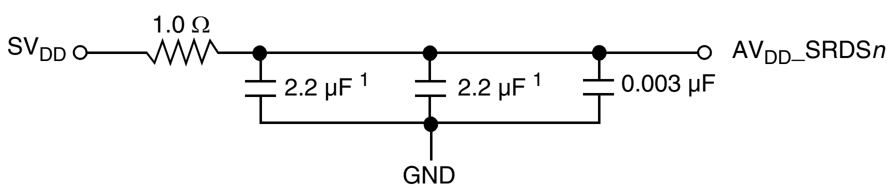


Figure 64. MPC8641 PLL Power Supply Filter Circuit (for cores)

The AV_{DD}_SRDS*n* signals provide power for the analog portions of the SerDes PLL. To ensure stability of the internal clock, the power supplied to the PLL is filtered using a circuit similar to the one shown in following figure. For maximum effectiveness, the filter circuit is placed as closely as possible to the AV_{DD}_SRDS*n* balls to ensure it filters out as much noise as possible. The ground connection should be near the AV_{DD}_SRDS*n* balls. The 0.003-µF capacitor is closest to the balls, followed by the two 2.2-µF capacitors, and finally the 1 Ω resistor to the board supply plane. The capacitors are connected from AV_{DD}_SRDS*n* to the ground plane. Use ceramic chip capacitors with the highest possible self-resonant frequency. All traces should be kept short, wide and direct.



1. An 0805 sized capacitor is recommended for system initial bring-up.

Figure 65. SerDes PLL Power Supply Filter

Note the following:

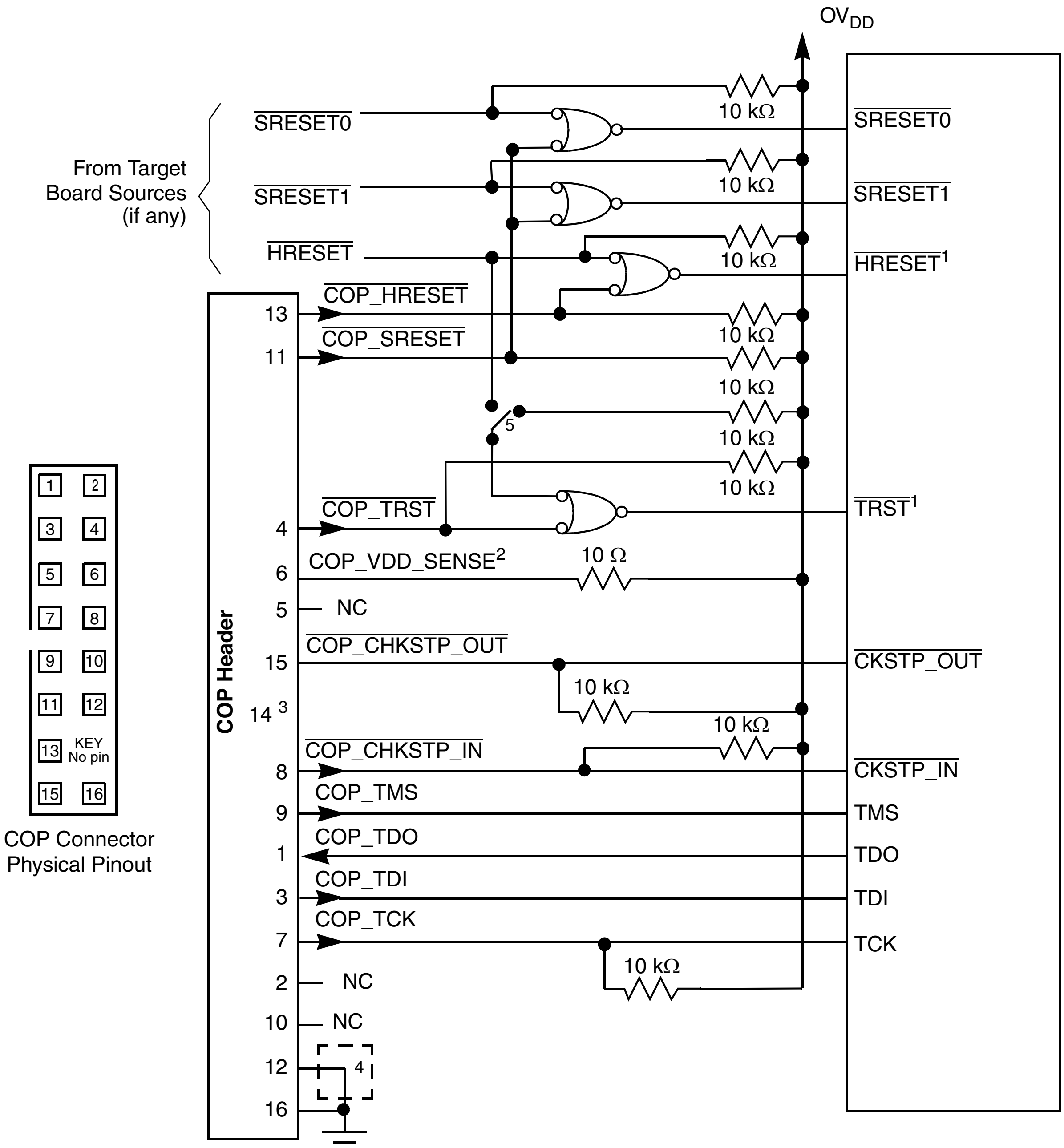
- AV_{DD}_SRDS*n* should be a filtered version of SV_{DD}.
- Signals on the SerDes interface are fed from the SV_{DD} power plan.

20.2.2 PLL Power Supply Sequencing

For details on power sequencing for the AV_{DD} type and supplies refer to Section 2.2, "Power Up/Down Sequence."

20.3 Decoupling Recommendations

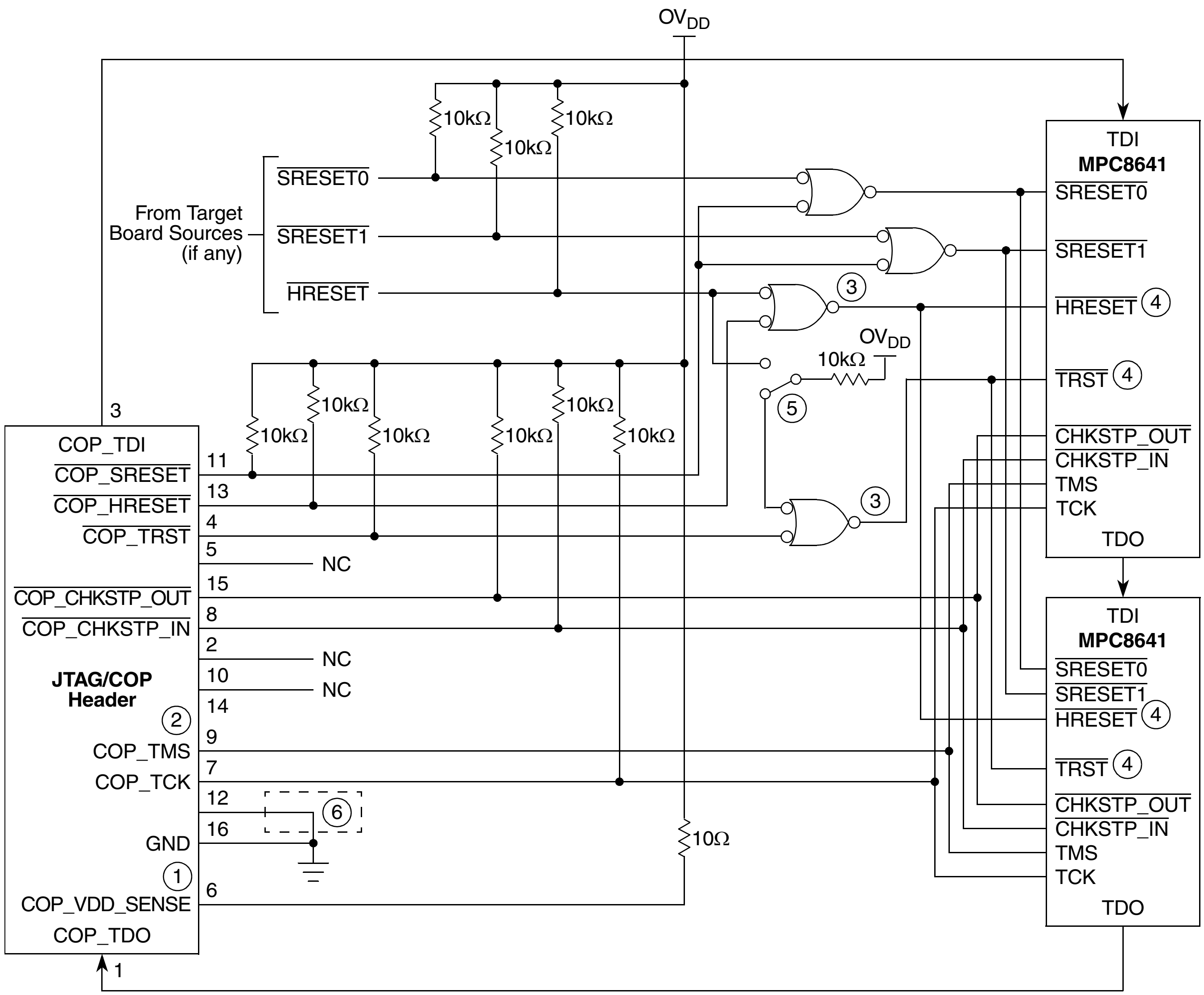
Due to large address and data buses, and high operating frequencies, the device can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the MPC8641 system, and the device itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system



Notes:

1. The COP port and target board should be able to independently assert HRESET and TRST to the processor in order to fully control the processor as shown here.
2. Populate this with a 10 Ω resistor for short-circuit/current-limiting protection.
3. The KEY location (pin 14) is not physically present on the COP header.
4. Although pin 12 is defined as a No-Connect, some debug tools may use pin 12 as an additional GND pin for improved signal integrity.
5. This switch is included as a precaution for BSDL testing. The switch should be open during BSDL testing to avoid accidentally asserting the TRST line. If BSDL testing is not being performed, this switch should be closed or removed.

Figure 68. JTAG/COP Interface Connection for one MPC8641 device



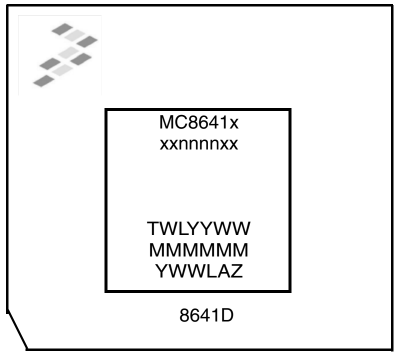
Notes:

1. Populate this with a 10Ω resistor for short circuit/current-limiting protection.
2. KEY location; pin 14 is not physically present on the COP header.
3. Use a AND gate with sufficient drive strength to drive two inputs.
4. The COP port and target board should be able to independently assert $\overline{\text{HRESET}}$ and $\overline{\text{TRST}}$ to the processor in order to fully control the processor as shown above.
5. This switch is included as a precaution for BSDL testing. The switch should be open during BSDL testing to avoid accidentally asserting the $\overline{\text{TRST}}$ line. If BSDL testing is not being performed, this switch should be closed or removed.
6. Although pin 12 is defined as a No-Connect, some debug tools may use pin 12 as an additional GND pin for improved signal integrity.

Figure 69. JTAG/COP Interface Connection for Multiple MPC8641 Devices in Daisy Chain Configuration

21.2 Part Marking

Parts are marked as the example shown in Figure 70.



NOTE:
TWLYYWW is the test code
MMMMMM is the M00 (mask) number.
YWWLAZ is the assembly traceability code.

Figure 70. Part Marking for FC-CBGA Device

22 Document Revision History

Table 76 provides a revision history for the MPC8641D hardware specification.

Table 76. Document Revision History

Revision	Date	Substantive Change(s)
3	05/2014	• Updated the Serial RapidIO equation in Section 4.4, "Platform Frequency Requirements for PCI-Express and Serial RapidIO" • Updated Section 19.2.4, "Temperature Diode," by removing the ideality factor value. • Added VJ package type designator and footnotes to Table 74, "Part Numbering Nomenclature" and Section 16.1, "Package Parameters for the MPC8641."
2	07/2009	• Added note 8 to Table 49, "Differential Transmitter (TX) Output Specifications." • Added Revision E to Table 74, "Part Numbering Nomenclature."
1	11/2008	• Added Section 4.4, "Platform Frequency Requirements for PCI-Express and Serial RapidIO." • Removed the statement "Note that core processor speed of 1500 MHz is only available for the MPC8641D (dual core)" from Note 2 in Table 74 because a 1500 MHz core is offered for both MPC8641D (dual core) and MPC8641 (single core). • Added Note 8 to Figure 57 and Figure 58.
0	07/2008	• Initial Release