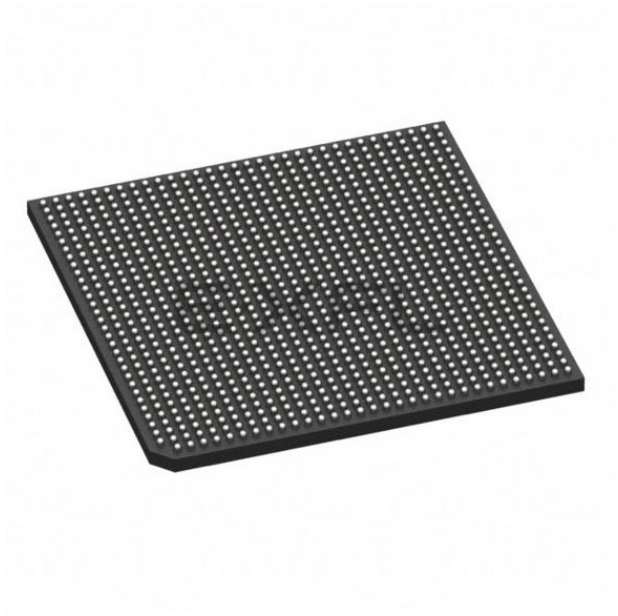

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e600
Number of Cores/Bus Width	2 Core, 32-Bit
Speed	1.0GHz
Co-Processors/DSP	-
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (4)
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	1023-BCBGA, FCCBGA
Supplier Device Package	1023-FCCBGA (33x33)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc8641dvu1000nb

Table 2. Recommended Operating Conditions (continued)

Characteristic	Symbol	Recommended Value	Unit	Notes
Junction temperature range	T_J	0 to 105	°C	—

Notes:

1. Core 1 characteristics apply only to MPC8641D
2. If two separate power supplies are used for V_{DD}_Core0 and V_{DD}_Core1, they must be at the same nominal voltage and the individual power supplies must be tracked and kept within 100 mV of each other during normal run time.
3. **Caution:** D*n*_MV_{IN} must meet the overshoot/undershoot requirements for D*n*_GV_{DD} as shown in Figure 2.
4. **Caution:** L/TV_{IN} must meet the overshoot/undershoot requirements for L/TV_{DD} as shown in Figure 2 during regular run time.
5. **Caution:** OV_{IN} must meet the overshoot/undershoot requirements for OV_{DD} as shown in Figure 2 during regular run time.
6. Timing limitations for M,L,T,O)V_{IN} and D*n*_MV_{REF} during regular run time is provided in Figure 2
7. Applies to devices marked with a core frequency of 1333 MHz and below. Refer to Table 74 Part Numbering Nomenclature to determine if the device has been marked for a core frequency of 1333 MHz and below.
8. Applies to devices marked with a core frequency above 1333 MHz. Refer to Table 74 Part Numbering Nomenclature to determine if the device has been marked for a core frequency above 1333 MHz.
9. The 2.5 V ± 125 mV range is for DDR and 1.8 V ± 90 mV range is for DDR2.
10. See Section 8.2, "FIFO, GMII, MII, TBI, RGMII, RMII, and RTBI AC Timing Specifications," for details on the recommended operating conditions per protocol.
11. The PCI Express interface of the device is expected to receive signals from 0.175 to 1.2 V. For more information refer to Section 14.4.3, "Differential Receiver (RX) Input Specifications."
12. Applies to Part Number MC8641xxx1000NX only. V_{DD}_Core*n* = 0.95 V and V_{DD}_PLAT = 1.05 V devices. Refer to Table 74 Part Numbering Nomenclature to determine if the device has been marked for V_{DD}_Core*n* = 0.95 V.
13. This voltage is the input to the filter discussed in Section 20.2, "Power Supply Design and Sequencing," and not necessarily the voltage at the AV_{DD}_Core*n* pin, which may be reduced from V_{DD}_Core*n* by the filter.

3 Power Characteristics

The power dissipation for the dual core MPC8641D device is shown in Table 4.

Table 4. MPC8641D Power Dissipation (Dual Core)

Power Mode	Core Frequency (MHz)	Platform Frequency (MHz)	V_{DD}_Coren, V_{DD}_PLAT (Volts)	Junction Temperature	Power (Watts)	Notes
Typical	1500 MHz	600 MHz	1.1 V	65 °C	32.1	1, 2
Thermal				105 °C	43.4	1, 3
Maximum					49.9	1, 4
Typical	1333 MHz	533 MHz	1.05 V	65 °C	23.9	1, 2
Thermal				105 °C	30.0	1, 3
Maximum					34.1	1, 4
Typical	1250 MHz	500 MHz	1.05 V	65 °C	23.9	1, 2
Thermal				105 °C	30.0	1, 3
Maximum					34.1	1, 4
Typical	1000 MHz	400 MHz	1.05 V	65 °C	23.9	1, 2
Thermal				105 °C	30.0	1, 3
Maximum					34.1	1, 4
Typical	1000 MHz	500 MHz	0.95 V, 1.05 V	65 °C	16.2	1, 2, 5
Thermal				105 °C	21.8	1, 3, 5
Maximum					25.0	1, 4, 5

Notes:

1. These values specify the power consumption at nominal voltage and apply to all valid processor bus frequencies and configurations. The values do not include power dissipation for I/O supplies.
2. Typical power is an average value measured at the nominal recommended core voltage (V_{DD}_Core*n*) and 65°C junction temperature (see Table 2)while running the Dhrystone 2.1 benchmark and achieving 2.3 Dhrystone MIPs/MHz with one core at 100% efficiency and the second core at 65% efficiency.
3. Thermal power is the average power measured at nominal core voltage (V_{DD}_Core*n*) and maximum operating junction temperature (see Table 2) while running the Dhrystone 2.1 benchmark and achieving 2.3 Dhrystone MIPs/MHz on both cores and a typical workload on platform interfaces.
4. Maximum power is the maximum power measured at nominal core voltage (V_{DD}_Core*n*) and maximum operating junction temperature (see Table 2) while running a test which includes an entirely L1-cache-resident, contrived sequence of instructions which keep all the execution units maximally busy on both cores.
5. These power numbers are for Part Number MC8641Dxx1000NX only. V_{DD}_Core*n* = 0.95 V and V_{DD}_PLAT = 1.05 V.

The maximum power dissipation for individual power supplies of the MPC8641D is shown in Table 5.

Table 5. MPC8641D Individual Supply Maximum Power Dissipation [1]

Component Description	Supply Voltage (Volts)	Power (Watts)	Notes
Per Core voltage Supply	V_{DD}_Core0/V_{DD}_Core1 = 1.1 V @ 1500 MHz	21.00	
Per Core PLL voltage supply	AV_{DD}_Core0/AV_{DD}_Core1 = 1.1 V @ 1500 MHz	0.0125	
Per Core voltage Supply	V_{DD}_Core0/V_{DD}_Core1 = 1.05 V @ 1333 MHz	17.00	
Per Core PLL voltage supply	AV_{DD}_Core0/AV_{DD}_Core1 = 1.05 V @ 1333 MHz	0.0125	
Per Core voltage Supply	V_{DD}_Core0/V_{DD}_Core1 = 0.95 V @ 1000 MHz	11.50	5
Per Core PLL voltage supply	AV_{DD}_Core0/AV_{DD}_Core1 = 0.95 V @ 1000 MHz	0.0125	5
DDR Controller I/O voltage supply	D*n*_GV_{DD} = 2.5 V @ 400 MHz	0.80	2
	D*n*_GV_{DD} = 1.8 V @ 533 MHz	0.68	2
	D*n*_GV_{DD} = 1.8 V @ 600 MHz	0.77	2
16-bit FIFO @ 200 MHz eTsec 1&2/3&4 Voltage Supply	L/TV_{DD} = 3.3 V	0.11	2, 3
non-FIFO eTsec*n* Voltage Supply	L/TV_{DD} = 3.3 V	0.08	2
x8 SerDes transceiver Supply	SV_{DD} = 1.1 V	0.70	2
x8 SerDes I/O Supply	XV_{DD}_SRDS*n* = 1.1 V	0.66	2
SerDes PLL voltage supply Port 1 or 2	AV_{DD}_SRDS1/AV_{DD}_SRDS2 = 1.1 V	0.10	
Platform I/O Supply	OV_{DD} = 3.3 V	0.45	4
Platform source Supply	V_{DD}_PLAT = 1.1 V @ 600 MHz	12.00	
Platform source Supply	V_{DD}_PLAT = 1.05 Vn @ 500 MHz	9.80	5
Platform source Supply	V_{DD}_PLAT = 1.05 Vn @ 400 MHz	7.70	
Platform, Local Bus PLL voltage Supply	AV_{DD}_PLAT, AV_{DD}_LB = 1.1 V	0.0125	

Notes:

1. This is a maximum power supply number which is provided for power supply and board design information. The numbers are based on 100% bus utilization for each component. The components listed are not expected to have 100% bus usage simultaneously for all components. Actual numbers may vary based on activity.
2. Number is based on a per port/interface value.
3. This is based on one eTSEC port used. Since 16-bit FIFO mode involves two ports, the number will need to be multiplied by two for the total. The other eTSEC protocols dissipate less than this number per port. Note that the power needs to be multiplied by the number of ports used for the protocol for the total eTSEC port power dissipation.
4. This includes Local Bus, DUART, I^2C, DMA, Multiprocessor Interrupts, System Control & Clocking, Debug, Test, Power management, JTAG and Miscellaneous I/O voltage.
5. These power numbers are for Part Number MC8641xxx1000NX only. V_{DD}_Core*n* = 0.95 V and V_{DD}_PLAT = 1.05 V.

Table 28. GMII Transmit AC Timing Specifications (continued)

At recommended operating conditions with L/TV_{DD} of 3.3 V ± 5% and 2.5 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
GTX_CLK data clock fall time (80%-20%)	t_{GTXF}[2]	—	—	1.0	ns

Notes:

1. The symbols used for timing specifications herein follow the pattern $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{GTKHDV} symbolizes GMII transmit timing (GT) with respect to the t_{GTX} clock reference (K) going to the high state (H) relative to the time date input signals (D) reaching the valid state (V) to state or setup time. Also, t_{GTKHDX} symbolizes GMII transmit timing (GT) with respect to the t_{GTX} clock reference (K) going to the high state (H) relative to the time date input signals (D) going invalid (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{GTX} represents the GMII(G) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Guaranteed by design.

Figure 10 shows the GMII transmit AC timing diagram.

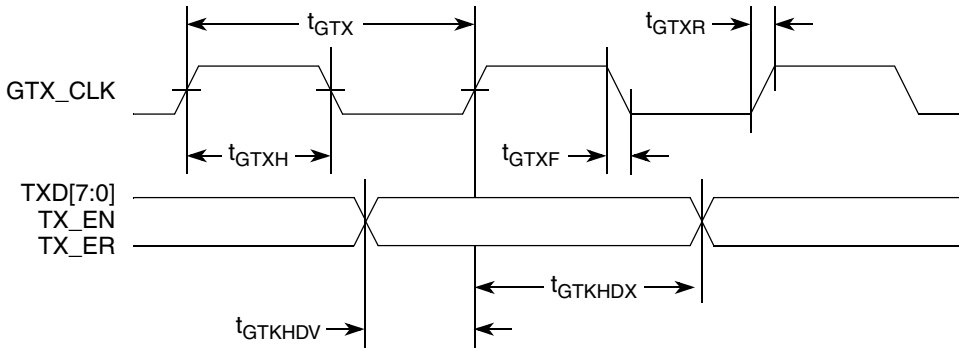

Figure 10. GMII Transmit AC Timing Diagram

8.2.2.2 GMII Receive AC Timing Specifications

Table 29 provides the GMII receive AC timing specifications.

Table 29. GMII Receive AC Timing Specifications

At recommended operating conditions with L/TV_{DD} of 3.3 V ± 5% and 2.5 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
RX_CLK clock period	t_{GRX}[3]	—	8.0	—	ns
RX_CLK duty cycle	t_{GRXH}/t_{GRX}	40	—	60	ns
RXD[7:0], RX_DV, RX_ER setup time to RX_CLK	t_{GRDVKH}	2.0	—	—	ns
RXD[7:0], RX_DV, RX_ER hold time to RX_CLK	t_{GRDXKH}	0.5	—	—	ns
RX_CLK clock rise time (20%-80%)	t_{GRXR}[2]	—	—	1.0	ns

Table 39. MII Management AC Timing Specifications (continued)

At recommended operating conditions with OV_{DD} is 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit	Notes
MDIO to MDC hold time	t_{MDDXKH}	0	—	—	ns	—
MDC rise time	t_{MDCR}	—	—	10	ns	4
MDC fall time	t_{MDHF}	—	—	10	ns	4

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. This parameter is dependent on the system clock speed. (The maximum frequency is the maximum platform frequency divided by 64.)
3. This parameter is dependent on the system clock speed. (That is, for a system clock of 267 MHz, the maximum frequency is 8.3 MHz and the minimum frequency is 1.2 MHz; for a system clock of 375 MHz, the maximum frequency is 11.7 MHz and the minimum frequency is 1.7 MHz.)
4. Guaranteed by design.
5. t_{MPXCLK} is the platform (MPX) clock

Figure 23 provides the AC test load for eTSEC.

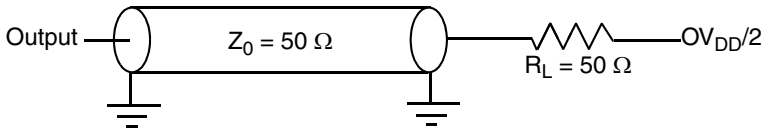

Figure 23. eTSEC AC Test Load

NOTE

Output will see a 50-Ω load since what it sees is the transmission line.

Figure 24 shows the MII management AC timing diagram.

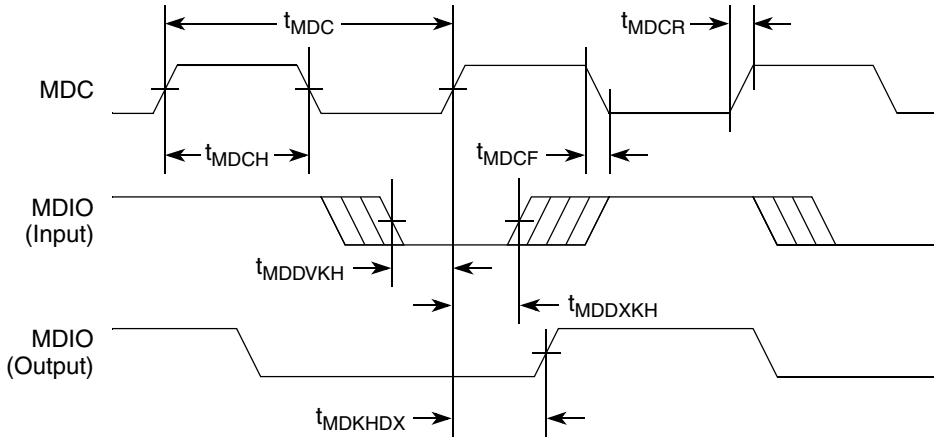

Figure 24. MII Management Interface Timing Diagram

Figure 26 to Figure 31 show the local bus signals.

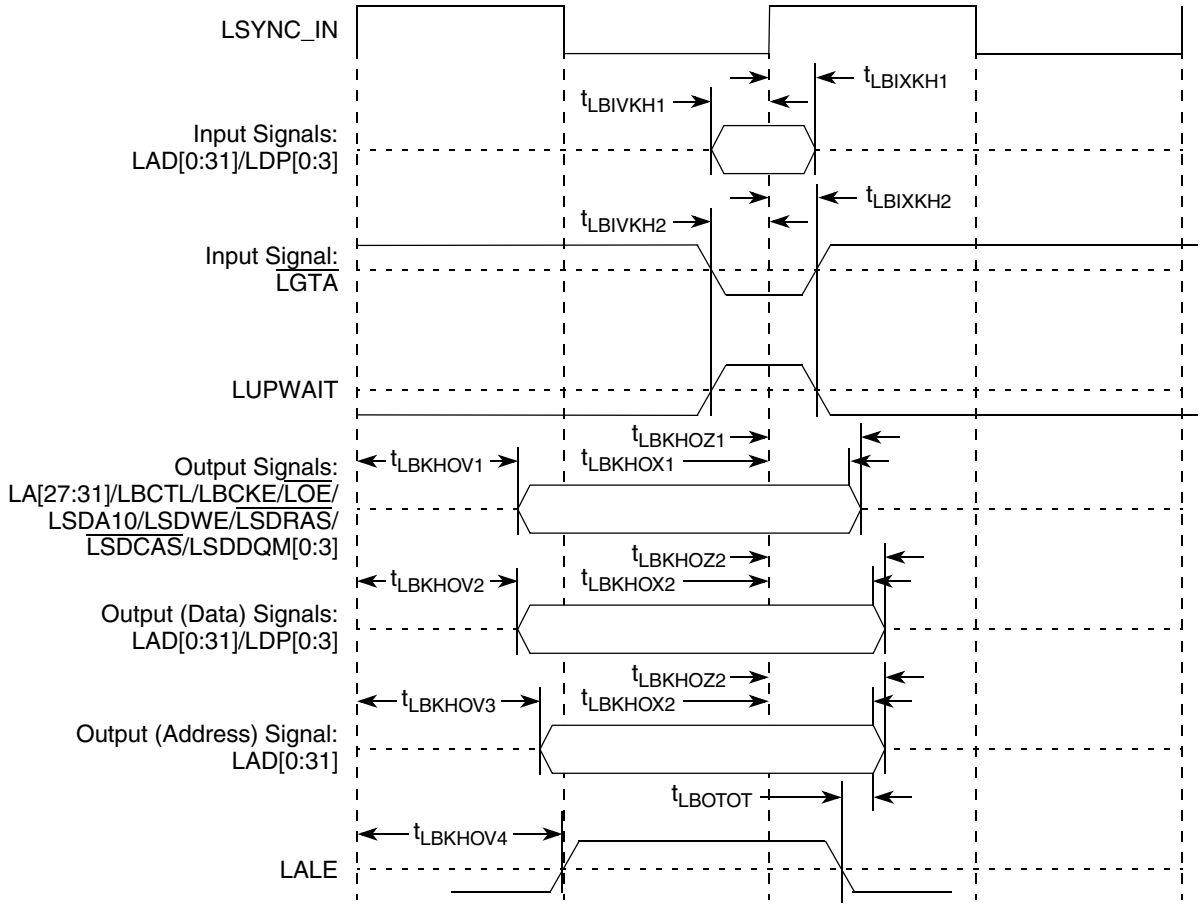

Figure 26. Local Bus Signals (PLL Enabled)

NOTE

PLL bypass mode is recommended when LBIU frequency is at or below 83 MHz. When LBIU operates above 83 MHz, LBIU PLL is recommended to be enabled.

Table 42 describes the general timing parameters of the local bus interface at OV_{DD} = 3.3 V with PLL bypassed.

Table 42. Local Bus Timing Parameters—PLL Bypassed

Parameter	Symbol [1]	Min	Max	Unit	Notes
Local bus cycle time	t_{LBK}	12	—	ns	2
Local bus duty cycle	t_{LBKH}/t_{LBK}	45	55	%	—
Internal launch/capture clock to LCLK delay	t_{LBKHKT}	2.3	3.9	ns	8
Input setup to local bus clock (except $\overline{\text{LGTA}}$/LUPWAIT)	$t_{LBIVKH1}$	5.7	—	ns	4, 5
$\overline{\text{LGTA}}$/LUPWAIT input setup to local bus clock	$t_{LBIVKL2}$	5.6	—	ns	4, 5
Input hold from local bus clock (except $\overline{\text{LGTA}}$/LUPWAIT)	$t_{LBIXKH1}$	–1.8	—	ns	4, 5

Table 42. Local Bus Timing Parameters—PLL Bypassed (continued)

Parameter	Symbol [1]	Min	Max	Unit	Notes
$\overline{\text{LGTA}}$/LUPWAIT input hold from local bus clock	$t_{LBIXKL2}$	–1.3	—	ns	4, 5
LALE output transition to LAD/LDP output transition (LATCH hold time)	t_{LBOTOT}	1.5	—	ns	6
Local bus clock to output valid (except LAD/LDP and LALE)	$t_{LBKLOV1}$	—	–0.3	ns	
Local bus clock to data valid for LAD/LDP	$t_{LBKLOV2}$	—	–0.1	ns	4
Local bus clock to address valid for LAD	$t_{LBKLOV3}$	—	0	ns	4
Local bus clock to LALE assertion	$t_{LBKLOV4}$	—	0	ns	4
Output hold from local bus clock (except LAD/LDP and LALE)	$t_{LBKLOX1}$	–3.2	—	ns	4
Output hold from local bus clock for LAD/LDP	$t_{LBKLOX2}$	–3.2	—	ns	4
Local bus clock to output high Impedance (except LAD/LDP and LALE)	$t_{LBKLOZ1}$	—	0.2	ns	7
Local bus clock to output high impedance for LAD/LDP	$t_{LBKLOZ2}$	—	0.2	ns	7

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(First two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(First two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one(1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to local bus clock for PLL bypass mode. Timings may be negative with respect to the local bus clock because the actual launch and capture of signals is done with the internal launch/capture clock, which precedes LCLK by t_{LBKHKT}.
3. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at $BV_{DD}/2$.
4. All signals are measured from BVDD/2 of the rising edge of local bus clock for PLL bypass mode to 0.4 x BVDD of the signal in question for 3.3-V signaling levels.
5. Input timings are measured at the pin.
6. The value of t_{LBOTOT} is the measurement of the minimum time between the negation of LALE and any change in LAD
7. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
8. Guaranteed by characterization.

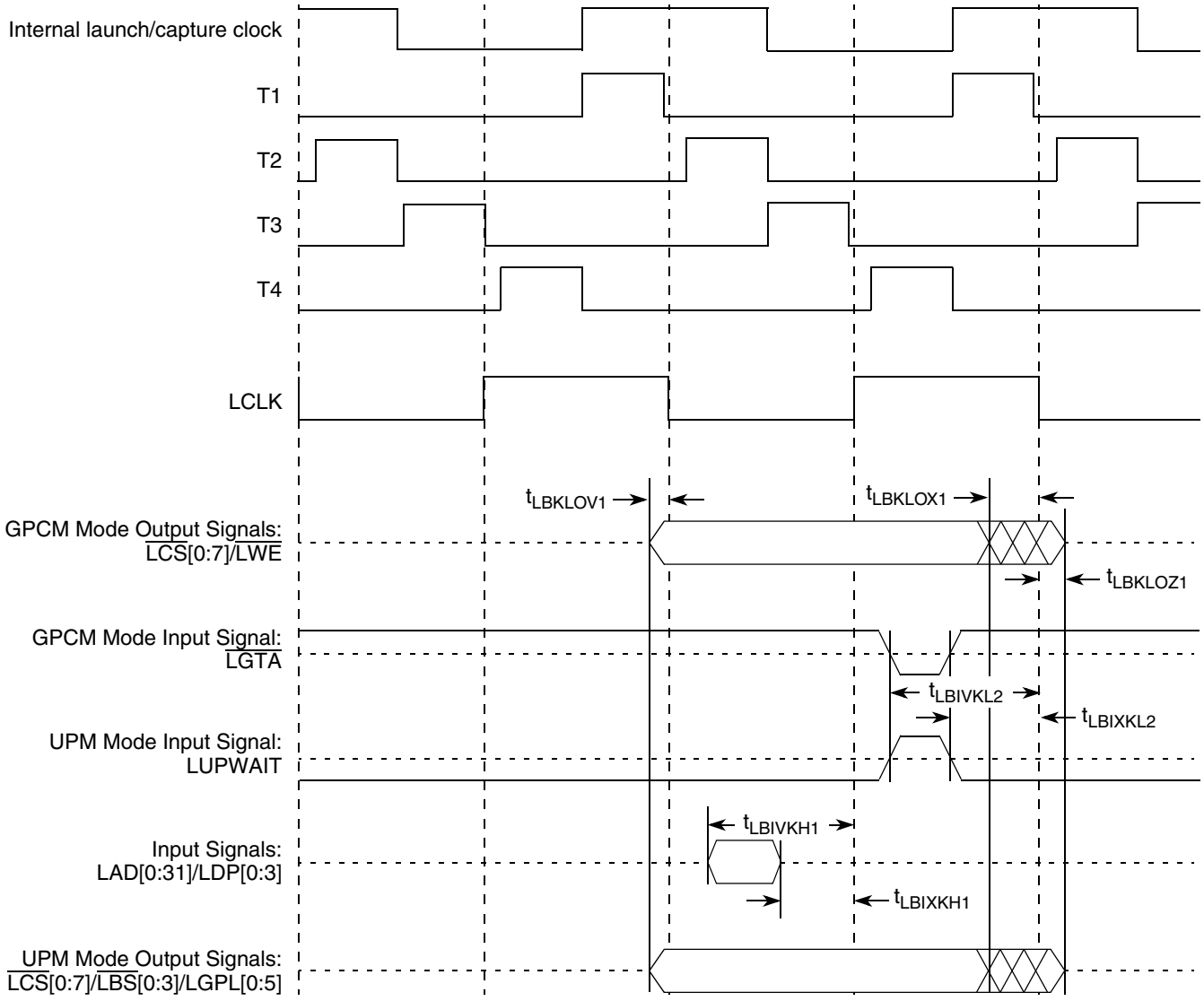

Figure 31. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 4 or 8 (clock ratio of 8 or 16) (PLL Bypass Mode)

— The SD*n*_REF_CLK input average voltage must be between 200 and 400 mV. Figure 42 shows the SerDes reference clock input requirement for single-ended signaling mode.

— To meet the input amplitude requirement, the reference clock inputs might need to be DC or AC-coupled externally. For the best noise performance, the reference of the clock could be DC or AC-coupled into the unused phase ($\overline{\text{SD}n\text{\_REF\_CLK}}$) through the same source impedance as the clock input (SD*n*_REF_CLK) in use.

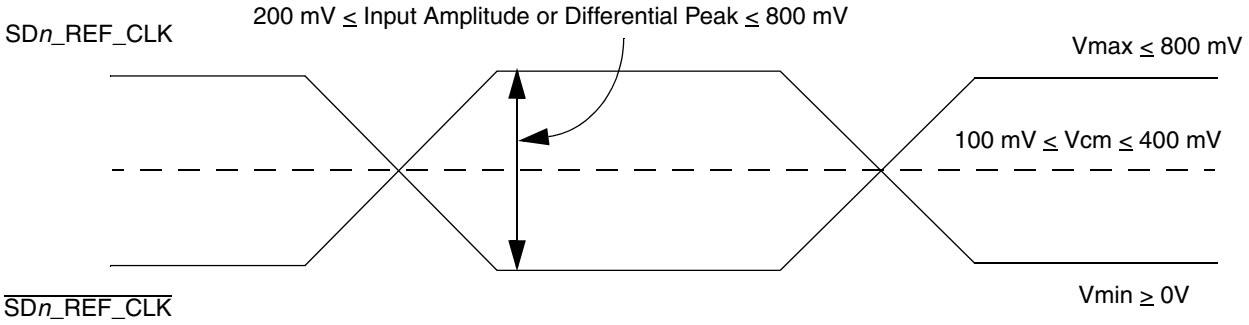

Figure 40. Differential Reference Clock Input DC Requirements (External DC-Coupled)

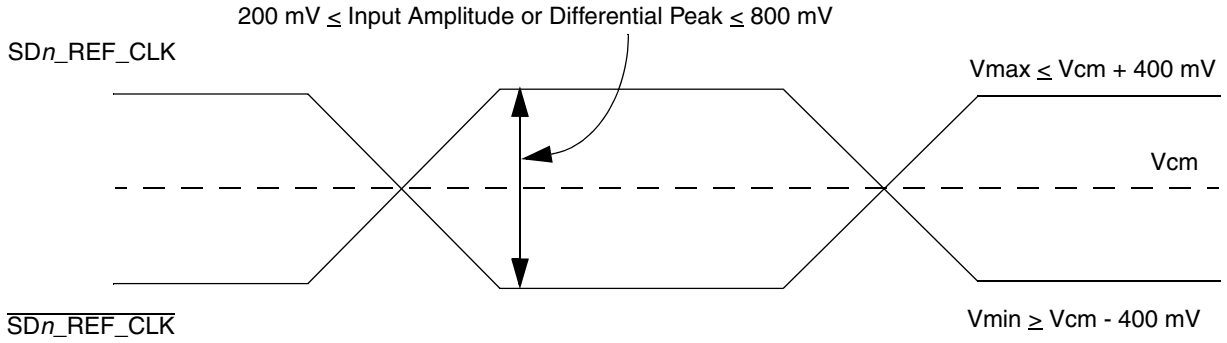

Figure 41. Differential Reference Clock Input DC Requirements (External AC-Coupled)

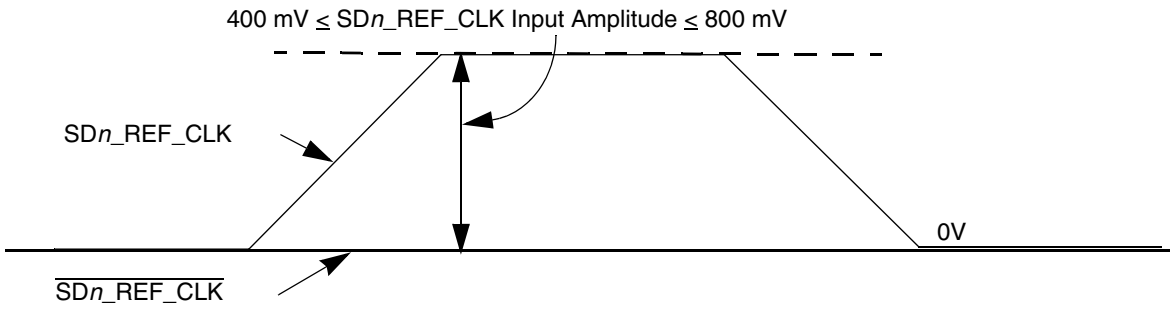

Figure 42. Single-Ended Reference Clock Input DC Requirements

14.1 DC Requirements for PCI Express SD*n*_REF_CLK and $\overline{\text{SD}n\text{\_REF\_CLK}}$

For more information, see Section 13.2, "SerDes Reference Clocks."

14.2 AC Requirements for PCI Express SerDes Clocks

Table 48 lists AC requirements.

Table 48. SD*n*_REF_CLK and $\overline{\text{SD}n\text{\_REF\_CLK}}$ AC Requirements

Symbol	Parameter Description	Min	Typical	Max	Units	Notes
t_{REF}	REFCLK cycle time	—	10	—	ns	—
t_{REFCJ}	REFCLK cycle-to-cycle jitter. Difference in the period of any two adjacent REFCLK cycles	—	—	100	ps	—
t_{REFPJ}	Phase jitter. Deviation in edge location with respect to mean edge location	–50	—	50	ps	—

14.3 Clocking Dependencies

The ports on the two ends of a link must transmit data at a rate that is within 600 parts per million (ppm) of each other at all times. This is specified to allow bit rate clock sources with a +/– 300 ppm tolerance.

14.4 Physical Layer Specifications

The following is a summary of the specifications for the physical layer of PCI Express on this device. For further details as well as the specifications of the Transport and Data Link layer please use the PCI EXPRESS Base Specification. REV. 1.0a document.

14.4.1 Differential Transmitter (TX) Output

Table 49 defines the specifications for the differential output at all transmitters (TXs). The parameters are specified at the component pins.

Table 49. Differential Transmitter (TX) Output Specifications

Symbol	Parameter	Min	Nom	Max	Units	Comments
UI	Unit Interval	399.88	400	400.12	ps	Each UI is 400 ps ± 300 ppm. UI does not account for Spread Spectrum Clock dictated variations. See Note 1.
$V_{TX\text{-}DIFFp\text{-}p}$	Differential Peak-to-Peak Output Voltage	0.8	—	1.2	V	$V_{TX\text{-}DIFFp\text{-}p} = 2*\lvert V_{TX\text{-}D+} - V_{TX\text{-}D-}\rvert$ See Note 2.
$V_{TX\text{-}DE\text{-}RATIO}$	De- Emphasized Differential Output Voltage (Ratio)	–3.0	–3.5	–4.0	dB	Ratio of the $V_{TX\text{-}DIFFp\text{-}p}$ of the second and following bits after a transition divided by the $V_{TX\text{-}DIFFp\text{-}p}$ of the first bit after a transition. See Note 2.

Table 49. Differential Transmitter (TX) Output Specifications (continued)

Symbol	Parameter	Min	Nom	Max	Units	Comments
T_{TX-EYE}	Minimum TX Eye Width	0.70	—	—	UI	The maximum Transmitter jitter can be derived as $T_{TX-MAX-JITTER}$ = 1 – T_{TX-EYE}= 0.3 UI. See Notes 2 and 3.
$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time between the jitter median and maximum deviation from the median.	—	—	0.15	UI	Jitter is defined as the measurement variation of the crossing points ($V_{TX-DIFFp-p}$ = 0 V) in relation to a recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI. See Notes 2 and 3.
$T_{TX-RISE}$, $T_{TX-FALL}$	D+/D– TX Output Rise/Fall Time	0.125	—	—	UI	See Notes 2 and 5
$V_{TX-CM-ACp}$	RMS AC Peak Common Mode Output Voltage	—	—	20	mV	$V_{TX-CM-ACp}$ = RMS(|V_{TXD+} + V_{TXD-}|/2 – $V_{TX-CM-DC}$) $V_{TX-CM-DC}$ = $DC_{(avg)}$ of |V_{TX-D+} + V_{TX-D-}|/2 See Note 2
$V_{TX-CM-DC-ACTIVE-IDLE-DELTA}$	Absolute Delta of DC Common Mode Voltage During L0 and Electrical Idle	0	—	100	mV	|$V_{TX-CM-DC\ (during\ L0)}$ – $V_{TX-CM-Idle-DC\ (During\ Electrical\ Idle)}$|<=100 mV $V_{TX-CM-DC}$ = $DC_{(avg)}$ of |V_{TX-D+} + V_{TX-D-}|/2 [L0] $V_{TX-CM-Idle-DC}$ = $DC_{(avg)}$ of |V_{TX-D+} + V_{TX-D-}|/2 [Electrical Idle] See Note 2.
$V_{TX-CM-DC-LINE-DELTA}$	Absolute Delta of DC Common Mode between D+ and D–	0	—	25	mV	|$V_{TX-CM-DC-D+}$ – $V_{TX-CM-DC-D-}$| <= 25 mV $V_{TX-CM-DC-D+}$ = $DC_{(avg)}$ of |V_{TX-D+}| $V_{TX-CM-DC-D-}$ = $DC_{(avg)}$ of |V_{TX-D-}| See Note 2.
$V_{TX-IDLE-DIFFp}$	Electrical Idle differential Peak Output Voltage	0	—	20	mV	$V_{TX-IDLE-DIFFp}$ = |$V_{TX-IDLE-D+}$ –$V_{TX-IDLE-D-}$| <= 20 mV See Note 2.
$V_{TX-RCV-DETECT}$	The amount of voltage change allowed during Receiver Detection	—	—	600	mV	The total amount of voltage change that a transmitter can apply to sense whether a low impedance Receiver is present. See Note 6.
$V_{TX-DC-CM}$	The TX DC Common Mode Voltage	0	—	3.6	V	The allowed DC Common Mode voltage under any conditions. See Note 6.
$I_{TX-SHORT}$	TX Short Circuit Current Limit	—	—	90	mA	The total current the Transmitter can provide when shorted to its ground
$T_{TX-IDLE-MIN}$	Minimum time spent in Electrical Idle	50	—	—	UI	Minimum time a Transmitter must be in Electrical Idle Utilized by the Receiver to start looking for an Electrical Idle Exit after successfully receiving an Electrical Idle ordered set

8. Note that for MPC8641 (single core) the solder balls for the following signals/pins are not populated in the package: VDD_Core1 (R16, R18, R20, T17, T19, T21, T23, U16, U18, U22, V17, V19, V21, V23, W16, W18, W20, W22, Y17, Y19, Y21, Y23, AA16, AA18, AA20, AA22, AB23, AC24) and SENSEVDD_Core1 (U20).

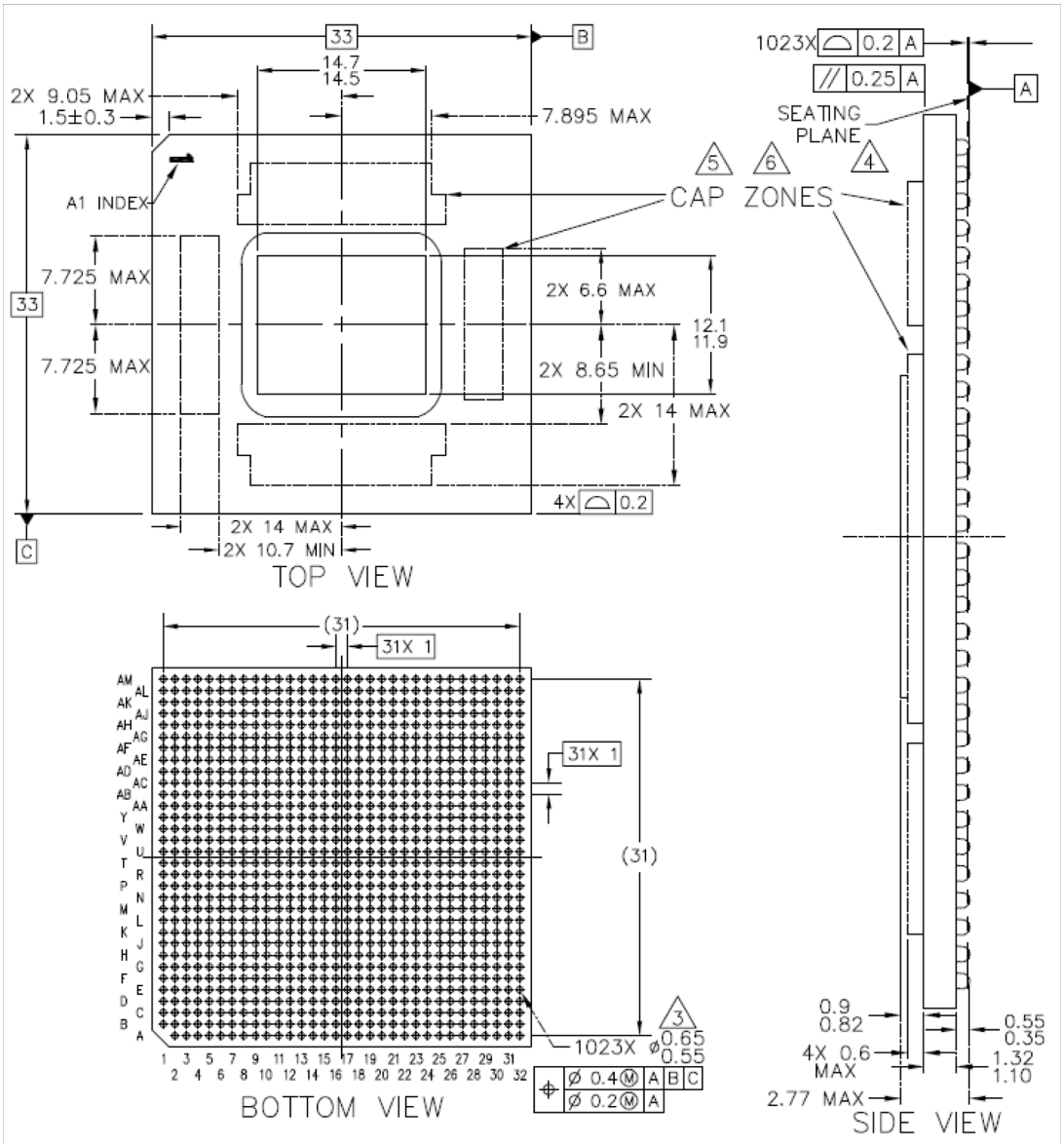

Figure 58. MPC8641D Lead-Free FC-CBGA Dimensions

NOTES for Figure 58

1. All dimensions are in millimeters.
2. Dimensions and tolerances per ASME Y14.5M-1994.
3. Maximum solder ball diameter measured parallel to datum A.
4. Datum A, the seating plane, is defined by the spherical crowns of the solder balls.
5. Capacitors may not be present on all devices.
6. Caution must be taken not to short capacitors or expose metal capacitor pads on package top.
7. All dimensions symmetrical about centerlines unless otherwise specified.
8. Note that for MPC8641 (single core) the solder balls for the following signals/pins are not populated in the package: VDD_Core1 (R16, R18, R20, T17, T19, T21, T23, U16, U18, U22, V17, V19, V21, V23, W16, W18, W20, W22, Y17, Y19, Y21, Y23, AA16, AA18, AA20, AA22, AB23, AC24) and SENSEVDD_Core1 (U20).

Table 63. MPC8641 Signal Reference by Functional Block (continued)

Name[1]	Package Pin Number	Pin Type	Power Supply	Notes
SD1_PLL_TPA	T28	Analog	SV_{DD}	13, 18
SD1_DLL_TPD	N28	O	SV_{DD}	13, 17
SD1_DLL_TPA	P31	Analog	SV_{DD}	13, 18
High Speed I/O Interface 2 (SERDES 2)[4]				
SD2_TX[0:3]	Y24, AA27, AB25, AC27	O	SV_{DD}	—
SD2_TX[4:7]	AE27, AG27, AJ27, AL27	O	SV_{DD}	34
$\overline{\text{SD2\_TX}}$[0:3]	Y25, AA28, AB26, AC28	O	SV_{DD}	—
$\overline{\text{SD2\_TX}}$[4:7]	AE28, AG28, AJ28, AL28	O	SV_{DD}	34
SD2_RX[0:3]	Y30, AA32, AB30, AC32	I	SV_{DD}	32
SD2_RX[4:7]	AH30, AJ32, AK30, AL32	I	SV_{DD}	32, 35
$\overline{\text{SD2\_RX}}$[0:3]	Y29, AA31, AB29, AC31	I	SV_{DD}	—
$\overline{\text{SD2\_RX}}$[4:7]	AH29, AJ31, AK29, AL31	I	SV_{DD}	35
SD2_REF_CLK	AE32	I	SV_{DD}	—
$\overline{\text{SD2\_REF\_CLK}}$	AE31	I	SV_{DD}	—
SD2_IMP_CAL_TX	AM29	Analog	SV_{DD}	19
SD2_IMP_CAL_RX	AA26	Analog	SV_{DD}	30
SD2_PLL_TPD	AF29	O	SV_{DD}	13, 17
SD2_PLL_TPA	AF31	Analog	SV_{DD}	13, 18
SD2_DLL_TPD	AD29	O	SV_{DD}	13, 17
SD2_DLL_TPA	AD30	Analog	SV_{DD}	13, 18
Special Connection Requirement pins				
No Connects	K24, K25, P28, P29, W26, W27, AD25, AD26	—	—	13
Reserved	H30, R32, V28, AG32	—	—	14
Reserved	H29, R31, W28, AG31	—	—	15
Reserved	AD24, AG26	—	—	16
Ethernet Miscellaneous Signals[5]				
EC1_GTX_CLK125	AL23	I	LV_{DD}	39
EC2_GTX_CLK125	AM23	I	TV_{DD}	39
EC_MDC	G31	O	OV_{DD}	—
EC_MDIO	G32	I/O	OV_{DD}	—
eTSEC Port 1 Signals[5]				

Table 63. MPC8641 Signal Reference by Functional Block (continued)

Name[1]	Package Pin Number	Pin Type	Power Supply	Notes
TSEC3_TX_EN	AH19	O	TV_{DD}	36
TSEC3_TX_ER	AH17	O	TV_{DD}	—
TSEC3_TX_CLK	AH18	I	TV_{DD}	40
TSEC3_GTX_CLK	AG19	O	TV_{DD}	41
TSEC3_CRS	AE15	I/O	TV_{DD}	37
TSEC3_COL	AF15	I	TV_{DD}	—
TSEC3_RXD[0:7]	AJ17, AE16, AH16, AH14, AJ19, AH15, AG16, AE19	I	TV_{DD}	—
TSEC3_RX_DV	AG15	I	TV_{DD}	—
TSEC3_RX_ER	AF16	I	TV_{DD}	—
TSEC3_RX_CLK	AJ18	I	TV_{DD}	40
eTSEC Port 4 Signals[5]				
TSEC4_TXD[0:3]	AC18, AC16, AD18, AD17	O	TV_{DD}	6
TSEC4_TXD[4]	AD16	O	TV_{DD}	25
TSEC4_TXD[5:7]	AB18, AB17, AB16	O	TV_{DD}	6
TSEC4_TX_EN	AF17	O	TV_{DD}	36
TSEC4_TX_ER	AF19	O	TV_{DD}	—
TSEC4_TX_CLK	AF18	I	TV_{DD}	40
TSEC4_GTX_CLK	AG17	O	TV_{DD}	41
TSEC4_CRS	AB14	I/O	TV_{DD}	37
TSEC4_COL	AC13	I	TV_{DD}	—
TSEC4_RXD[0:7]	AG14, AD13, AF13, AD14, AE14, AB15, AC14, AE17	I	TV_{DD}	—
TSEC4_RX_DV	AC15	I	TV_{DD}	—
TSEC4_RX_ER	AF14	I	TV_{DD}	—
TSEC4_RX_CLK	AG13	I	TV_{DD}	40
Local Bus Signals[5]				
LAD[0:31]	A30, E29, C29, D28, D29, H25, B29, A29, C28, L22, M22, A28, C27, H26, G26, B27, B26, A27, E27, G25, D26, E26, G24, F27, A26, A25, C25, H23, K22, D25, F25, H22	I/O	OV_{DD}	6
LDP[0:3]	A24, E24, C24, B24	I/O	OV_{DD}	6, 22
LA[27:31]	J21, K21, G22, F24, G21	O	OV_{DD}	6, 22
$\overline{\text{LCS}}$[0:4]	A22, C22, D23, E22, A23	O	OV_{DD}	7
$\overline{\text{LCS}}$[5]/$\overline{\text{DMA\_DREQ}}$[2]	B23	O	OV_{DD}	7, 9, 10

Table 63. MPC8641 Signal Reference by Functional Block (continued)

Name[1]	Package Pin Number	Pin Type	Power Supply	Notes
XV_{DD}_SRDS2	AA25, AB28, AC26, AD27, AE25, AF28, AH27, AK28, AM27, W24, Y27	Serial I/O Power Supply for SerDes Port 2	XV_{DD}_SRDS2 1.05/1.1 V	—
V_{DD}_Core0	L12, L13, L14, M13, M15, N12, N14, P11, P13, P15, R12, R14, T11, T13, T15, U12, U14, V11, V13, V15, W12, W14, Y12, Y13, Y15, AA12, AA14, AB13	Core 0 voltage supply	V_{DD}_Core0 0.95/1.05/1.1 V	—
V_{DD}_Core1	R16, R18, R20, T17, T19, T21, T23, U16, U18, U22, V17, V19, V21, V23, W16, W18, W20, W22, Y17, Y19, Y21, Y23, AA16, AA18, AA20, AA22, AB23, AC24	Core 1 voltage supply	V_{DD}_Core1 0.95/1.05/1.1 V	12, *S1*
V_{DD}_PLAT	M16, M17, M18, N16, N20, N22, P17, P19, P21, P23, R22	Platform supply voltage	V_{DD}_PLAT 1.05/1.1 V	—
AV_{DD}_Core0	B20	Core 0 PLL Supply	AV_{DD}_Core0 0.95/1.05/1.1 V	—
AV_{DD}_Core1	A19	Core 1 PLL Supply	AV_{DD}_Core1 0.95/1.05/1.1 V	12, *S2*
AV_{DD}_PLAT	B19	Platform PLL supply voltage	AV_{DD}_PLAT 1.05/1.1 V	—
AV_{DD}_LB	A20	Local Bus PLL supply voltage	AV_{DD}_LB 1.05/1.1 V	—
AV_{DD}_SRDS1	P32	SerDes Port 1 PLL & DLL Power Supply	AV_{DD}_SRDS1 1.05/1.1 V	—
AV_{DD}_SRDS2	AF32	SerDes Port 2 PLL & DLL Power Supply	AV_{DD}_SRDS2 1.05/1.1 V	—
GND	C3, C6, C9, C12, C15, C23, C26, E5, E8, E11, E14, E18, E25, E28, F3, G7, G10, G13, G20, G23, G27, G30, H5, J3, J9, J12, J15, J22, J25, K7, L5, L20, M3, M9, M12, N7, N11, N13, N15, N17, N19, N21, N23, P5, P12, P16, P20, P22, R3, R9, R11, R13, R15, R17, R19, R21, R23, T7, T12, T14, T16, T18, T20, T22, U5, U11,U13, U15, U17, U19, U21, U23, V3, V9, V12, V14, V16, V18, V22, W7, W11, W13, W15, W17, W19, W21, W23,Y5, Y14, Y16, Y18, Y20, Y22, AA3, AA9, AA13, AA15, AA17, AA19, AA21, AA23, AB7, AB24, AC5, AC11, AD3, AD9, AD15, AE7, AE13, AE18, AF5, AF11, AF21, AF24, AG3, AG9, AH7, AH13, AJ5, AJ11, AK3, AK9, AK15, AK19, AK23, AL7, AL13	GND	—	—

Table 63. MPC8641 Signal Reference by Functional Block (continued)

Name[1]	Package Pin Number	Pin Type	Power Supply	Notes

37.This pin is only an output in FIFO mode when used as Rx Flow Control.

38.This pin functions as cfg_dram_type[0 or 1] at reset and MUST BE VALID BEFORE HRESET ASSERTION in device sleep mode.

39. Should be pulled to ground if unused (such as in FIFO, MII and RMII modes).

40. See Section 18.4.2, “Platform to FIFO Restrictions” for clock speed limitations for this pin when used in FIFO mode.

41. The phase between the output clocks TSEC1_GTX_CLK and TSEC2_GTX_CLK (ports 1 and 2) is no more than 100 ps. The phase between the output clocks TSEC3_GTX_CLK and TSEC4_GTX_CLK (ports 3 and 4) is no more than 100 ps.

42. For systems which boot from Local Bus (GPCM)-controlled flash, a pullup on LGPL4 is required.

Special Notes for Single Core Device:

S1. Solder ball for this signal will not be populated in the single core package.

S2. The PLL filter from V_{DD}_Core1 to AV_{DD}_Core1 should be removed. AV_{DD}_Core1 should be pulled to ground with a weak (2–10 kΩ) resistor. See Section 20.2.1, “PLL Power Supply Filtering” for more details.

S3. This pin should be pulled to GND for the single core device.

S4. No special requirement for this pin on single core device. Pin should be tied to power supply as directed for dual core.

18 Clocking

This section describes the PLL configuration of the MPC8641. Note that the platform clock is identical to the MPX clock.

18.1 Clock Ranges

Table 64 provides the clocking specifications for the processor cores and Table 65 provides the clocking specifications for the memory bus. Table 66 provides the clocking for the Platform/MPX bus and Table 67 provides the clocking for the Local bus.

Table 64. Processor Core Clocking Specifications

Characteristic	Maximum Processor Core Frequency								Unit	Notes
	1000 MHz		1250MHz		1333MHz		1500 MHz			
	Min	Max	Min	Max	Min	Max	Min	Max		
e600 core processor frequency	800	1000	800	1250	800	1333	800	1500	MHz	1, 2

Notes:

1. **Caution:** The MPX clock to SYSCLK ratio and e600 core to MPX clock ratio settings must be chosen such that the resulting SYSCLK frequency, e600 (core) frequency, and MPX clock frequency do not exceed their respective maximum or minimum operating frequencies. Refer to Section 18.2, “MPX to SYSCLK PLL Ratio,” and Section 18.3, “e600 to MPX clock PLL Ratio,” for ratio settings.
2. The minimum e600 core frequency is based on the minimum platform clock frequency of 400 MHz.

19.2.2 Thermal Interface Materials

A thermal interface material is recommended at the package-to-heat sink interface to minimize the thermal contact resistance. Figure 61 shows the thermal performance of three thin-sheet thermal-interface materials (silicone, graphite/oil, floroether oil), a bare joint, and a joint with thermal grease as a function of contact pressure. As shown, the performance of these thermal interface materials improves with increasing contact pressure. The use of thermal grease significantly reduces the interface thermal resistance. That is, the bare joint results in a thermal resistance approximately seven times greater than the thermal grease joint.

Often, heat sinks are attached to the package by means of a spring clip to holes in the printed-circuit board (see Figure 59). Therefore, synthetic grease offers the best thermal performance, considering the low interface pressure, and is recommended due to the high power dissipation of the MPC8641. Of course, the selection of any thermal interface material depends on many factors—thermal performance requirements, manufacturability, service temperature, dielectric properties, cost, and so on.

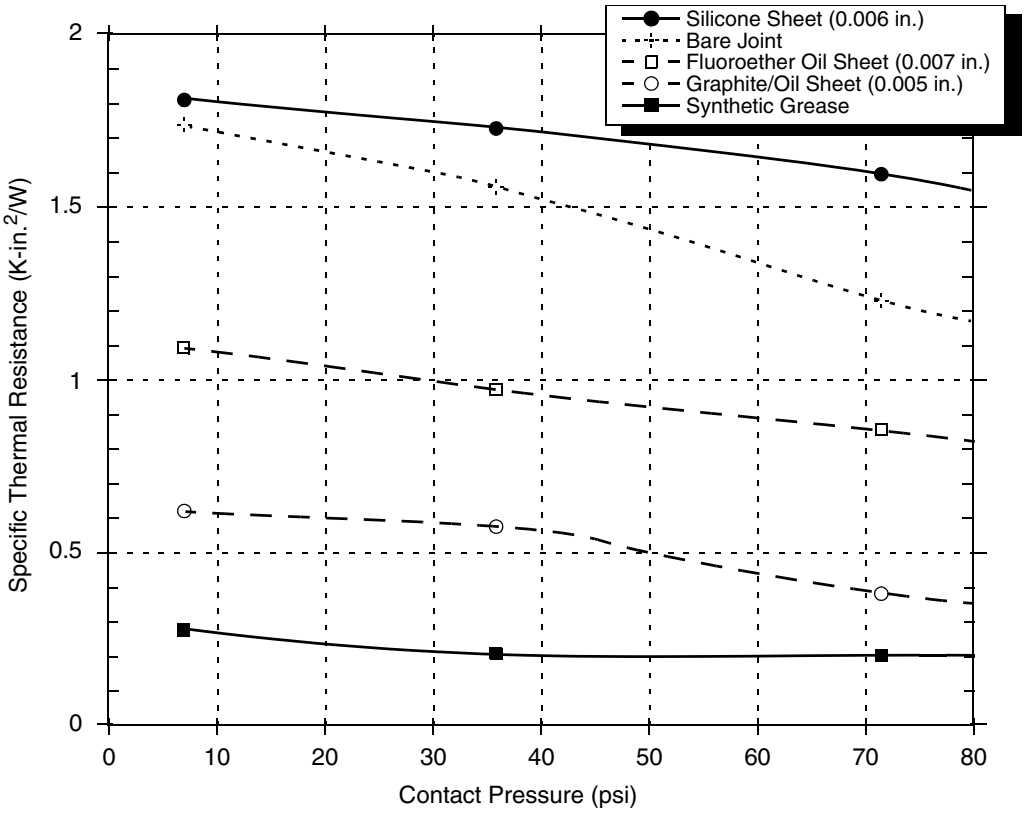

Figure 61. Thermal Performance of Select Thermal Interface Material

The board designer can choose between several types of thermal interface. Heat sink adhesive materials should be selected based on high conductivity and mechanical strength to meet equipment shock/vibration requirements. There are several commercially available thermal interfaces and adhesive materials provided by the following vendors:

The Bergquist Company 18930 West 78th St. Chanhassen, MN 55317 Internet: www.bergquistcompany.com	800-347-4572
Chomerics, Inc. 77 Dragon Ct. Woburn, MA 01801 Internet: www.chomerics.com	781-935-4850
Dow-Corning Corporation Corporate Center PO Box 994 Midland, MI 48686-0994 Internet: www.dowcorning.com	800-248-2481
Shin-Etsu MicroSi, Inc. 10028 S. 51st St. Phoenix, AZ 85044 Internet: www.microsi.com	888-642-7674
Thermagon Inc. 4707 Detroit Ave. Cleveland, OH 44102 Internet: www.thermagon.com	888-246-9050

The following section provides a heat sink selection example using one of the commercially available heat sinks.

19.2.3 Heat Sink Selection Example

For preliminary heat sink sizing, the die-junction temperature can be expressed as follows:

$$T_j = T_i + T_r + (R_{\theta JC} + R_{\theta int} + R_{\theta sa}) \times P_d$$

where:

T_j is the die-junction temperature
T_i is the inlet cabinet ambient temperature
T_r is the air temperature rise within the computer cabinet
$R_{\theta JC}$ is the junction-to-case thermal resistance
$R_{\theta int}$ is the adhesive or interface material thermal resistance
$R_{\theta sa}$ is the heat sink base-to-ambient thermal resistance
P_d is the power dissipated by the device

During operation, the die-junction temperatures (T_j) should be maintained less than the value specified in Table 2. The temperature of air cooling the component greatly depends on the ambient inlet air temperature and the air temperature rise within the electronic cabinet. An electronic cabinet inlet-air temperature (T_i) may range from 30° to 40°C. The air temperature rise within a cabinet (T_r) may be in the range of 5° to 10°C. The thermal resistance of the thermal interface material ($R_{\theta int}$) is typically about 0.2°C/W. For

The following pins must be connected to GND:

- SD*n*_RX[7:0]
- $\overline{\text{SD}n\text{\_RX}}$[7:0]
- SD*n*_REF_CLK
- $\overline{\text{SD}n\text{\_REF\_CLK}}$

NOTE

It is recommended to power down the unused lane through SRDS1CR1[0:7] register (offset = 0xE_0F08) and SRDS2CR1[0:7] register (offset = 0xE_0F44.) (This prevents the oscillations and holds the receiver output in a fixed state.) that maps to SERDES lane 0 to lane 7 accordingly.

For other directions on reserved or no-connects pins see Section 17, "Signal Listings."

20.6 Pull-Up and Pull-Down Resistor Requirements

The MPC8641 requires weak pull-up resistors (2–10 kΩ is recommended) on all open drain type pins.

The following pins must NOT be pulled down during power-on reset: TSEC4_TXD[4], LGPL0/LSDA10, LGPL1/$\overline{\text{LSDWE}}$, TRIG_OUT/READY, and D1_MSRCID[2].

The following are factory test pins and require strong pull up resistors (100 Ω –1 kΩ) to OVDD

LSSD_MODE, TEST_MODE[0:3].The following pins require weak pull up resistors (2–10 kΩ) to their specific power supplies: LCS[0:4], LCS[5]/DMA_DREQ2, LCS[6]/DMA_DACK[2], LCS[7]/DMA_DDONE[2], IRQ_OUT, IIC1_SDA, IIC1_SCL, IIC2_SDA, IIC2_SCL, and CKSTP_OUT.

The following pins should be pulled to ground with a 100-Ω resistor: SD1_IMP_CAL_TX, SD2_IMP_CAL_TX. The following pins should be pulled to ground with a 200-Ω resistor: SD1_IMP_CAL_RX, SD2_IMP_CAL_RX.

TSEC*n*_TX_EN signals require an external 4.7-kΩ pull down resistor to prevent PHY from seeing a valid Transmit Enable before it is actively driven.

When the platform frequency is 400 MHz, TSEC1_TXD[1] must be pulled down at reset.

TSEC2_TXD[4] and TSEC2_TX_ER pins function as cfg_dram_type[0 or 1] at reset and MUST BE VALID BEFORE HRESET ASSERTION when coming out of device sleep mode.

20.6.1 Special instructions for Single Core device

The mechanical drawing for the single core device does not have all the solder balls that exist on the single core device. This includes all the balls for VDD_Core1 and $\text{SENSEV}_{\text{DD}}$_Core1 which exist on the package for the dual core device, but not on the single core package. A solder ball is present for $\text{SENSEV}_{\text{SS}}$_Core1 and needs to be connected to ground with a weak (2-10 kΩ) pull down resistor. Likewise, AV_{DD}_Core1 needs to be pulled to ground as shown in Figure 64.

The mechanical drawing for the single core device is located in Section 16.2, "Mechanical Dimensions of the MPC8641 FC-CBGA."

21 Ordering Information

Ordering information for the parts fully covered by this specification document is provided in Section 21.1, "Part Numbers Fully Addressed by This Document."

21.1 Part Numbers Fully Addressed by This Document

Table 74 provides the Freescale part numbering nomenclature for the MPC8641. Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Freescale sales office. In addition to the processor frequency, the part numbering scheme also includes an application modifier which may specify special application conditions. Each part number also contains a revision code which refers to the die mask revision number.

Table 74. Part Numbering Nomenclature

MC	nnnn	x	xx	nnnn	x	x
Product Code	**Part Identifier**	**Core Count**	**Package [1]**	**Core Processor Frequency [2] (MHz)**	**DDR speed (MHz)**	**Product Revision Level**
MC	8641	Blank = Single Core D = Dual Core	HX = High-lead HCTE FC-CBGA VU = RoHS lead-free HCTE FC-CBGA[5] VJ = lead-free HCTE FC-CBGA[6]	1000, 1250, 1333, 1500	N = 500 MHz[4] K = 600 MHz J = 533 MHz H = 500 MHz G = 400 MHz	Revision B = 2.0 System Version Register Value for Rev B: 0x8090_0020 - MPC8641 0x8090_0120 - MPC8641D Revision C = 2.1 System Version Register Value for Rev C: 0x8090_0021 - MPC8641 0x8090_0121 - MPC8641D Revision E = 3.0 System Version Register Value for Rev E: 0x8090_0030 - MPC8641 0x8090_0130 - MPC8641D

Notes:

1. See Section 16, "Package," for more information on available package types.
2. Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by part number specifications may support other maximum core frequencies.
3. The P prefix in a Freescale part number designates a "Pilot Production Prototype" as defined by Freescale SOP 3-13. These parts have only preliminary reliability and characterization data. Before pilot production prototypes may be shipped, written authorization from the customer must be on file in the applicable sales office acknowledging the qualification status and the fact that product changes may still occur while shipping pilot production prototypes.
4. Part Number MC8641xxx1000NX is our low V_{DD}_Core*n* device. V_{DD}_Core*n* = 0.95 V and V_{DD}_PLAT = 1.05 V.
5. VU part number is RoHS compliant with the permitted exception of the C4 die bumps.
6. VJ part number is entirely lead-free including the C4 die bumps.