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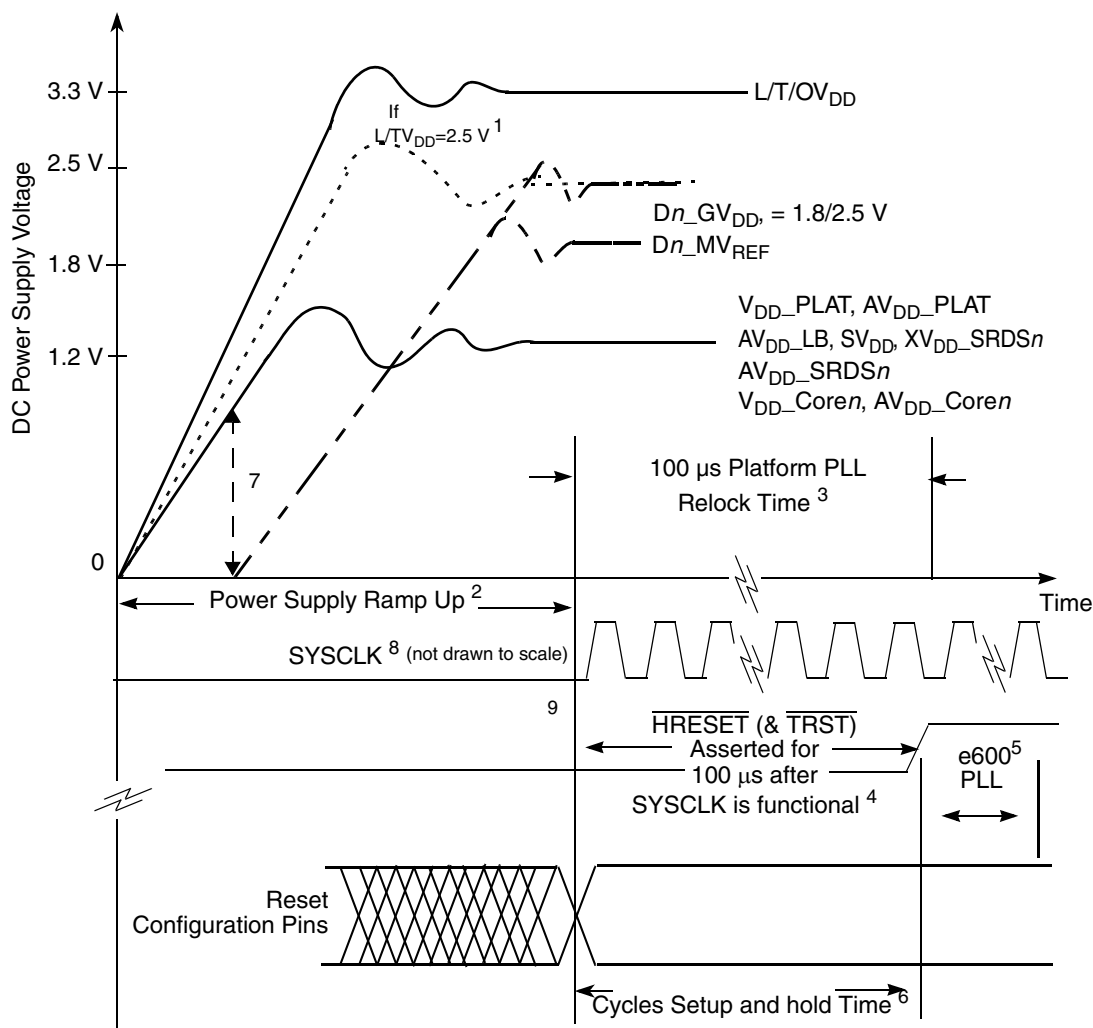
Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e600
Number of Cores/Bus Width	2 Core, 32-Bit
Speed	1.25GHz
Co-Processors/DSP	-
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (4)
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	1023-BCBGA, FCCBGA
Supplier Device Package	1023-FCCBGA (33x33)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc8641dvu1250hb

Figure 3 illustrates the Power Up sequence as described above.



Notes:

1. Dotted waveforms correspond to optional supply values for a specified power supply. See [Table 2](#).
2. The recommended maximum ramp up time for power supplies is 20 milliseconds.
3. Refer to [Section 5, "RESET Initialization"](#) for additional information on PLL relock and reset signal assertion timing requirements.
4. Refer to [Table 11](#) for additional information on reset configuration pin setup timing requirements. In addition see [Figure 68](#) regarding HRESET and JTAG connection details including TRST.
5. e600 PLL relock time is 100 microseconds maximum plus 255 MPX_clk cycles.
6. Stable PLL configuration signals are required as stable SYSCLK is applied. All other POR configuration inputs are required 4 SYSCLK cycles before HRESET negation and are valid at least 2 SYSCLK cycles after HRESET has negated (hold requirement). See [Section 5, "RESET Initialization"](#) for more information on setup and hold time of reset configuration signals.
7. V_{DD_PLAT}, AV_{DD_PLAT} must strictly reach 90% of their recommended voltage before the rail for D_{n_GV_DD}, and D_{n_MV_REF} reaches 10% of their recommended voltage.
8. SYSCLK must be driven only AFTER the power for the various power supplies is stable.
9. In device sleep mode, the reset configuration signals for DRAM types (TSEC2_TXD[4], TSEC2_TX_ER) must be valid BEFORE HRESET is asserted.

Figure 3. MPC8641 Power-Up and Reset Sequence

Figure 7 provides the AC test load for the DDR bus.

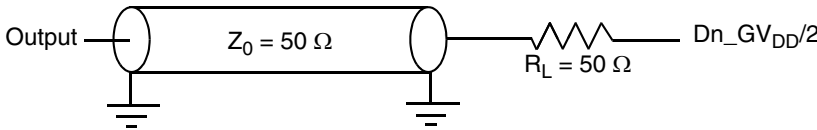


Figure 7. DDR AC Test Load

7 DUART

This section describes the DC and AC electrical specifications for the DUART interface of the MPC8641.

7.1 DUART DC Electrical Characteristics

Table 22 provides the DC electrical characteristics for the DUART interface.

Table 22. DUART DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	$OV_{DD} + 0.3$	V
Low-level input voltage	V_{IL}	-0.3	0.8	V
Input current ($V_{IN} = 0$ V or $V_{IN} = V_{DD}$)	I_{IN}	—	± 5	μA
High-level output voltage ($OV_{DD} = \text{min}$, $I_{OH} = -100 \mu A$)	V_{OH}	$OV_{DD} - 0.2$	—	V
Low-level output voltage ($OV_{DD} = \text{min}$, $I_{OL} = 100 \mu A$)	V_{OL}	—	0.2	V

Note:

- Note that the symbol V_{IN} , in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

7.2 DUART AC Electrical Specifications

Table 23 provides the AC timing parameters for the DUART interface.

Table 23. DUART AC Timing Specifications

Parameter	Value	Unit	Notes
Minimum baud rate	MPX clock/1,048,576	baud	1,2
Maximum baud rate	MPX clock/16	baud	1,3
Oversample rate	16	—	1,4

Notes:

- Guaranteed by design.
- MPX clock refers to the platform clock.
- Actual attainable baud rate will be limited by the latency of interrupt processing.
- The middle of a start bit is detected as the 8th sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16th sample.

Table 29. GMII Receive AC Timing Specifications (continued)

At recommended operating conditions with L/TV_{DD} of $3.3\text{ V} \pm 5\%$ and $2.5\text{ V} \pm 5\%$.

Parameter/Condition	Symbol ¹	Min	Typ	Max	Unit
RX_CLK clock fall time (80%-20%)	t_{GRXF}^2	—	—	1.0	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{GRDVKH} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{RX} clock reference (K) going to the high state (H) or setup time. Also, t_{GRDXKL} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{GRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{GRX} represents the GMII (G) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Guaranteed by design.
3. ± 100 ppm tolerance on RX_CLK frequency

Figure 11 provides the AC test load for eTSEC.

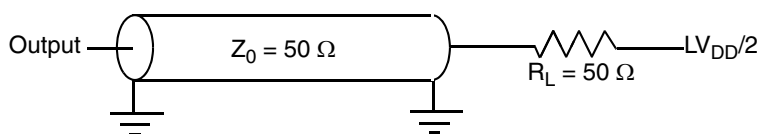


Figure 11. eTSEC AC Test Load

Figure 12 shows the GMII receive AC timing diagram.

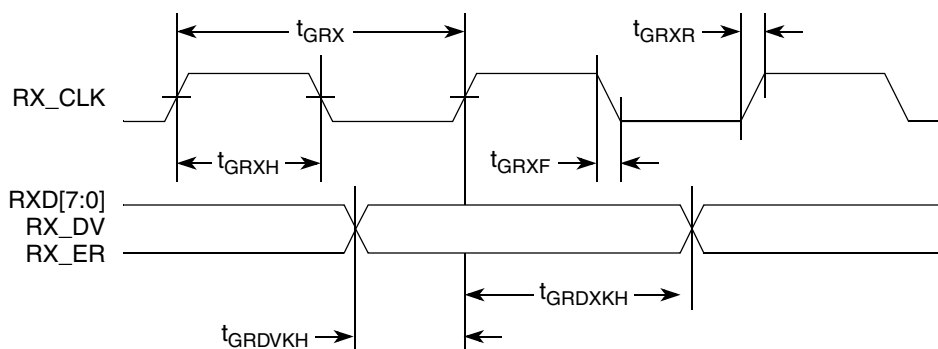


Figure 12. GMII Receive AC Timing Diagram

8.2.3.2 MII Receive AC Timing Specifications

Table 31 provides the MII receive AC timing specifications.

Table 31. MII Receive AC Timing Specifications

At recommended operating conditions with L/TV_{DD} of $3.3\text{ V} \pm 5\%$.

Parameter/Condition	Symbol ¹	Min	Typ	Max	Unit
RX_CLK clock period 10 Mbps	$t_{MRX}^{2,3}$	—	400	—	ns
RX_CLK clock period 100 Mbps	t_{MRX}^3	—	40	—	ns
RX_CLK duty cycle	t_{MRXH}/t_{MRX}	35	—	65	%
RXD[3:0], RX_DV, RX_ER setup time to RX_CLK	t_{MRDVKH}	10.0	—	—	ns
RXD[3:0], RX_DV, RX_ER hold time to RX_CLK	t_{MRDXKH}	10.0	—	—	ns
RX_CLK clock rise time (20%-80%)	t_{MRXR}^2	1.0	—	4.0	ns
RX_CLK clock fall time (80%-20%)	t_{MRXF}^2	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)\ (reference)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Guaranteed by design.
3. ± 100 ppm tolerance on RX_CLK frequency

Figure 14 provides the AC test load for eTSEC.

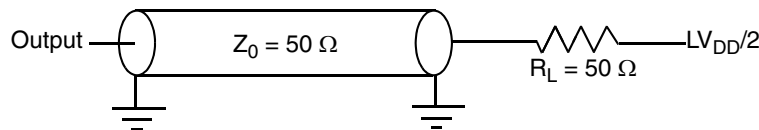


Figure 14. eTSEC AC Test Load

Figure 15 shows the MII receive AC timing diagram.

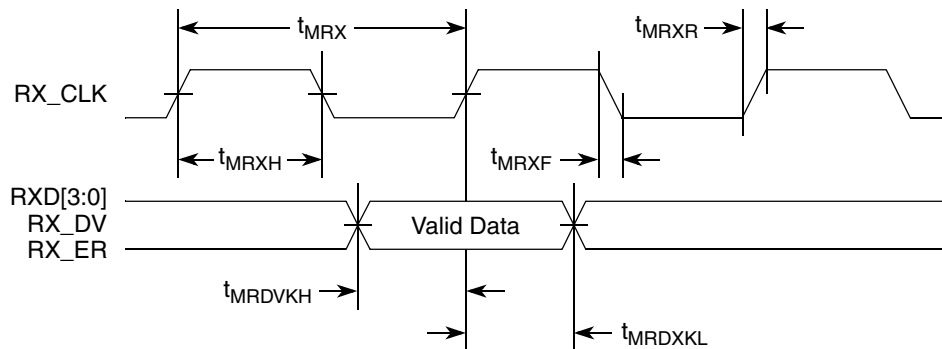


Figure 15. MII Receive AC Timing Diagram

10 Local Bus

This section describes the DC and AC electrical specifications for the local bus interface of the MPC8641.

10.1 Local Bus DC Electrical Characteristics

Table 40 provides the DC electrical characteristics for the local bus interface operating at $OV_{DD} = 3.3$ V DC.

Table 40. Local Bus DC Electrical Characteristics (3.3 V DC)

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	$OV_{DD} + 0.3$	V
Low-level input voltage	V_{IL}	-0.3	0.8	V
Input current ($V_{IN}^1 = 0$ V or $V_{IN} = OV_{DD}$)	I_{IN}	—	± 5	μA
High-level output voltage ($OV_{DD} = \min$, $I_{OH} = -2$ mA)	V_{OH}	$OV_{DD} - 0.2$	—	V
Low-level output voltage ($OV_{DD} = \min$, $I_{OL} = 2$ mA)	V_{OL}	—	0.2	V

Note:

- Note that the symbol V_{IN} , in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

10.2 Local Bus AC Electrical Specifications

Table 41 describes the timing parameters of the local bus interface at $OV_{DD} = 3.3$ V with PLL enabled. For information about the frequency range of local bus see Section 18.1, “Clock Ranges.”

Table 41. Local Bus Timing Parameters ($OV_{DD} = 3.3$ V)m - PLL Enabled

Parameter	Symbol ¹	Min	Max	Unit	Notes
Local bus cycle time	t_{LBK}	7.5	—	ns	2
Local Bus Duty Cycle	t_{LBKH}/t_{LBK}	45	55	%	—
LCLK[n] skew to LCLK[m] or LSYNC_OUT	$t_{LBKSKEW}$	—	150	ps	7, 8
Input setup to local bus clock (except $\overline{LGTA}/LUPWAIT$)	$t_{LBIVKH1}$	1.8	—	ns	3, 4
$\overline{LGTA}/LUPWAIT$ input setup to local bus clock	$t_{LBIVKH2}$	1.7	—	ns	3, 4
Input hold from local bus clock (except $\overline{LGTA}/LUPWAIT$)	$t_{LBIXKH1}$	1.0	—	ns	3, 4
$\overline{LGTA}/LUPWAIT$ input hold from local bus clock	$t_{LBIXKH2}$	1.0	—	ns	3, 4
LALE output transition to LAD/LDP output transition (LATCH hold time)	t_{LBOTOT}	1.5	—	ns	6
Local bus clock to output valid (except LAD/LDP and LALE)	$t_{LBKHOV1}$	—	2.0	ns	—
Local bus clock to data valid for LAD/LDP	$t_{LBKHOV2}$	—	2.2	ns	—
Local bus clock to address valid for LAD	$t_{LBKHOV3}$	—	2.3	ns	—

Table 42. Local Bus Timing Parameters—PLL Bypassed (continued)

Parameter	Symbol ¹	Min	Max	Unit	Notes
$\overline{\text{LGTA}}/\text{LUPWAIT}$ input hold from local bus clock	t_{LBIXKL2}	−1.3	—	ns	4, 5
LALE output transition to LAD/LDP output transition (LATCH hold time)	t_{LBOTOT}	1.5	—	ns	6
Local bus clock to output valid (except LAD/LDP and LALE)	t_{LBKLOV1}	—	−0.3	ns	
Local bus clock to data valid for LAD/LDP	t_{LBKLOV2}	—	−0.1	ns	4
Local bus clock to address valid for LAD	t_{LBKLOV3}	—	0	ns	4
Local bus clock to LALE assertion	t_{LBKLOV4}	—	0	ns	4
Output hold from local bus clock (except LAD/LDP and LALE)	t_{LBKLOX1}	−3.2	—	ns	4
Output hold from local bus clock for LAD/LDP	t_{LBKLOX2}	−3.2	—	ns	4
Local bus clock to output high Impedance (except LAD/LDP and LALE)	t_{LBKLOZ1}	—	0.2	ns	7
Local bus clock to output high impedance for LAD/LDP	t_{LBKLOZ2}	—	0.2	ns	7

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{(\text{First two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{First two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{LBIXKH1} symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one(1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to local bus clock for PLL bypass mode. Timings may be negative with respect to the local bus clock because the actual launch and capture of signals is done with the internal launch/capture clock, which precedes LCLK by t_{LBKHK1} .
3. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at $\text{BV}_{\text{DD}}/2$.
4. All signals are measured from $\text{BV}_{\text{DD}}/2$ of the rising edge of local bus clock for PLL bypass mode to $0.4 \times \text{BV}_{\text{DD}}$ of the signal in question for 3.3-V signaling levels.
5. Input timings are measured at the pin.
6. The value of t_{LBOTOT} is the measurement of the minimum time between the negation of LALE and any change in LAD.
7. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
8. Guaranteed by characterization.

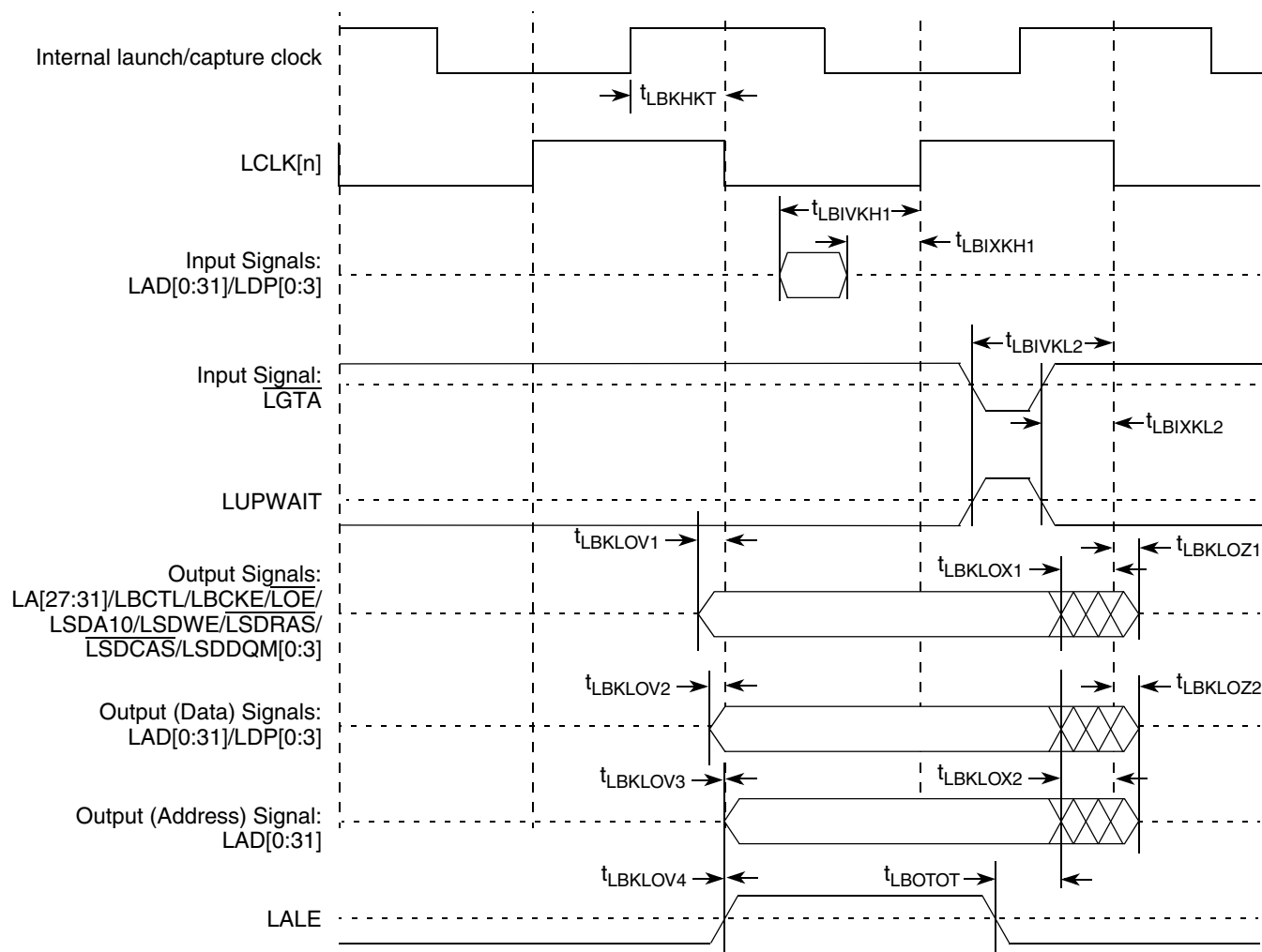


Figure 27. Local Bus Signals (PLL Bypass Mode)

NOTE

In PLL bypass mode, LCLK[n] is the inverted version of the internal clock with the delay of t_{LBKHK1} . In this mode, signals are launched at the rising edge of the internal clock and are captured at falling edge of the internal clock, with the exception of the LGTA/LUPWAIT signal, which is captured at the rising edge of the internal clock.

Figure 34 provides the $\overline{\text{TRST}}$ timing diagram.

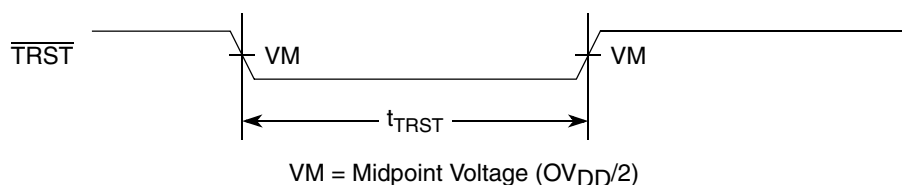


Figure 34. $\overline{\text{TRST}}$ Timing Diagram

Figure 35 provides the boundary-scan timing diagram.

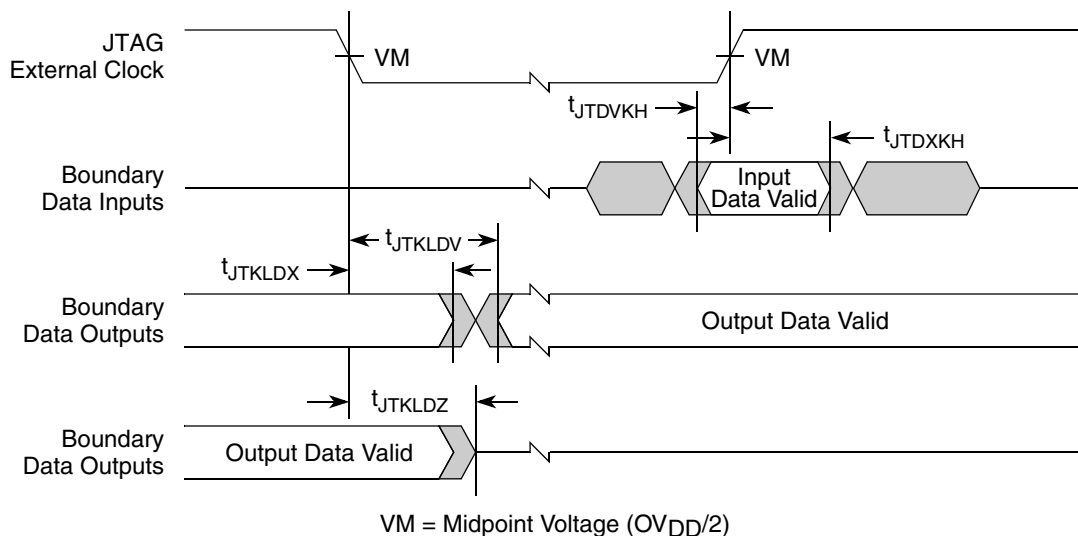


Figure 35. Boundary-Scan Timing Diagram

12 I²C

This section describes the DC and AC electrical characteristics for the I²C interfaces of the MPC8641.

12.1 I²C DC Electrical Characteristics

Table 45 provides the DC electrical characteristics for the I²C interfaces.

Table 45. I²C DC Electrical Characteristics

At recommended operating conditions with OV_{DD} of $3.3 \text{ V} \pm 5\%$.

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage level	V_{IH}	$0.7 \times \text{OV}_{\text{DD}}$	$\text{OV}_{\text{DD}} + 0.3$	V	—
Input low voltage level	V_{IL}	-0.3	$0.3 \times \text{OV}_{\text{DD}}$	V	—
Low level output voltage	V_{OL}	0	$0.2 \times \text{OV}_{\text{DD}}$	V	1
Pulse width of spikes which must be suppressed by the input filter	t_{i2KHKL}	0	50	ns	2
Input current each I/O pin (input voltage is between $0.1 \times \text{OV}_{\text{DD}}$ and $0.9 \times \text{OV}_{\text{DD}}$ (max))	I_{I}	-10	10	μA	3

Table 49. Differential Transmitter (TX) Output Specifications (continued)

Symbol	Parameter	Min	Nom	Max	Units	Comments
T_{TX-EYE}	Minimum TX Eye Width	0.70	—	—	UI	The maximum Transmitter jitter can be derived as $T_{TX-MAX-JITTER} = 1 - T_{TX-EYE} = 0.3 \text{ UI}$. See Notes 2 and 3.
$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time between the jitter median and maximum deviation from the median.	—	—	0.15	UI	Jitter is defined as the measurement variation of the crossing points ($V_{TX-DIFFp-p} = 0 \text{ V}$) in relation to a recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI. See Notes 2 and 3.
$T_{TX-RISE}, T_{TX-FALL}$	D+/D– TX Output Rise/Fall Time	0.125	—	—	UI	See Notes 2 and 5
$V_{TX-CM-ACp}$	RMS AC Peak Common Mode Output Voltage	—	—	20	mV	$V_{TX-CM-ACp} = \text{RMS}(IV_{TXD+} + V_{TXD-}/2 - V_{TX-CM-DC})$ $V_{TX-CM-DC} = DC_{(avg)} \text{ of } IV_{TXD+} + V_{TXD-}/2$ See Note 2
$V_{TX-CM-DC-ACTIVE-IDLE-DELTA}$	Absolute Delta of DC Common Mode Voltage During L0 and Electrical Idle	0	—	100	mV	$ V_{TX-CM-DC} \text{ (during L0)} - V_{TX-CM-DC} \text{ (During Electrical Idle)} \leq 100 \text{ mV}$ $V_{TX-CM-DC} = DC_{(avg)} \text{ of } IV_{TXD+} + V_{TXD-}/2 \text{ [L0]}$ $V_{TX-CM-DC} = DC_{(avg)} \text{ of } IV_{TXD+} + V_{TXD-}/2 \text{ [Electrical Idle]}$ See Note 2.
$V_{TX-CM-DC-LINE-DELTA}$	Absolute Delta of DC Common Mode between D+ and D–	0	—	25	mV	$ V_{TX-CM-DC-D+} - V_{TX-CM-DC-D-} \leq 25 \text{ mV}$ $V_{TX-CM-DC-D+} = DC_{(avg)} \text{ of } IV_{TXD+}$ $V_{TX-CM-DC-D-} = DC_{(avg)} \text{ of } IV_{TXD-}$ See Note 2.
$V_{TX-IDLE-DIFFp}$	Electrical Idle differential Peak Output Voltage	0	—	20	mV	$V_{TX-IDLE-DIFFp} = IV_{TX-IDLE-D+} - IV_{TX-IDLE-D-} \leq 20 \text{ mV}$ See Note 2.
$V_{TX-RCV-DETECT}$	The amount of voltage change allowed during Receiver Detection	—	—	600	mV	The total amount of voltage change that a transmitter can apply to sense whether a low impedance Receiver is present. See Note 6.
$V_{TX-DC-CM}$	The TX DC Common Mode Voltage	0	—	3.6	V	The allowed DC Common Mode voltage under any conditions. See Note 6.
$I_{TX-SHORT}$	TX Short Circuit Current Limit	—	—	90	mA	The total current the Transmitter can provide when shorted to its ground
$T_{TX-IDLE-MIN}$	Minimum time spent in Electrical Idle	50	—	—	UI	Minimum time a Transmitter must be in Electrical Idle Utilized by the Receiver to start looking for an Electrical Idle Exit after successfully receiving an Electrical Idle ordered set

Table 50. Differential Receiver (RX) Input Specifications (continued)

Symbol	Parameter	Min	Nom	Max	Units	Comments
$T_{RX-IDLE-DET-DIFF-ENTERTIME}$	Unexpected Electrical Idle Enter Detect Threshold Integration Time	—	—	10	ms	An unexpected Electrical Idle ($V_{RX-DIFFp-p} < V_{RX-IDLE-DET-DIFFp-p}$) must be recognized no longer than $T_{RX-IDLE-DET-DIFF-ENTERING}$ to signal an unexpected idle condition.
$L_{TX-SKEW}$	Total Skew	—	—	20	ns	Skew across all lanes on a Link. This includes variation in the length of SKP ordered set (for example, COM and one to five Symbols) at the RX as well as any delay differences arising from the interconnect itself.

Notes:

1. No test load is necessarily associated with this value.
2. Specified at the measurement point and measured over any 250 consecutive UIs. The test load in [Figure 52](#) should be used as the RX device when taking measurements (also refer to the Receiver compliance eye diagram shown in [Figure 51](#)). If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.
3. A $T_{RX-EYE} = 0.40$ UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the Transmitter and interconnect collected any 250 consecutive UIs. The $T_{RX-EYE-MEDIAN-to-MAX-JITTER}$ specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total. UI jitter budget collected over any 250 consecutive TX UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as the reference for the eye diagram.
4. The Receiver input impedance shall result in a differential return loss greater than or equal to 15 dB with the D+ line biased to 300 mV and the D- line biased to -300 mV and a common mode return loss greater than or equal to 6 dB (no bias required) over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements for is 50 Ω to ground for both the D+ and D- line (that is, as measured by a Vector Network Analyzer with 50 ohm probes - see [Figure 52](#)). Note: that the series capacitors C_{TX} is optional for the return loss measurement.
5. Impedance during all LTSSM states. When transitioning from a Fundamental Reset to Detect (the initial state of the LTSSM) there is a 5 ms transition time before Receiver termination values must be met on all un-configured Lanes of a Port.
6. The RX DC Common Mode Impedance that exists when no power is present or Fundamental Reset is asserted. This helps ensure that the Receiver Detect circuit will not falsely assume a Receiver is powered on when it is not. This term must be measured at 300 mV above the RX ground.
7. It is recommended that the recovered TX UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function. Least squares and median deviation fits have worked well with experimental and simulated data.

14.5 Receiver Compliance Eye Diagrams

The RX eye diagram in [Figure 51](#) is specified using the passive compliance/test measurement load (see [Figure 52](#)) in place of any real PCI Express RX component.

Note: In general, the minimum Receiver eye diagram measured with the compliance/test measurement load (see [Figure 52](#)) will be larger than the minimum Receiver eye diagram measured over a range of systems at the input Receiver of any real PCI Express component. The degraded eye diagram at the input Receiver is due to traces internal to the package as well as silicon parasitic characteristics which cause the real PCI Express component to vary in impedance from the compliance/test measurement load. The input Receiver eye diagram is implementation specific and is not specified. RX component designer should

provide additional margin to adequately compensate for the degraded minimum Receiver eye diagram (shown in [Figure 51](#)) expected at the input Receiver based on some adequate combination of system simulations and the Return Loss measured looking into the RX package and silicon. The RX eye diagram must be aligned in time using the jitter median to locate the center of the eye diagram.

The eye diagram must be valid for any 250 consecutive UIs.

A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.

NOTE

The reference impedance for return loss measurements is 50Ω to ground for both the D+ and D- line (that is, as measured by a Vector Network Analyzer with 50Ω probes—see [Figure 52](#)). Note that the series capacitors, C_{TX} , are optional for the return loss measurement.

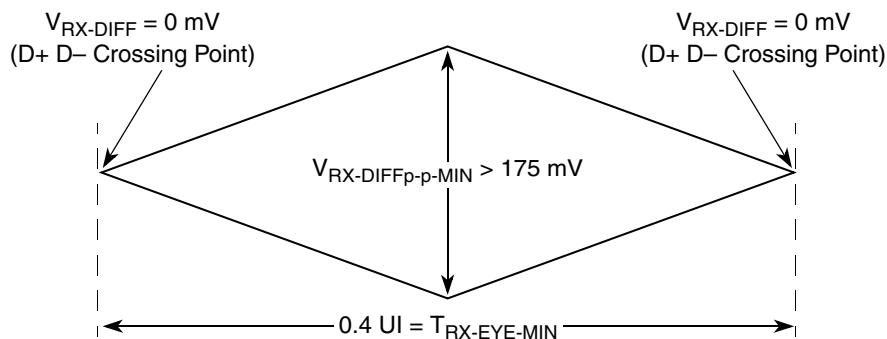


Figure 51. Minimum Receiver Eye Timing and Voltage Compliance Specification

14.5.1 Compliance Test and Measurement Load

The AC timing and voltage parameters must be verified at the measurement point, as specified within 0.2 inches of the package pins, into a test/measurement load shown in [Figure 52](#).

NOTE

The allowance of the measurement point to be within 0.2 inches of the package pins is meant to acknowledge that package/board routing may benefit from D+ and D- not being exactly matched in length at the package pin boundary.

Table 51. SDn_REF_CLK and $\overline{SDn_REF_CLK}$ AC Requirements

Symbol	Parameter Description	Min	Typical	Max	Units	Comments
t_{REF}	REFCLK cycle time	—	10(8)	—	ns	8 ns applies only to serial RapidIO with 125-MHz reference clock
t_{REFCJ}	REFCLK cycle-to-cycle jitter. Difference in the period of any two adjacent REFCLK cycles	—	—	80	ps	—
t_{REFPJ}	Phase jitter. Deviation in edge location with respect to mean edge location	–40	—	40	ps	—

15.3 Signal Definitions

LP-Serial links use differential signaling. This section defines terms used in the description and specification of differential signals. Figure 53 shows how the signals are defined. The figures show waveforms for either a transmitter output (TD and $\overline{TD}$) or a receiver input (RD and $\overline{RD}$). Each signal swings between A Volts and B Volts where $A > B$. Using these waveforms, the definitions are as follows:

1. The transmitter output signals and the receiver input signals TD, $\overline{TD}$, RD and $\overline{RD}$ each have a peak-to-peak swing of $A - B$ Volts
2. The differential output signal of the transmitter, V_{OD} , is defined as $V_{TD} - V_{\overline{TD}}$
3. The differential input signal of the receiver, V_{ID} , is defined as $V_{RD} - V_{\overline{RD}}$
4. The differential output signal of the transmitter and the differential input signal of the receiver each range from $A - B$ to $-(A - B)$ Volts
5. The peak value of the differential transmitter output signal and the differential receiver input signal is $A - B$ Volts
6. The peak-to-peak value of the differential transmitter output signal and the differential receiver input signal is $2 * (A - B)$ Volts

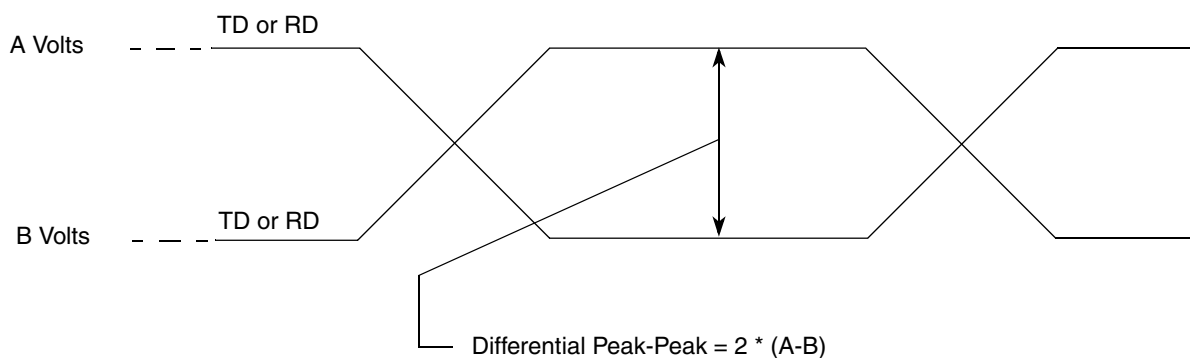


Figure 53. Differential Peak-Peak Voltage of Transmitter or Receiver

To illustrate these definitions using real values, consider the case of a CML (Current Mode Logic) transmitter that has a common mode voltage of 2.25 V and each of its outputs, TD and $\overline{TD}$, has a swing that goes between 2.5V and 2.0V. Using these values, the peak-to-peak voltage swing of the signals TD and $\overline{TD}$ is 500 mV p-p. The differential output signal ranges between 500 mV and –500 mV. The peak differential voltage is 500 mV. The peak-to-peak differential voltage is 1000 mV p-p.

Table 63. MPC8641 Signal Reference by Functional Block (continued)

Name ¹	Package Pin Number	Pin Type	Power Supply	Notes
SD1_PLL_TPA	T28	Analog	SV _{DD}	13, 18
SD1_DLL_TPD	N28	O	SV _{DD}	13, 17
SD1_DLL_TPA	P31	Analog	SV _{DD}	13, 18
High Speed I/O Interface 2 (SERDES 2)⁴				
SD2_TX[0:3]	Y24, AA27, AB25, AC27	O	SV _{DD}	—
SD2_TX[4:7]	AE27, AG27, AJ27, AL27	O	SV _{DD}	34
$\overline{\text{SD2_TX}}[0:3]$	Y25, AA28, AB26, AC28	O	SV _{DD}	—
$\overline{\text{SD2_TX}}[4:7]$	AE28, AG28, AJ28, AL28	O	SV _{DD}	34
SD2_RX[0:3]	Y30, AA32, AB30, AC32	I	SV _{DD}	32
SD2_RX[4:7]	AH30, AJ32, AK30, AL32	I	SV _{DD}	32, 35
$\overline{\text{SD2_RX}}[0:3]$	Y29, AA31, AB29, AC31	I	SV _{DD}	—
$\overline{\text{SD2_RX}}[4:7]$	AH29, AJ31, AK29, AL31	I	SV _{DD}	35
SD2_REF_CLK	AE32	I	SV _{DD}	—
$\overline{\text{SD2_REF_CLK}}$	AE31	I	SV _{DD}	—
SD2_IMP_CAL_TX	AM29	Analog	SV _{DD}	19
SD2_IMP_CAL_RX	AA26	Analog	SV _{DD}	30
SD2_PLL_TPD	AF29	O	SV _{DD}	13, 17
SD2_PLL_TPA	AF31	Analog	SV _{DD}	13, 18
SD2_DLL_TPD	AD29	O	SV _{DD}	13, 17
SD2_DLL_TPA	AD30	Analog	SV _{DD}	13, 18
Special Connection Requirement pins				
No Connects	K24, K25, P28, P29, W26, W27, AD25, AD26	—	—	13
Reserved	H30, R32, V28, AG32	—	—	14
Reserved	H29, R31, W28, AG31	—	—	15
Reserved	AD24, AG26	—	—	16
Ethernet Miscellaneous Signals⁵				
EC1_GTX_CLK125	AL23	I	LV _{DD}	39
EC2_GTX_CLK125	AM23	I	TV _{DD}	39
EC_MDC	G31	O	OV _{DD}	—
EC_MDIO	G32	I/O	OV _{DD}	—
eTSEC Port 1 Signals⁵				

Table 63. MPC8641 Signal Reference by Functional Block (continued)

Name ¹	Package Pin Number	Pin Type	Power Supply	Notes
TSEC1_TXD[0:7]/ GPOUT[0:7]	AF25, AC23, AG24, AG23, AE24, AE23, AE22, AD22	O	LV _{DD}	6, 10
TSEC1_TX_EN	AB22	O	LV _{DD}	36
TSEC1_TX_ER	AH26	O	LV _{DD}	—
TSEC1_TX_CLK	AC22	I	LV _{DD}	40
TSEC1_GTX_CLK	AH25	O	LV _{DD}	41
TSEC1_CRS	AM24	I/O	LV _{DD}	37
TSEC1_COL	AM25	I	LV _{DD}	—
TSEC1_RXD[0:7]/ GPIN[0:7]	AL25, AL24, AK26, AK25, AM26, AF26, AH24, AG25	I	LV _{DD}	10
TSEC1_RX_DV	AJ24	I	LV _{DD}	—
TSEC1_RX_ER	AJ25	I	LV _{DD}	—
TSEC1_RX_CLK	AK24	I	LV _{DD}	40
eTSEC Port 2 Signals⁵				
TSEC2_TXD[0:3]/ GPOUT[8:15]	AB20, AJ23, AJ22, AD19	O	LV _{DD}	6, 10
TSEC2_TXD[4]/ GPOUT[12]	AH23	O	LV _{DD}	6, 10, 38
TSEC2_TXD[5:7]/ GPOUT[13:15]	AH21, AG22, AG21	O	LV _{DD}	6, 10
TSEC2_TX_EN	AB21	O	LV _{DD}	36
TSEC2_TX_ER	AB19	O	LV _{DD}	6, 38
TSEC2_TX_CLK	AC21	I	LV _{DD}	40
TSEC2_GTX_CLK	AD20	O	LV _{DD}	41
TSEC2_CRS	AE20	I/O	LV _{DD}	37
TSEC2_COL	AE21	I	LV _{DD}	—
TSEC2_RXD[0:7]/ GPIN[8:15]	AL22, AK22, AM21, AH20, AG20, AF20, AF23, AF22	I	LV _{DD}	10
TSEC2_RX_DV	AC19	I	LV _{DD}	—
TSEC2_RX_ER	AD21	I	LV _{DD}	—
TSEC2_RX_CLK	AM22	I	LV _{DD}	40
eTSEC Port 3 Signals⁵				
TSEC3_TXD[0:3]	AL21, AJ21, AM20, AJ20	O	TV _{DD}	6
TSEC3_TXD[4]/	AM19	O	TV _{DD}	—
TSEC3_TXD[5:7]	AK21, AL20, AL19	O	TV _{DD}	6

Table 63. MPC8641 Signal Reference by Functional Block (continued)

Name ¹	Package Pin Number	Pin Type	Power Supply	Notes
AGND_SRDS1	P30	SerDes Port 1 Ground pin for AV _{DD} _SRDS1	—	—
AGND_SRDS2	AF30	SerDes Port 2 Ground pin for AV _{DD} _SRDS2	—	—
SGND	H28, H32, J30, K31, L28, L29, M32, N30, R29, T32, U30, V31, W29, Y32 AA30, AB31, AC29, AD32, AE30, AG29, AH32, AJ30, AK31, AL29, AM32	Ground pins for SV _{DD}	—	—
XGND	K27, L25, M26, N24, P27, R25, T26, U24, V27, W25, Y28, AA24, AB27, AC25, AD28, AE26, AF27, AH28, AJ26, AK27, AL26, AM28	Ground pins for XV _{DD} _SRDS _n	—	—
Reset Configuration Signals²⁰				
TSEC1_TXD[0] / cfg_alt_boot_vec	AF25	—	LV _{DD}	—
TSEC1_TXD[1] / cfg_platform_freq	AC23	—	LV _{DD}	21
TSEC1_TXD[2:4] / cfg_device_id[5:7]	AG24, AG23, AE24	—	LV _{DD}	—
TSEC1_TXD[5] / cfg_tsec1_reduce	AE23	—	LV _{DD}	—
TSEC1_TXD[6:7] / cfg_tsec1_prtcl[0:1]	AE22, AD22	—	LV _{DD}	—
TSEC2_TXD[0:3] / cfg_rom_loc[0:3]	AB20, AJ23, AJ22, AD19	—	LV _{DD}	—
TSEC2_TXD[4], TSEC2_TX_ER / cfg_dram_type[0:1]	AH23, AB19	—	LV _{DD}	38
TSEC2_TXD[5] / cfg_tsec2_reduce	AH21	—	LV _{DD}	—
TSEC2_TXD[6:7] / cfg_tsec2_prtcl[0:1]	AG22, AG21	—	LV _{DD}	—
TSEC3_TXD[0:1] / cfg_spare[0:1]	AL21, AJ21	O	TV _{DD}	33
TSEC3_TXD[2] / cfg_core1_enable	AM20	O	TV _{DD}	—
TSEC3_TXD[3] / cfg_core1_lm_offset	AJ20	—	LV _{DD}	—
TSEC3_TXD[5] / cfg_tsec3_reduce	AK21	—	LV _{DD}	—

Table 63. MPC8641 Signal Reference by Functional Block (continued)

Name ¹	Package Pin Number	Pin Type	Power Supply	Notes
TSEC3_TXD[6:7]/ cfg_tsec3_prctl[0:1]	AL20, AL19	—	LV _{DD}	—
TSEC4_TXD[0:3]/ cfg_io_ports[0:3]	AC18, AC16, AD18, AD17	—	LV _{DD}	—
TSEC4_TXD[5]/ cfg_tsec4_reduce	AB18	—	LV _{DD}	—
TSEC4_TXD[6:7]/ cfg_tsec4_prctl[0:1]	AB17, AB16	—	LV _{DD}	—
LAD[0:31]/ cfg_gpporcr[0:31]	A30, E29, C29, D28, D29, H25, B29, A29, C28, L22, M22, A28, C27, H26, G26, B27, B26, A27, E27, G25, D26, E26, G24, F27, A26, A25, C25, H23, K22, D25, F25, H22	—	OV _{DD}	—
$\overline{\text{LWE}}[0]/$ cfg_cpu_boot	E21	—	OV _{DD}	—
$\overline{\text{LWE}}[1]/$ cfg_rio_sys_size	F21	—	OV _{DD}	—
$\overline{\text{LWE}}[2:3]/$ cfg_host_agt[0:1]	D22, E20	—	OV _{DD}	—
LDP[0:3], LA[27] / cfg_core_pll[0:4]	A24, E24, C24, B24, J21	—	OV _{DD}	22
LA[28:31]/ cfg_sys_pll[0:3]	K21, G22, F24, G21	—	OV _{DD}	22
LGPL[3], LGPL[5]/ cfg_boot_seq[0:1]	K20, J19	—	OV _{DD}	—
D1_MSRCID[0]/ cfg_mem_debug	F15	—	OV _{DD}	—
D1_MSRCID[1]/ cfg_ddr_debug	K15	—	OV _{DD}	—

Another useful equation is:

$$V_H - V_L = n \frac{KT}{q} \left[\ln \frac{I_H}{I_L} \right]$$

Where:

I_{fw} = Forward current

I_s = Saturation current

V_d = Voltage at diode

V_f = Voltage forward biased

V_H = Diode voltage while I_H is flowing

V_L = Diode voltage while I_L is flowing

I_H = Larger diode bias current

I_L = Smaller diode bias current

q = Charge of electron (1.6×10^{-19} C)

n = Ideality factor (normally 1.0)

K = Boltzman's constant (1.38×10^{-23} Joules/K)

T = Temperature (Kelvins)

The ratio of I_H to I_L is usually selected to be 10:1. The above simplifies to the following:

$$V_H - V_L = 1.986 \times 10^{-4} \times nT$$

Solving for T , the equation becomes:

$$nT = \frac{V_H - V_L}{1.986 \times 10^{-4}}$$

For other pin pull-up or pull-down recommendations of signals, please see [Section 17, “Signal Listings.”](#)

20.7 Output Buffer DC Impedance

The MPC8641 drivers are characterized over process, voltage, and temperature. For all buses, the driver is a push-pull single-ended driver type (open drain for I²C).

To measure Z_0 for the single-ended drivers, an external resistor is connected from the chip pad to OV_{DD} or GND. Then, the value of each resistor is varied until the pad voltage is $OV_{DD}/2$ (see [Figure 66](#)). The output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held high, SW1 is closed (SW2 is open) and R_P is trimmed until the voltage at the pad equals $OV_{DD}/2$. R_P then becomes the resistance of the pull-up devices. R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N)/2$.

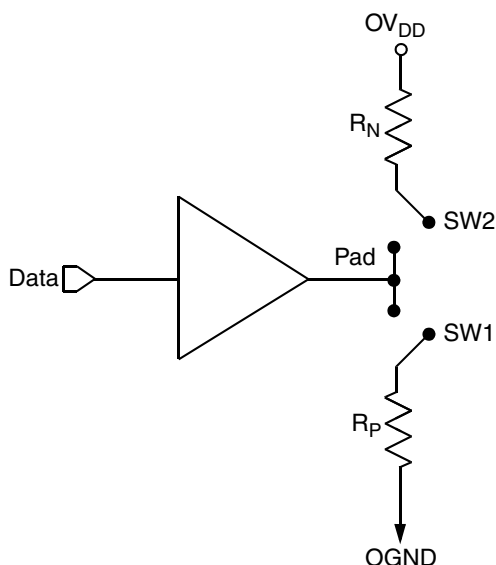


Figure 66. Driver Impedance Measurement

[Table 73](#) summarizes the signal impedance targets. The driver impedances are targeted at minimum V_{DD} , nominal OV_{DD} , 105°C.

Table 73. Impedance Characteristics

Impedance	DUART, Control, Configuration, Power Management	PCI Express	DDR DRAM	Symbol	Unit
R_N	43 Target	25 Target	20 Target	Z_0	W
R_P	43 Target	25 Target	20 Target	Z_0	W

Note: Nominal supply voltages. See [Table 1](#), $T_j = 105^\circ\text{C}$.

21 Ordering Information

Ordering information for the parts fully covered by this specification document is provided in [Section 21.1, “Part Numbers Fully Addressed by This Document.”](#)

21.1 Part Numbers Fully Addressed by This Document

[Table 74](#) provides the Freescale part numbering nomenclature for the MPC8641. Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Freescale sales office. In addition to the processor frequency, the part numbering scheme also includes an application modifier which may specify special application conditions. Each part number also contains a revision code which refers to the die mask revision number.

Table 74. Part Numbering Nomenclature

MC	nnnn	x	xx	nnnn	x	x
Product Code	Part Identifier	Core Count	Package ¹	Core Processor Frequency ² (MHz)	DDR speed (MHz)	Product Revision Level
MC	8641	Blank = Single Core D = Dual Core	HX = High-lead HCTE FC-CBGA VU = RoHS lead-free HCTE FC-CBGA ⁵ VJ = lead-free HCTE FC-CBGA ⁶	1000, 1250, 1333, 1500	N = 500 MHz ⁴ K = 600 MHz J = 533 MHz H = 500 MHz G = 400 MHz	Revision B = 2.0 System Version Register Value for Rev B: 0x8090_0020 - MPC8641 0x8090_0120 - MPC8641D Revision C = 2.1 System Version Register Value for Rev C: 0x8090_0021 - MPC8641 0x8090_0121 - MPC8641D Revision E = 3.0 System Version Register Value for Rev E: 0x8090_0030 - MPC8641 0x8090_0130 - MPC8641D

Notes:

1. See [Section 16, “Package,”](#) for more information on available package types.
2. Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by part number specifications may support other maximum core frequencies.
3. The P prefix in a Freescale part number designates a “Pilot Production Prototype” as defined by Freescale SOP 3-13. These parts have only preliminary reliability and characterization data. Before pilot production prototypes may be shipped, written authorization from the customer must be on file in the applicable sales office acknowledging the qualification status and the fact that product changes may still occur while shipping pilot production prototypes.
4. Part Number MC8641xxx1000NX is our low V_{DD_Coren} device. $V_{DD_Coren} = 0.95\text{ V}$ and $V_{DD_PLAT} = 1.05\text{ V}$.
5. VU part number is RoHS compliant with the permitted exception of the C4 die bumps.
6. VJ part number is entirely lead-free including the C4 die bumps.

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